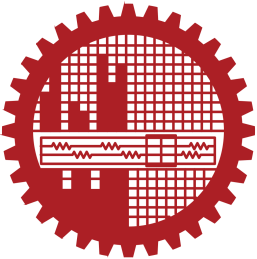
**BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY**



Gate Driver

**Prepared by- Submitted to-**

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**Task**

Further look into why and how the gate current looks like this shape, and change the gate drive (e.g. an ideal voltage pulse source) and compare the gate curves.

**Parasitic Capacitors of MOSFET:**

**capacitors.emf**

Here,

Gate to source capacitance, CGS

Gate to drain Capacitance, CGD (Miller Capacitance)

Drain to source Capacitance, CDS

And,

Input Capacitance, CISS = CGS + CGD

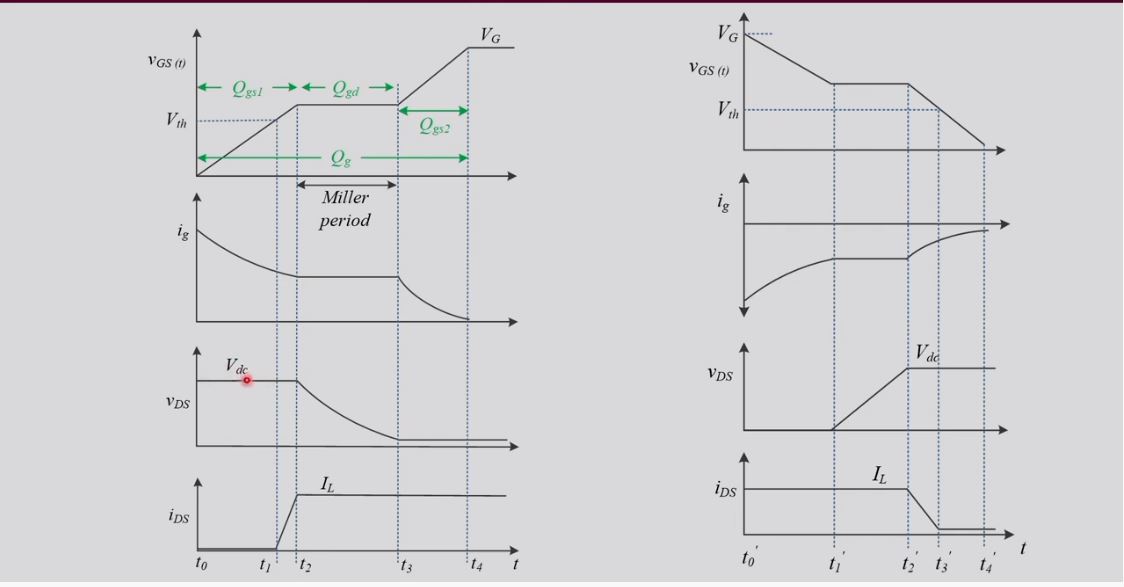
Output Capacitance, COSS = CDS + CGD

Reverse Transfer Capacitance, CRSS = CGD

“CGD plays an important role to On and Off the MOSFET.”

**Gate Current:**

From lecture video of **Prof. Shabari Nath(IIT,India)** we found,

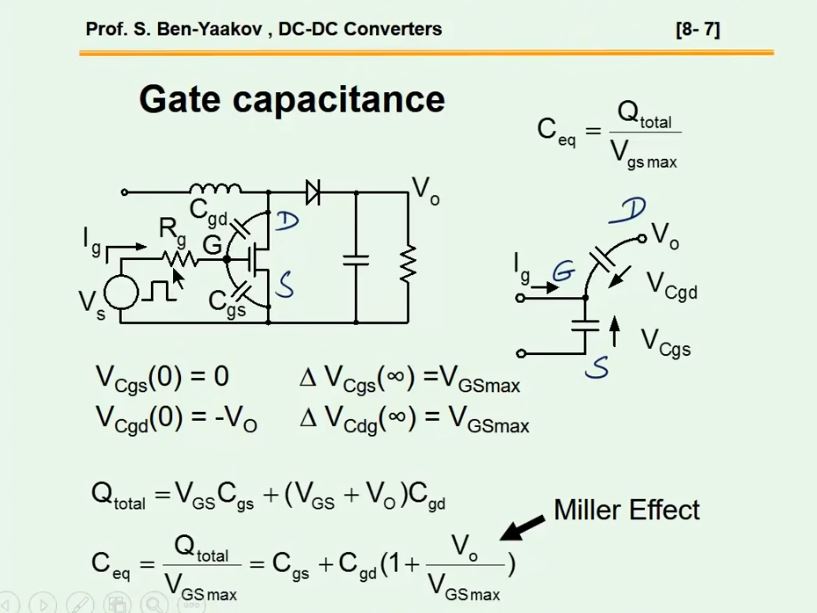


Here,

Gate current is not smooth. First it will get a peak then decrease with time. After some time current remain constant for few moments. This is caused by **“Miller Effect”**.

When the gate current and voltage waveshape is parallel to the time axis then it is called **“Miller Plateau”** region occurred by Miller Effect.

Here is the equation for this found from **Prof. S. Ben Yaakov’s** lecture on Miller effect,

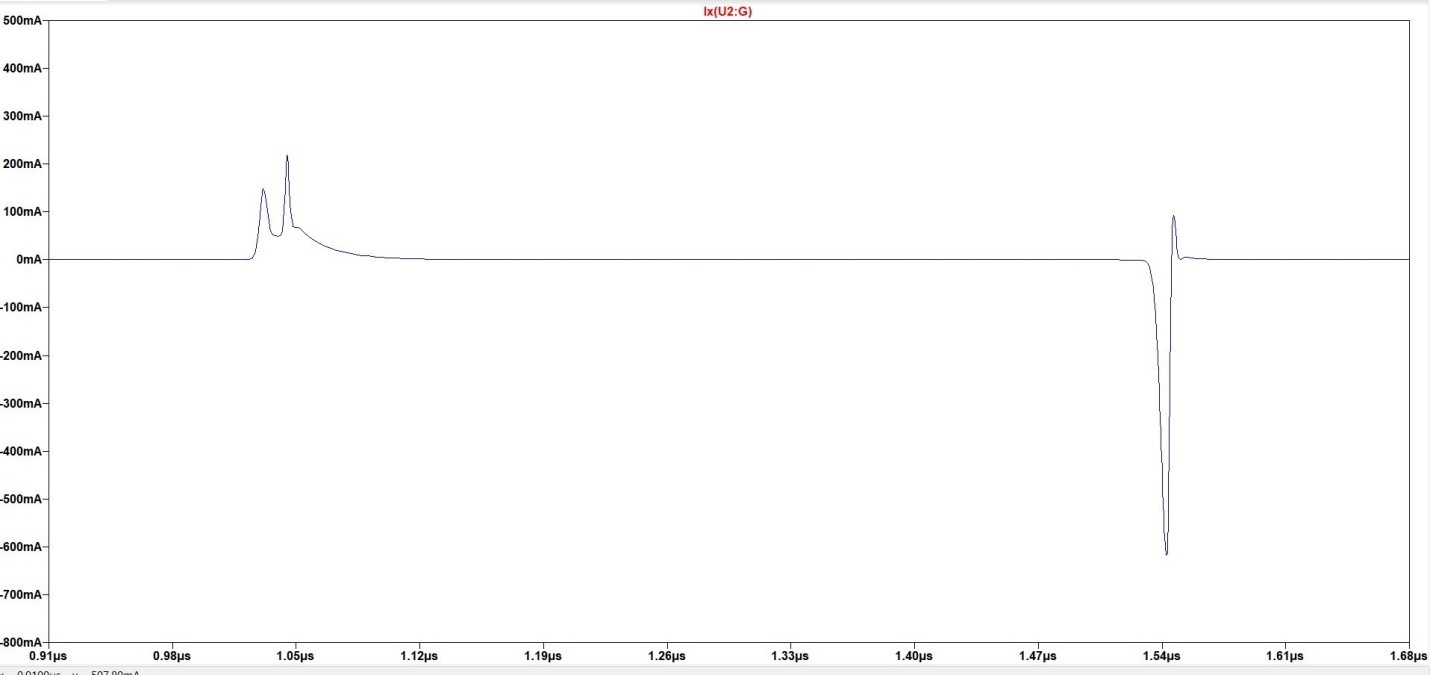


This extra Cgd capacitance causes Miller effect on the waveshape.

**Previous circuit(with Diode),**

cktwd.emf

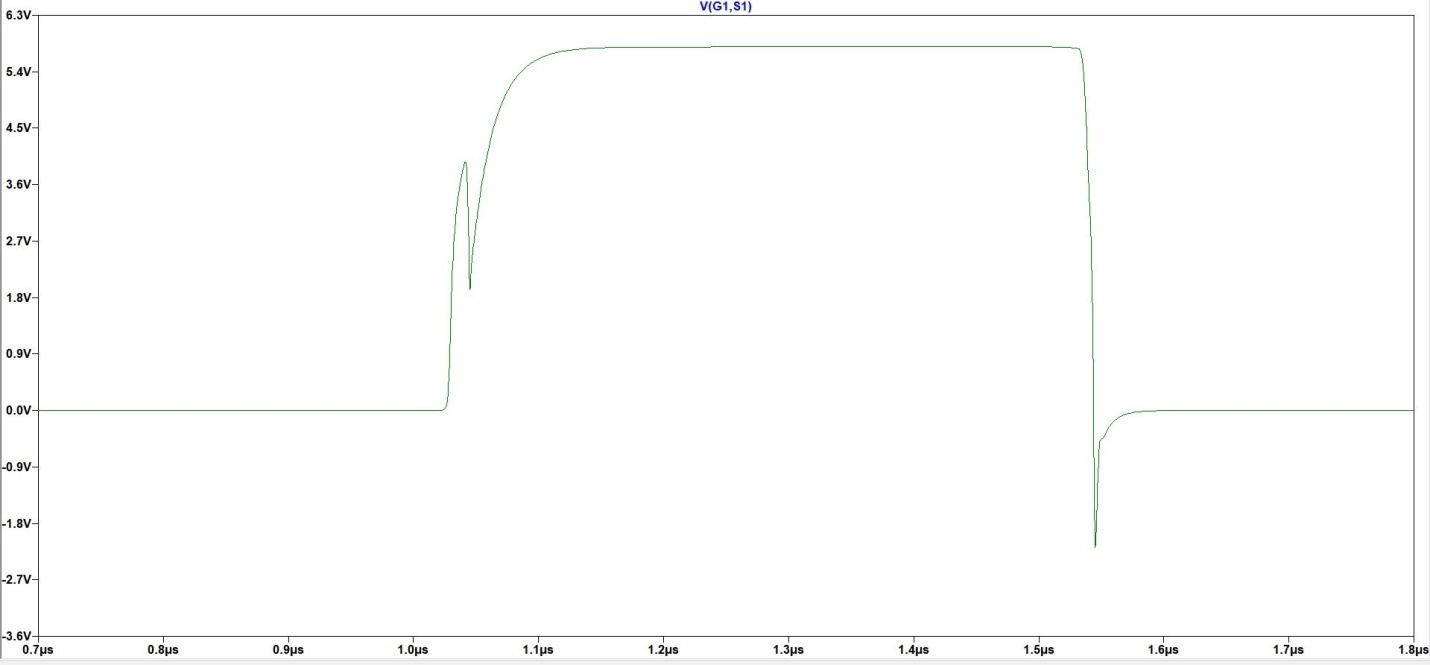
**On-Off Gate Current:**



During On, gate pulse “Miller Plateau” and 2 peaks.

During off, gate pulse doesn’t have a “Miller Plateau” region.

**Gate to source Voltage:**

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There is “Miller Plateau” during turning on, but not in turning off time rather having a negative voltage spike.

**If we Disconnect diode D1 and D2, the circuit:**

**(\*Datasheet suggest that diode part is optional)**

withoutd.emf

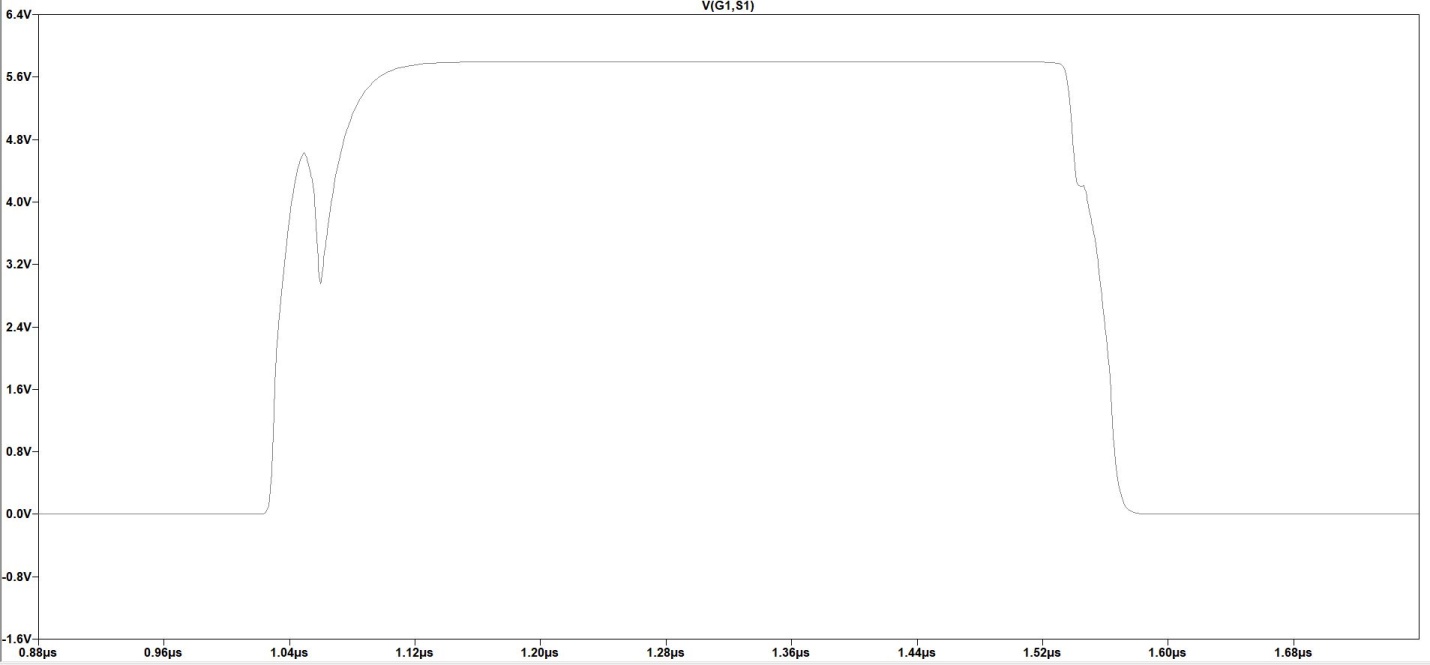
**Waveshape of Gate current:**

gate_currentWOD.emf

During Turn On, wavehape showing “Miller plateau”.

During Turn Off, again no “Miller plateau” region.

**Gate to Source voltage:**

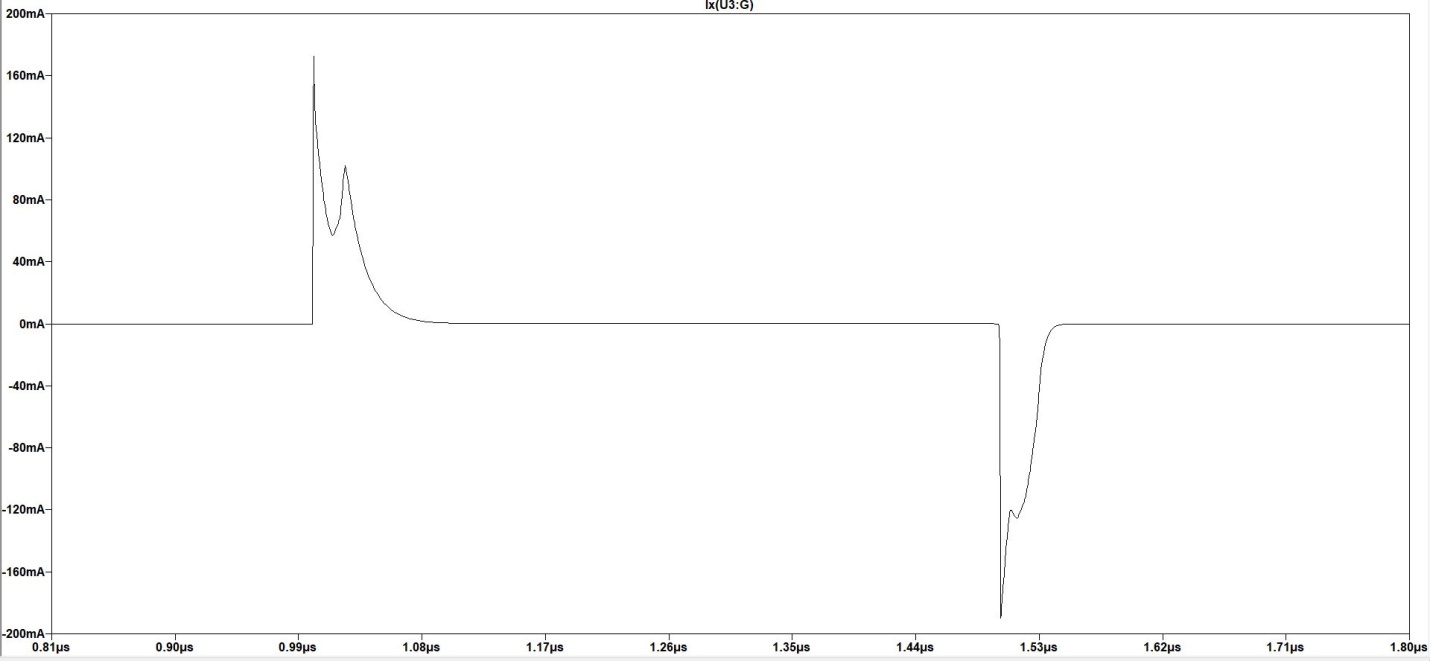
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Reduction of “Miller plateau” in turning off time and no negative voltage spike.

**Circuit with Voltage Pulse(without driver):**

cktwpulse.emf

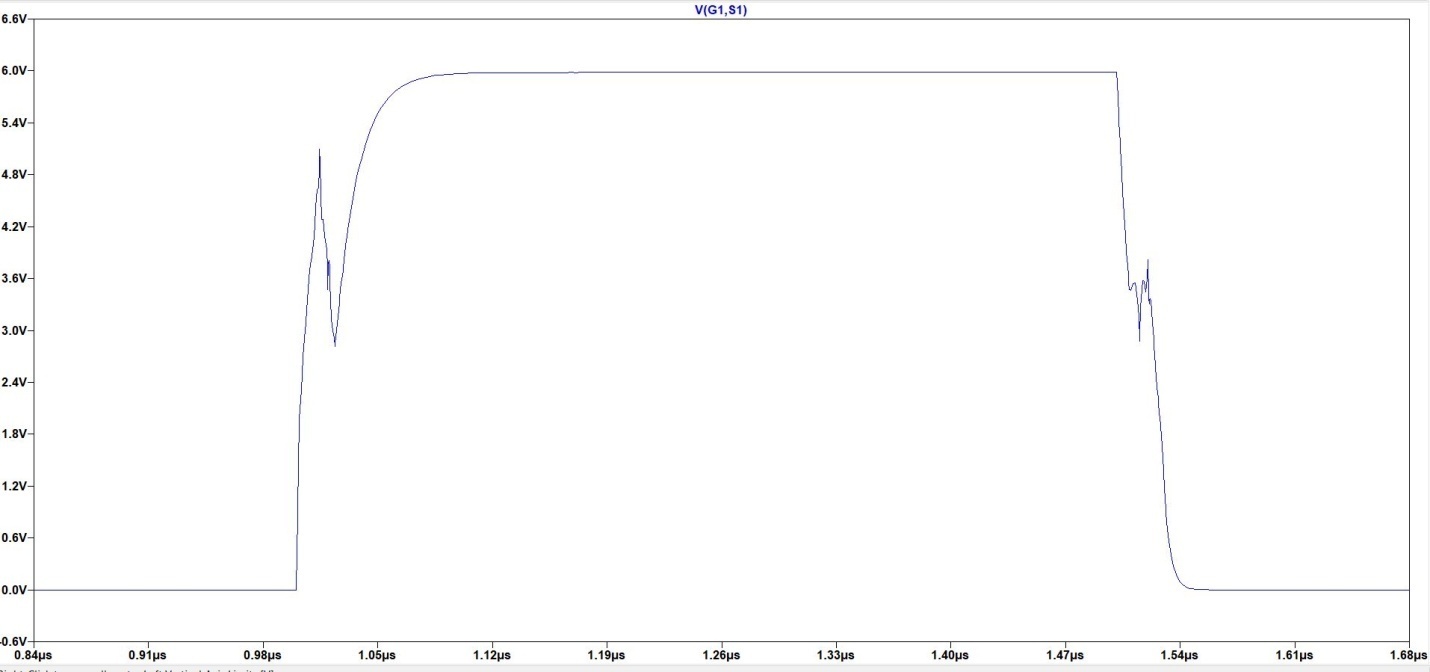
**Gate Current:**

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Here,

During on and off both time there is expected “Miller Plateau” region.

**Gate to source voltage:**



Here is also found expected “Miller Plateau” region during on and off of the MOSFET.

**Comparison**

**\*With driver circuit,** there is less Miller effect. But need to choose proper Rg on/off resistor & diode for better performance.

**\*Without driver,** more Miller effect.