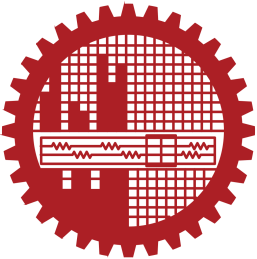
**BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY**



H-Bridge with Phase Shifted PWM

**Prepared by-**

Sagar Kumar Das

MSc’22

BUET

Supervised by- Submitted to-

**Nadim Chowdhury Dr. Cheng Zhang**

Assistant Professor, BUETLecturer, University of Manchester

**Task**

H-Bridge circuit with phase shifted PWM

**H Bridge Circuit:**

full_bridge.emf

This circuit designed with **ADuM4121 gate driver** for 100V and 1K output resistance. Though Voltage and resistance can change.

**Gate Current:**

gate_current.emf

Gate current is showing same waveshape like previous assignment. So Circuit is working.

**Gate to Source Voltage:**

**gate2source_voltage.emf**

This waveshape is showing gate to source voltages from different side of the circuit. For this we take duty cycle of 0.5(half time on & half time off).

**Output Voltage:**

**Output_voltage.emf**

Output voltage is showing its ringing between +100 to -100V in 50% duty cycle.

**Phase Shifted PWM generator circuit:**

**Signal_generator.emf**

**[Reference:** [**https://youtu.be/0hgoZGzc3Vw**](https://youtu.be/0hgoZGzc3Vw)**]**

**Output(A8 and A2) with carrier and Duty cycle(D=0.1) :**

**carrier&referece.emf**

Figure showing that, Vc(ramp func.) and d=0.1V input of a comparator.

**Dead Time:**

dead_time.emf

From graph, we can see dead time is very close to calculated value of 0.0007µm. [Dead time means time difference between MOSFET’s turning on-off to avoid overlap of switching.]

**Signal Generator connected H-Bridge:**

**H_bridge_with_phase_shifted.emf**

M1, M2, M3, M4 points are connected to the gate driver through VCVS with gain=5 that controls the gate to source voltage.

**At D=0.1:**

**d=0.1.emf**

Figure showing voltage across the output resistor with duty cycle 0.1

**At D=0.4:**

**d=0.4.emf**

Figure showing voltage across the output resistor with duty cycle 0.4