



## Enhancement-Mode GaN Transistor Technology for Harsh Environment Operation

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# Enhancement-Mode GaN Transistor Technology for Harsh Environment Operation

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**Abstract**—This letter reports an enhancement-mode (E-mode) GaN transistor technology which has been demonstrated to operate in a simulated Venus environment ( $460^{\circ}\text{C}$ ,  $\approx 90\text{ atm}$ ,  $\text{CO}_2/\text{N}_2$ ) for 10 days. The robustness of the W/p-GaN-gate AlGaN/GaN high electron mobility transistor (HEMT) was evaluated by two complementary approaches, (1) *in-situ* electrical characterization, where proper transistor operation (including E-mode  $V_{TH}$  with  $<0.09\text{ V}$  variation) was demonstrated in extreme environments; and (2) advanced microscopy investigation of the device after test, which highlighted the effect of the testing on the epitaxial structure. To the best of the authors' knowledge, this is the first demonstration and comprehensive analysis of E-mode GaN transistors in such harsh environments. The results establish the reported technology as a leading option for harsh environment mixed-signal applications.

**Index Terms**—GaN, transistor, enhancement-mode, mixed-signal, harsh environment, Venus, high temperature, high pressure, corrosive gas, degradation, microscopy

## I. INTRODUCTION

ELECTRONICS operating at high temperature (HT), well above the effective  $250\text{--}300^{\circ}\text{C}$  limit of silicon-on-insulator (SOI) technology, are critical in enabling emerging applications in aerospace, automotive, geothermal, and oil and gas extraction [1], [2]. A promising solution is GaN and III-N thanks to its superior electrical, mechanical, and chemical properties, which have enabled a wide range of devices including transistors, MEMS and solar cells [3]–[5]. GaN electronics have demonstrated excellent performance in extreme environments (from cryogenic to high temperatures) across RF [6]–[8], power [9]–[11] and mixed-signal applications [12] using cost-competitive GaN-on-Si wafers.

Initial experiments have indicated the promising potential of E/D-mode n-FETs (E: enhancement; D: depletion) [13] and complementary (n-FET and p-FET) configurations [14], [15] for GaN HT integrated circuits. The key enabler (and challenge) is high performance E-mode transistor operation. p-GaN-gate AlGaN/GaN HEMTs are of significant interest thanks to their possibility of monolithic integration in both

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E/D-mode and complementary platforms [16]. Given the rapid advancement of GaN HT technology, in particular in mixed-signal circuits [12], [17], [18], it is an opportune time to examine the robustness of E-mode GaN technology under realistic harsh environments to further optimize these transistors.

In this work, an E-mode GaN transistor technology was demonstrated, characterized, and analyzed up to  $500^{\circ}\text{C}$ . Testing in a realistic harsh environment (beyond the typical SOI rating) reveals the unexplored potential of E-mode GaN technology for these applications. The robustness of the proposed transistor was comprehensively evaluated by *in-situ* electrical characterization, and advanced microscopy investigation.

## II. TRANSISTOR TECHNOLOGY

The proposed p-GaN-gate AlGaN/GaN-on-Si HEMTs [Fig. 1(a)] were fabricated with several features distinct from conventional p-GaN-gate HEMTs, namely, a gate-first process, a refractory metal gate (Tungsten, W), and self-alignment in the metal/p-GaN gate. These device features result in improved thermal stability, reduced hysteresis [19], and high scaling potential [16]. A  $\text{SiO}_2$  layer (200 nm) was deposited using tetraethyl orthosilicate (TEOS), followed by via opening. Lastly, Ti (20 nm)/Au (300 nm) bonding pads were formed to allow for subsequent packaging for *in-situ* measurement.

## III. TEMPERATURE DEPENDENCY

The bare die was characterized in a probe station with a thermal chuck (rating of  $500^{\circ}\text{C}$ ) in air. As shown in Fig. 1(b)–(c),  $V_{TH}$  is relatively stable below  $300^{\circ}\text{C}$ . The small initial increase of  $V_{TH}$  from room temperature to  $200^{\circ}\text{C}$  can be attributed to a higher acceptor (Mg) ionization ratio in p-GaN at increasing temperature. Above  $300^{\circ}\text{C}$ , a decrease in  $V_{TH}$  is observed. The gate region may be modeled as two back-to-back junctions [Fig. 1(c) inset], the Schottky junction (W/p-GaN) and the p-i-n junction (p-GaN/AlGaN/GaN). The trend of  $V_{TH}$  could be explained by the lower forward turn-on voltage of p-i-n junction, and reduced Schottky barrier height.

The gate leakage current characteristics is shown in Fig. 1(d). Below the turn-on voltage of the p-i-n junction, the vertical junction current is blocked by the p-i-n junction. The gate leakage current is dominated by the surface current (two-dimensional variable range hopping, 2D-VRH), leading to the increase of  $I_G$  over temperature and voltage-independent conductance  $\sigma \propto \exp(-T^{-1/3})$  [Fig. 1(e)] [20]. The vertical junction current dominates the gate leakage current at a large forward bias. The turn-on current  $I_G$  decreases with increasing temperature due to increased resistance in the drift region of p-i-n junction.  $I_G$  shows a similar trend as  $I_D$  up to  $500^{\circ}\text{C}$  due to the reduced mobility [Fig. 1(f)] [21].

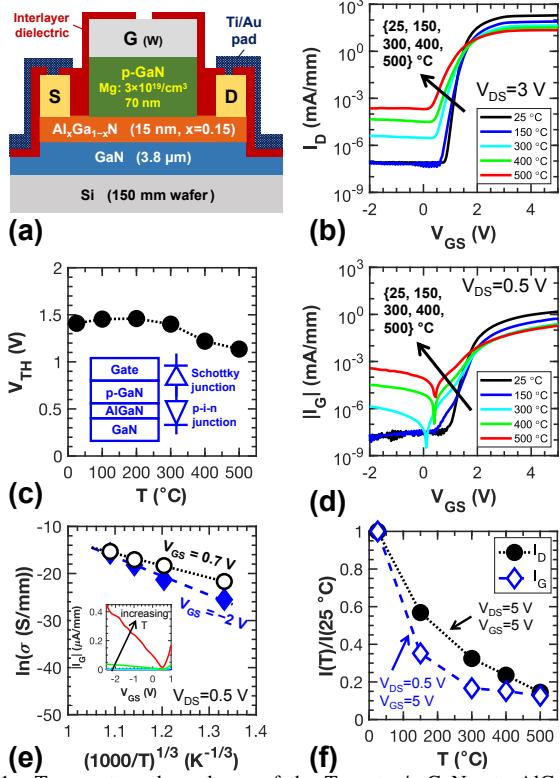


Fig. 1. Temperature dependency of the Tungsten/p-GaN-gate AlGaN/GaN HEMT up to 500 °C. (a) Device structure. (b)  $I_D$  vs.  $V_{GS}$ . (c)  $V_{TH}$ . (Inset: A simple two-diode model for the gate region.) (d)  $|I_G|$  vs.  $V_{GS}$ . (e) 2D-VRH model.  $I_G$  (linear scale) near the  $V_{GS} = 0$  V bias is shown in the inset. (f)  $I_D$  and  $I_G$  vs. temperature normalized to their room temperature values.

#### IV. ROBUSTNESS IN HARSH ENVIRONMENT

The device under test (DUT) was packaged using HT-rated components [2], [22] and placed in a simulated Venus environment (460 °C, ≈ 90 atm., mainly CO<sub>2</sub>/N<sub>2</sub> [23]) over 10 days in the NASA Glenn Extreme Environments Rig (GEER) [Fig. 2(a)] [24]. An automated setup ensured that *in-situ* measurements of the DUT could be made at regular time intervals (≈ 70 min.). A comparison of the DC characteristics [Fig. 2(b)–(c)] reveals that good transistor operation was maintained at the end of the test. Throughout the test, accurate control of the chamber temperature was maintained [Fig. 2(d)(i)]. It was observed that  $I_{D,max}$  of the package DUT (50 mA/mm) was lower than that of the bare die DUT (30 mA/mm), likely due to the degradation of the packaging (e.g. bond pad) [22].

The transistor metrics over time are presented in Fig. 2(d)(ii)–(vi). A stable  $V_{TH}$  of 0.9 ~ 1 V (E-mode) was maintained, throughout harsh environment stress over 10 days. Assuming  $V_{DD} = 5$  V operation and no  $V_{SS}$  [19], the peak-to-peak variation (< 0.09 V) corresponds to 1.8 % of the rail-to-rail voltage. The current decreased by ≈ 5.3 mA/mm (17 %), and  $R_{ON}$  increased by 9 Ω-mm (12 %), likely caused by degradation of the intrinsic transistor and bond pad in the test environment. A stable gate leakage (< 0.1 mA/mm variation, 12 %) and current ON-OFF ratio (< 5 % variation in terms of order of magnitude, limited by gate leakage) was maintained.

At the end of the test, the DUT was characterized using advanced microscopy. The device structure was found to be largely intact [Fig. 3(a)]. The p-GaN-gate region deserves special attention because it enables E-mode operation of the

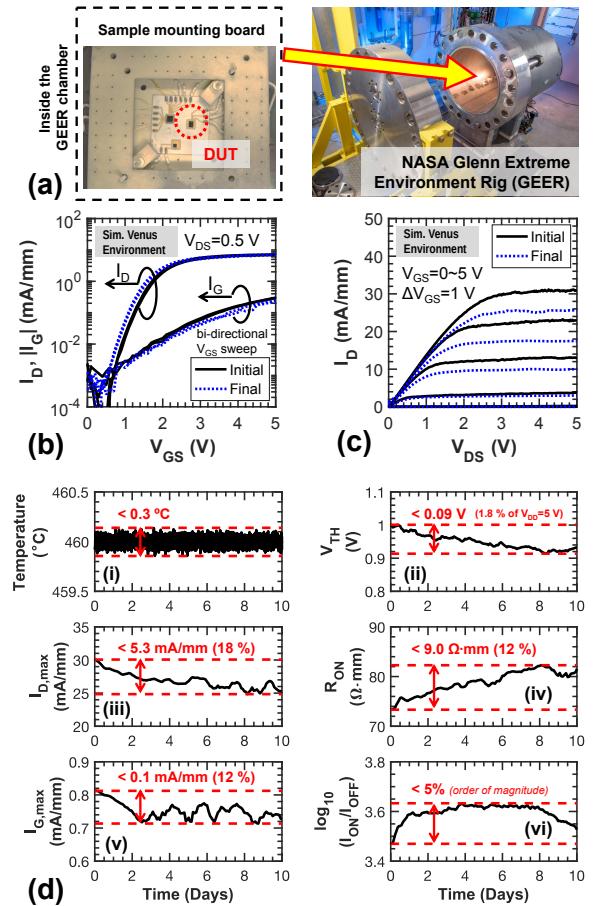


Fig. 2. (a) Setup which allows for the *in-situ* measurement of the DUT in a simulated Venus environment. (b)–(c) Transfer and output characteristics of the DUT for the initial measurement and the final measurement of the DUT in the simulated environment. (d) Variation of (i) temperature and (ii)–(vi) key transistor metrics during the test. For each metric, the absolute peak-to-peak value (in parenthesis: percentage of the peak-to-peak value with respect to the initial value, unless otherwise stated) are labelled.

DUT but the effect of harsh environment conditions has not been well studied. A p-GaN/AlGaN/GaN heterostructure was maintained, as reflected in the smooth interface between the epitaxial layers [Fig. 3(b)], and the crystallinity in p-GaN [Fig. 3(c)]. The p-GaN-gate region was fabricated by an optimized low-damage GaN/AlGaN selective etch recipe [25]. No noticeable degradation was found in the etched sidewall, AlGaN surface (etch stop layer), and the alloyed ohmic contact on the AlGaN surface [Fig. 3(d)–(e)]. A small crack (70 nm) was found in the SiO<sub>2</sub> layer [Fig. 3(f)], likely resulting from a mismatch in the thermal expansion coefficient between W (gate metal) and the SiO<sub>2</sub> which wraps around W. Overall, much of the structure is generally intact, but changes did occur. Future elemental analysis will be desired to understand if reactions of the device components occurred in the harsh simulated Venus surface conditions [26].

The robustness study of the proposed transistor was benchmarked against similar studies of GaN transistors in Table I [2], [6], [7], [22], [27]–[32]. To the best of the authors' knowledge, this is the first report of an E-mode GaN transistor working under a realistic harsh environment (> 300 °C and chemical environment). The reported transistor features competitive robustness, which is reflected in the relatively small degradation in both  $I_{D,max}$  and  $V_{TH}$ .

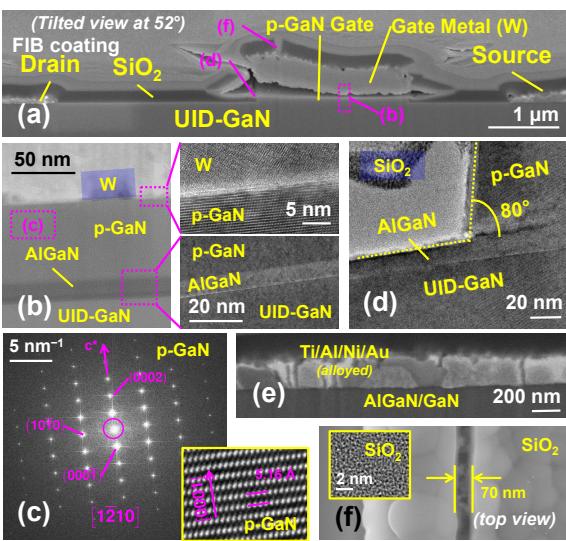


Fig. 3. Advanced microscopy investigation of the device after test. (a) FIB cross-sectional image of the DUT after the testing. (b) Zoom-in view of an intact region of the W/p-GaN/AlGaN/GaN structure (HAADF-STEM). The interfaces are shown in the insets (TEM). (c) Crystallinity (reciprocal lattice) of p-GaN (FFT of TEM). The inset shows the corresponding HRTEM image. (d) Sidewall of the p-GaN-gate region (TEM). (e) Drain contact located on the AlGaN/GaN surface (SEM). The original p-GaN on top of AlGaN was etched to expose the AlGaN surface for formation of ohmic contacts. (f) Small crack in the SiO<sub>2</sub> layer (top view, SEM). The inset shows the amorphous SiO<sub>2</sub> (TEM). All images are cross-sections unless otherwise stated. (FIB: focused ion beam; SEM: scanning electron microscope; TEM: transmission electron microscope; HAADF-STEM: high-angle annular dark-field scanning TEM; FFT: fast Fourier transform; HRTEM: high resolution TEM; UID: unintentionally doped.)

TABLE I  
ROBUSTNESS STUDIES OF GAN HEMTS IN HARSH ENVIRONMENT.

E/D-mode	Epitaxial Structure	Reference	Temp. (°C)	Ambient	Duration (h)	$\Delta V_{D,max}$ (%) <sup>(2)</sup>	$\Delta V_{th}$ (V) <sup>(2)</sup>
D	AlGaN /GaN	[7]	250	5% H <sub>2</sub> /95% N <sub>2</sub>	24	3	0.2
		[27]	400	Air	25	72	1.4
		[28]	175	N.A.	500	5	0.1
		[29]	525	N.A.	25	10	0.6
E	InAlN /GaN	[30]	900	Vacuum	50	100	N.A.
		[6]	1000	Vacuum	25	55	0.3
		[2]	465	Venus	240	30	0.04
	p-GaN /AlGaN /GaN	[31]	125	N.A.	5000	N.A.	0.15
This Work		[32]	85	High humidity	1000	N.A.	1
		[22]	500	N <sub>2</sub>	24	35	0.05
		This Work	460	Venus (complete chemical env.)	240	15	0.09

<sup>(1)</sup> Duration of *in-situ* measurement at the specified HT. <sup>(2)</sup> Values, if not explicitly reported, are based on best estimates from the published data.

## V. CONCLUSION

An E-mode GaN transistor technology was proposed and characterized. Its robustness in a realistic harsh environment was evaluated through both *in-situ* electrical characterization, and comprehensive microscopy of the epitaxial and device structures. This work demonstrated continued operation of the transistor after 10 days in simulated Venus condition, while some degradation of device operation and structure is observed. Nevertheless, the promising results serve as a foundation for further development of GaN for harsh environment mixed-signal electronics. This work also offers insights to p-GaN-gate HEMTs for harsh environment power electronics.

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