

UNIVERSITY OF BATANGAS – LIPA CAMPUS COLLEGE OF ENGINEERING AND ARCHITECTURE COMPUTER ENGINEERING

Arithmetic Circuits - Adders / Subtractors

Experiment #5

Hardware Description Language

NAME: MEDEL, PAMELA AMOR V.

STUDENT NUMBER: 2120646

DATE OF SUBMISSION: DECEMBER 20, 2022

ENGR. CHARLES RAY JUANILLAS

PROFESSOR



Output Screenshot:

```
Command Prompt
                                                                                                                    Microsoft Windows [Version 10.0.19045.2364]
c) Microsoft Corporation. All rights reserved.
 :\Users\pamvm>cd..
 :\Users>cd..
:\>dir
Volume in drive C has no label.
Volume Serial Number is D865-B202
Directory of C:\
01/07/2022 03:45 pm
                        <DIR>
                                        $WINDOWS.~BT
           12:26 pm
25/09/2022
                                     30 AVScanner.ini
           01:08 pm
20/01/2022
                        <DIR>
                                        Brother
03/07/2022
                        <DIR>
            06:13 pm
                                        ESD
19/01/2022
           11:27 pm
                        <DIR>
                                        Intel
                                        iverilog
18/12/2022
           06:27 pm
                        <DIR>
                                       PerfLogs
Program Files
07/12/2019
           05:14 pm
                        <DIR>
07/11/2022
            03:29 pm
                        <DIR>
18/12/2022
           11:13 am
                        <DTR>
                                        Program Files (x86)
16/05/2022
                                       Users
            11:05 am
                        <DIR>
<DIR>
                                       Windows
                                     30 bytes
              10 Dir(s) 134,254,485,504 bytes free
C:\>cd iverilog
C:\iverilog>dir
                                                                                                                   Command Prompt
:\>cd iverilog
:\iverilog>dir
Volume in drive C has no label.
Volume Serial Number is D865-B202
Directory of C:\iverilog
18/12/2022 06:27 pm
                        <DIR>
18/12/2022
            06:27 pm
                                        bin
19/09/2022
            08:02 am
                        <DIR>
18/12/2022
            06:07 pm
                                        exercises
09/10/2022
            09:43 pm
                        <DIR>
18/12/2022
            11:41 pm
                                        Experiments
                                    gtkwave
52 Icarus Verilog.url
19/09/2022
            08:02 am
                        <DIR>
19/09/2022
            08:02 am
            04:52 pm
                                18,902 icarus.ico
25/04/2004
19/09/2022
            08:02 am
                                        include
19/09/2022
            08:02 am
09/10/2022
            08:51 pm
                                        samples
19/09/2022
            08:02 am
                        <DIR>
19/09/2022
            08:02 am
                                184,689 unins000.dat
19/09/2022
            08:01 am
                              3,153,063 unins000.exe
               4 File(s)
                               3,356,706 bytes
              11 Dir(s) 134,253,977,600 bytes free
C:\iverilog>cd Experiments
```

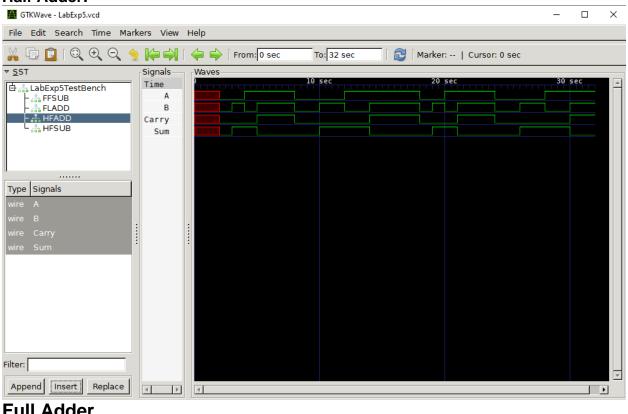


COLLEGE OF ENGINEERING & ARCHITECTURE

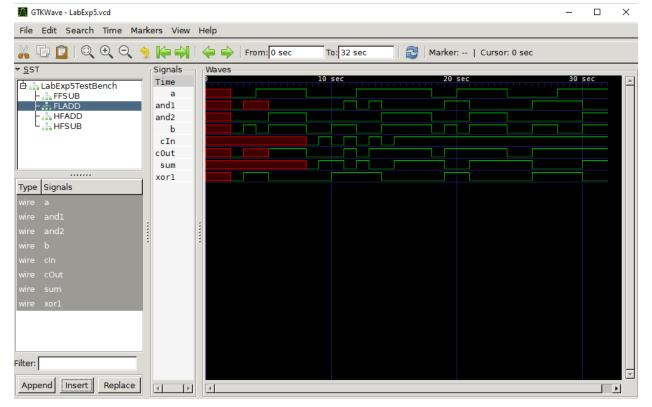
```
Command Prompt
                  11 Dir(s) 134,253,977,600 bytes free
C:\iverilog>cd Experiments
C:\iverilog\Experiments>dir
 Volume in drive C has no label.
 Volume Serial Number is D865-B202
 Directory of C:\iverilog\Experiments
18/12/2022 11:41 pm
                               <DIR>
18/12/2022
               11:41 pm
                               <DIR>
18/12/2022 06:28 pm
                                             948 Experiment1.v
18/12/2022 08:37 pm
                                           3,233 Experiment2.v
                                           3,996 Experiment3.v
18/12/2022 09:25 pm
18/12/2022 11:08 pm
                                           1,872 Experiment4.v
                                           2,580 Experiment5.v
19/12/2022 12:08 am
19/12/2022
               12:03 am
                                           2,206 Lab5CPE314.vcd
18/12/2022 07:04 pm
                                            848 LabExp1.vcd
18/12/2022 08:37 pm
                                           1,812 LabExp2.vcd
18/12/2022 09:25 pm
                                           4,510 LabExp3.vcd
18/12/2022
               11:21 pm
                                           1,217 LabExp4.vcd
19/12/2022 12:03 am
                                         12,479 test
                   11 File(s) 35,701 bytes
2 Dir(s) 134,253,977,600 bytes free
                  11 File(s)
C:\iverilog\Experiments>iverilog -o test Experiment5.v
C:\iverilog\Experiments>vvp test
VCD info: dumpfile Lab5CPE314.vcd
                                                                                                                                                   П
 Command Prompt
                                                                                                                                                           ×
Simulating Half Adder
A=0, B=0, Sum=0, Carry=0
A=0, B=1, Sum=1, Carry=0
A=1, B=0, Sum=1, Carry=0
A=1, B=1, Sum=0, Carry=1
Simulating Full Adder
A=0, B=0, cIn=0, Sum=0, Carry=0
A=0, B=0, cIn=1, Sum=1, Carry=0
A=0, B=1, cIn=0, Sum=1, Carry=0
A=0, B=1, cIn=1, Sum=0, Carry=1
A=1, B=0, cIn=0, Sum=1, Carry=0
A=1, B=0, cIn=1, Sum=0, Carry=1
A=1, B=1, cIn=0, Sum=0, Carry=1
A=1, B=1, cIn=1, Sum=1, Carry=1
Simulating Half Subtractor
A=0, B=0, Diff=0, Borrow=0
A=0, B=1, Diff=1, Borrow=1
A=1, B=0, Diff=1, Borrow=0
A=1, B=1, Diff=0, Borrow=0
Simulating Full Subtractor
A=0, B=0, bIn=0, Diff=0, Borrow=0
A=0, B=0, bIn=1, Diff=1, Borrow=1
A=0, B=1, bIn=0, Diff=1, Borrow=1
A=0, B=1, bIn=1, Diff=0, Borrow=1
A=1, B=0, bIn=0, Diff=1, Borrow=0
A=1, B=0, bIn=1, Diff=0, Borrow=0
A=1, B=1, bIn=0, Diff=0, Borrow=0
A=1, B=1, bIn=1, Diff=1, Borrow=1
Experiment5.v:117: $finish called at 32 (1s)
C:\iverilog\Experiments>
```



GTKwave: Half Adder:

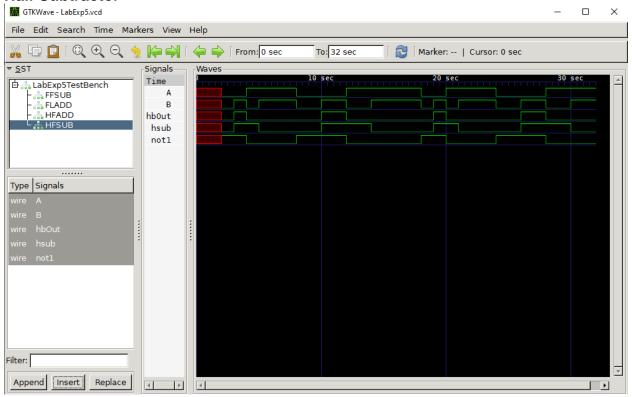


Full Adder





Half Subtractor



Full Subtractor

