University of Batangas
LIPA CITY
COLLEGE OF ENGINEERING & ARCHITECTURE

UNIVERSITY OF BATANGAS – LIPA CAMPUS
COLLEGE OF ENGINEERING AND ARCHITECTURE
COMPUTER ENGINEERING

De Morgan's Theorem and Universal Logic Gates

Experiment #2

Hardware Description Language

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PROFESSOR

Output Screenshot:

Command Prompt

```
Microsoft Windows [Version 10.0.19045.2364]
(c) Microsoft Corporation. All rights reserved.

C:\Users\pamvm>cd..

C:\Users>cd..

C:\>dir
 Volume in drive C has no label.
 Volume Serial Number is D865-B202

 Directory of C:\

01/07/2022  03:45 pm    <DIR>          $WINDOWS.~BT
25/09/2022  12:26 pm                30 AVScanner.ini
20/01/2022  01:08 pm    <DIR>          Brother
03/07/2022  06:13 pm    <DIR>          ESD
19/01/2022  11:27 pm    <DIR>          Intel
18/12/2022  06:27 pm    <DIR>          iverilog
07/12/2019  05:14 pm    <DIR>          PerfLogs
07/11/2022  03:29 pm    <DIR>          Program Files
18/12/2022  11:13 am    <DIR>          Program Files (x86)
16/05/2022  11:05 am    <DIR>          Users
15/12/2022  12:50 pm    <DIR>          Windows
               1 File(s)             30 bytes
              10 Dir(s)  135,234,678,784 bytes free

C:\>cd iverilog

C:\iverilog>dir
```

Command Prompt

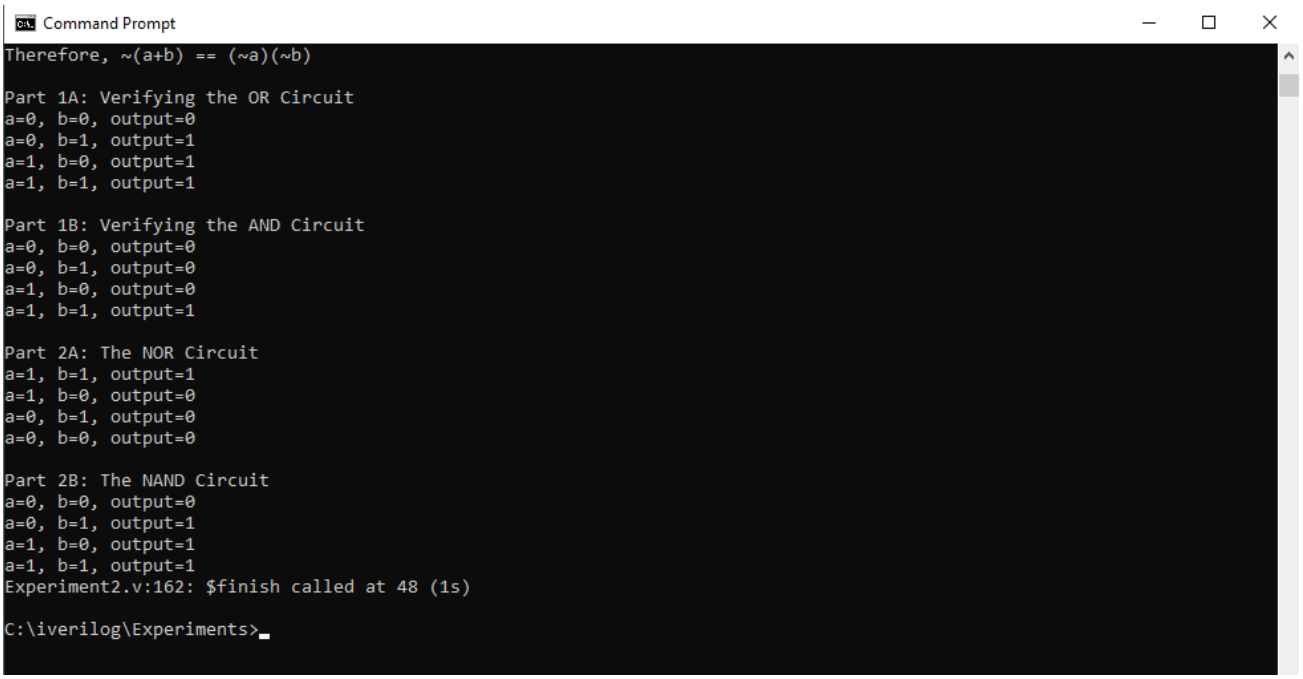
```
C:\>cd iverilog

C:\iverilog>dir
 Volume in drive C has no label.
 Volume Serial Number is D865-B202

 Directory of C:\iverilog

18/12/2022  06:27 pm    <DIR>          .
18/12/2022  06:27 pm    <DIR>          ..
19/09/2022  08:02 am    <DIR>          bin
18/12/2022  06:07 pm    <DIR>          exercises
09/10/2022  09:43 pm    <DIR>          exp
19/12/2022  09:00 pm    <DIR>          Experiments
19/09/2022  08:02 am    <DIR>          gtkwave
19/09/2022  08:02 am                52 Icarus Verilog.url
25/04/2004  04:52 pm            18,902 icarus.ico
19/09/2022  08:02 am    <DIR>          include
19/09/2022  08:02 am    <DIR>          lib
09/10/2022  08:51 pm    <DIR>          samples
19/09/2022  08:02 am    <DIR>          share
19/09/2022  08:02 am           184,689 unins000.dat
19/09/2022  08:01 am         3,153,063 unins000.exe
               4 File(s)      3,356,706 bytes
              11 Dir(s)  135,234,678,784 bytes free

C:\iverilog>cd Experiments

C:\iverilog\Experiments>
```

Command Prompt

```
C:\iverilog\Experiments>dir
 Volume in drive C has no label.
 Volume Serial Number is D865-B202

 Directory of C:\iverilog\Experiments

19/12/2022  09:00 pm    <DIR>          .
19/12/2022  09:00 pm    <DIR>          ..
19/12/2022  12:29 am             1,825 7Segment.v
19/12/2022  12:33 am             1,385 7Segment.vcd
18/12/2022  06:28 pm               948 Experiment1.v
19/12/2022  09:00 pm             3,719 Experiment2.v
18/12/2022  09:25 pm             3,996 Experiment3.v
18/12/2022  11:08 pm             1,872 Experiment4.v
19/12/2022  12:18 am             2,577 Experiment5.v
18/12/2022  07:04 pm               848 LabExp1.vcd
18/12/2022  09:25 pm             4,510 LabExp3.vcd
18/12/2022  11:21 pm             1,217 LabExp4.vcd
19/12/2022  12:18 am             2,206 LabExp5.vcd
19/12/2022  08:55 pm            14,343 test
              12 File(s)         39,446 bytes
               2 Dir(s)  135,231,193,088 bytes free

C:\iverilog\Experiments>iverilog -o test Experiment2.v

C:\iverilog\Experiments>vvp test
VCD info: dumpfile LabExp2.vcd opened for output.
```

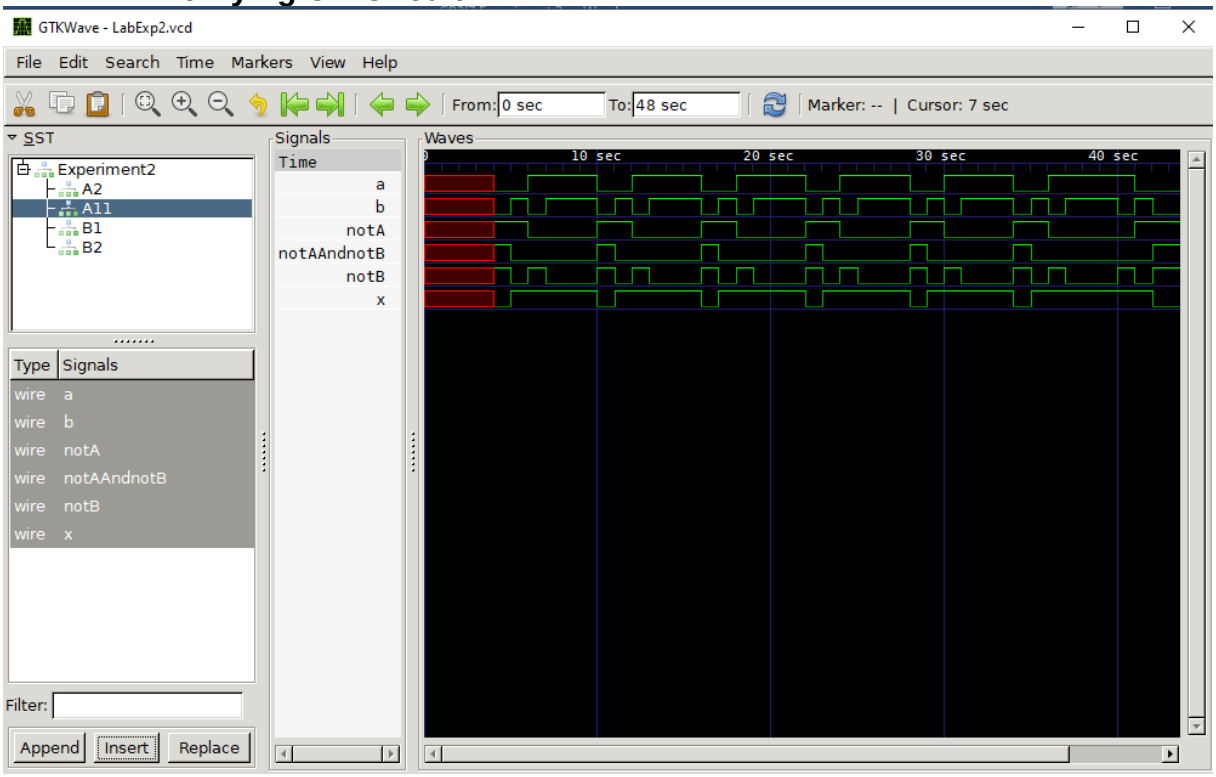
Command Prompt

```
DE MORGAN'S THEOREM

~((a)(b))
a=0, b=0, output=1
a=0, b=1, output=1
a=1, b=0, output=1
a=1, b=1, output=0

(~a)+(~b)
a=0, b=0, output=1
a=0, b=1, output=1
a=1, b=0, output=1
a=1, b=1, output=0
Therefore, ~((a)(b)) == (~a)+(~b)

~(a+b)
a=0, b=0, output=1
a=0, b=1, output=0
a=1, b=0, output=0
a=1, b=1, output=0

(~a)(~b)
a=0, b=0, output=1
a=0, b=1, output=0
a=1, b=0, output=0
a=1, b=1, output=0
Therefore, ~(a+b) == (~a)(~b)
```

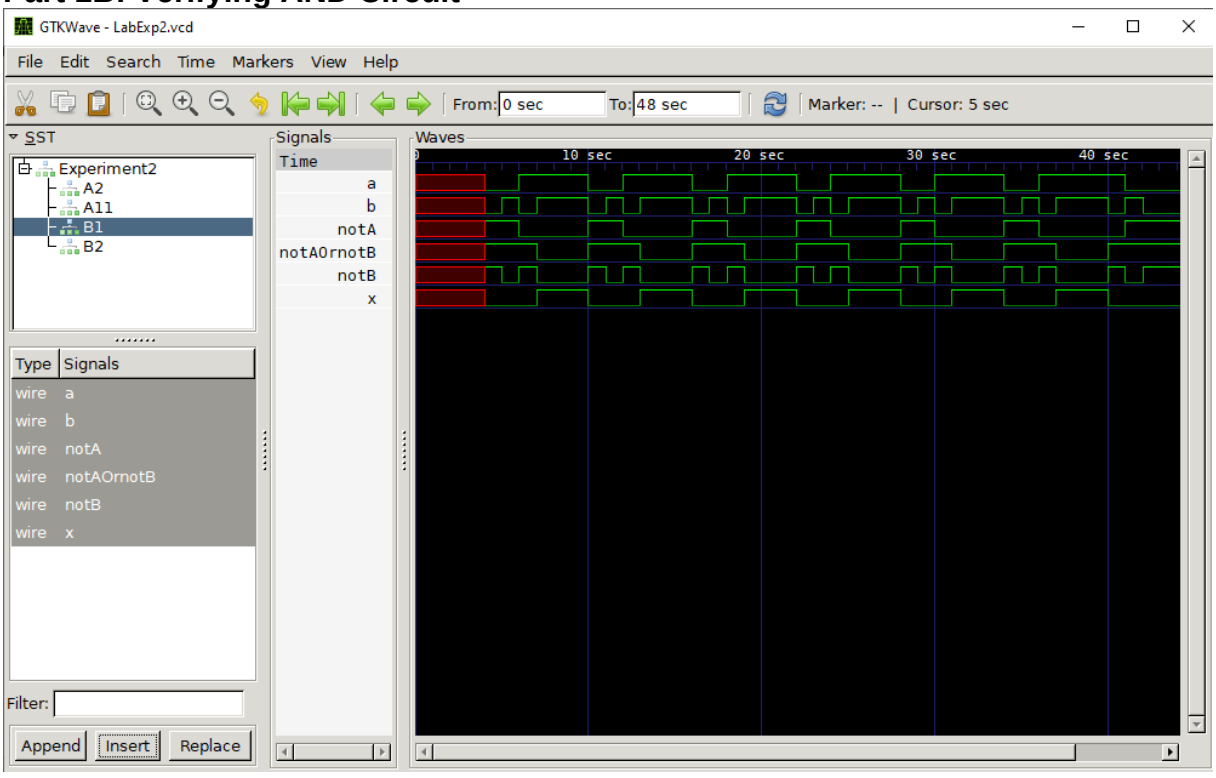

Command Prompt
Therefore, ~(a+b) == (~a)(~b)
Part 1A: Verifying the OR Circuit
a=0, b=0, output=0
a=0, b=1, output=1
a=1, b=0, output=1
a=1, b=1, output=1
Part 1B: Verifying the AND Circuit
a=0, b=0, output=0
a=0, b=1, output=0
a=1, b=0, output=0
a=1, b=1, output=1
Part 2A: The NOR Circuit
a=1, b=1, output=1
a=1, b=0, output=0
a=0, b=1, output=0
a=0, b=0, output=0
Part 2B: The NAND Circuit
a=0, b=0, output=0
a=0, b=1, output=1
a=1, b=0, output=1
a=1, b=1, output=1
Experiment2.v:162: $finish called at 48 (1s)
C:\iverilog\Experiments>

GTKwave:

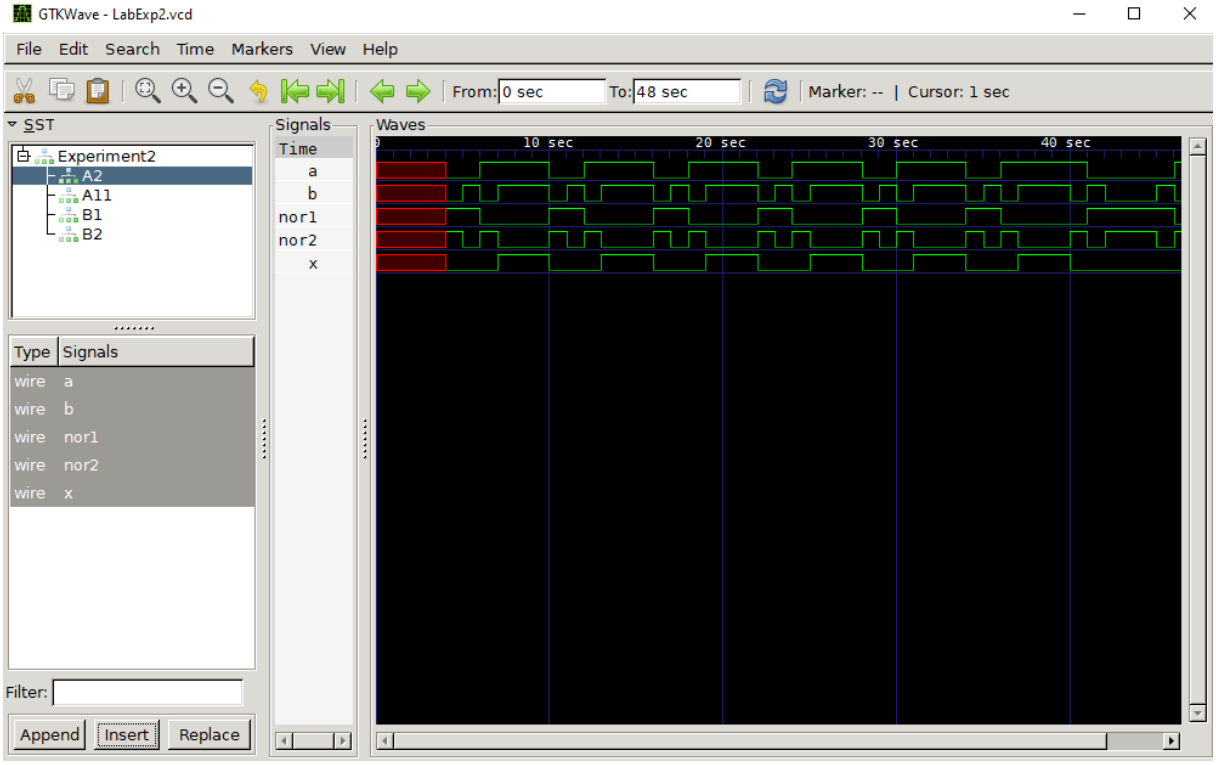
PART 1A: Verifying OR Circuit



Part 1B: Verifying AND Circuit



Part 2A: The NOR Circuit



Part 2B: The NAND Circuit