



**University of  
Batangas**  
LIPA CITY  
COLLEGE OF ENGINEERING  
& ARCHITECTURE

**UNIVERSITY OF BATANGAS – LIPA CAMPUS  
COLLEGE OF ENGINEERING AND ARCHITECTURE  
COMPUTER ENGINEERING**

Combinational Logic Circuits

**Experiment #4**  
Hardware Description Language

NAME: MEDEL, PAMELA AMOR V.

STUDENT NUMBER: 2120646

DATE OF SUBMISSION: DECEMBER 20, 2022

ENGR. CHARLES RAY JUANILLAS

---

PROFESSOR



## Output Screenshot:

```
Command Prompt
Microsoft Windows [Version 10.0.19045.2364]
(c) Microsoft Corporation. All rights reserved.

C:\Users\pamvm>cd..

C:\Users>cd..

C:\>dir
Volume in drive C has no label.
Volume Serial Number is D865-B202

Directory of C:\

01/07/2022  03:45 pm  <DIR>          $WINDOWS.~BT
25/09/2022  12:26 pm                30 AVScanner.ini
20/01/2022  01:08 pm  <DIR>          Brother
03/07/2022  06:13 pm  <DIR>          ESD
19/01/2022  11:27 pm  <DIR>          Intel
18/12/2022  06:27 pm  <DIR>          iverilog
07/12/2019  05:14 pm  <DIR>          PerfLogs
07/11/2022  03:29 pm  <DIR>          Program Files
18/12/2022  11:13 am  <DIR>          Program Files (x86)
16/05/2022  11:05 am  <DIR>          Users
15/12/2022  12:50 pm  <DIR>          Windows
                1 File(s)                30 bytes
                10 Dir(s)  134,518,616,064 bytes free

C:\>cd iverilog
```

```
Command Prompt
15/12/2022  12:50 pm  <DIR>          Windows
                1 File(s)                30 bytes
                10 Dir(s)  134,518,616,064 bytes free

C:\>cd iverilog

C:\iverilog>dir
Volume in drive C has no label.
Volume Serial Number is D865-B202

Directory of C:\iverilog

18/12/2022  06:27 pm  <DIR>          .
18/12/2022  06:27 pm  <DIR>          ..
19/09/2022  08:02 am  <DIR>          bin
18/12/2022  06:07 pm  <DIR>          exercises
09/10/2022  09:43 pm  <DIR>          exp
18/12/2022  10:35 pm  <DIR>          Experiments
19/09/2022  08:02 am  <DIR>          gtkwave
19/09/2022  08:02 am                52 Icarus Verilog.url
25/04/2004  04:52 pm            18,902 icarus.ico
19/09/2022  08:02 am  <DIR>          include
19/09/2022  08:02 am  <DIR>          lib
09/10/2022  08:51 pm  <DIR>          samples
19/09/2022  08:02 am  <DIR>          share
19/09/2022  08:02 am            184,689 unins000.dat
19/09/2022  08:01 am            3,153,063 unins000.exe
                4 File(s)            3,356,706 bytes
                11 Dir(s)  134,517,977,088 bytes free

C:\iverilog>cd Experiments
```



```
Command Prompt
C:\iverilog>cd Experiments

C:\iverilog\Experiments>dir
Volume in drive C has no label.
Volume Serial Number is D865-B202

Directory of C:\iverilog\Experiments

18/12/2022  10:35 pm    <DIR>          .
18/12/2022  10:35 pm    <DIR>          ..
18/12/2022  06:28 pm             948 Experiment1.v
18/12/2022  08:37 pm           3,233 Experiment2.v
18/12/2022  09:25 pm           3,996 Experiment3.v
18/12/2022  11:08 pm           1,872 Experiment4.v
18/12/2022  07:04 pm             848 LabExp1.vcd
18/12/2022  08:37 pm           1,812 LabExp2.vcd
18/12/2022  09:25 pm           4,510 LabExp3.vcd
18/12/2022  11:04 pm           1,217 LabExp4.vcd
18/12/2022  11:04 pm          14,146 test
                9 File(s)          32,582 bytes
                2 Dir(s)  134,517,977,088 bytes free

C:\iverilog\Experiments>iverilog -o test Experiment4.v

C:\iverilog\Experiments>vvp test
VCD info: dumpfile LabExp4.vcd opened for output.

Command Prompt

Circuit 1: A!B + !AB
a=0, b=0 : F=0
a=0, b=1 : F=1
a=1, b=0 : F=1
a=1, b=1 : F=0

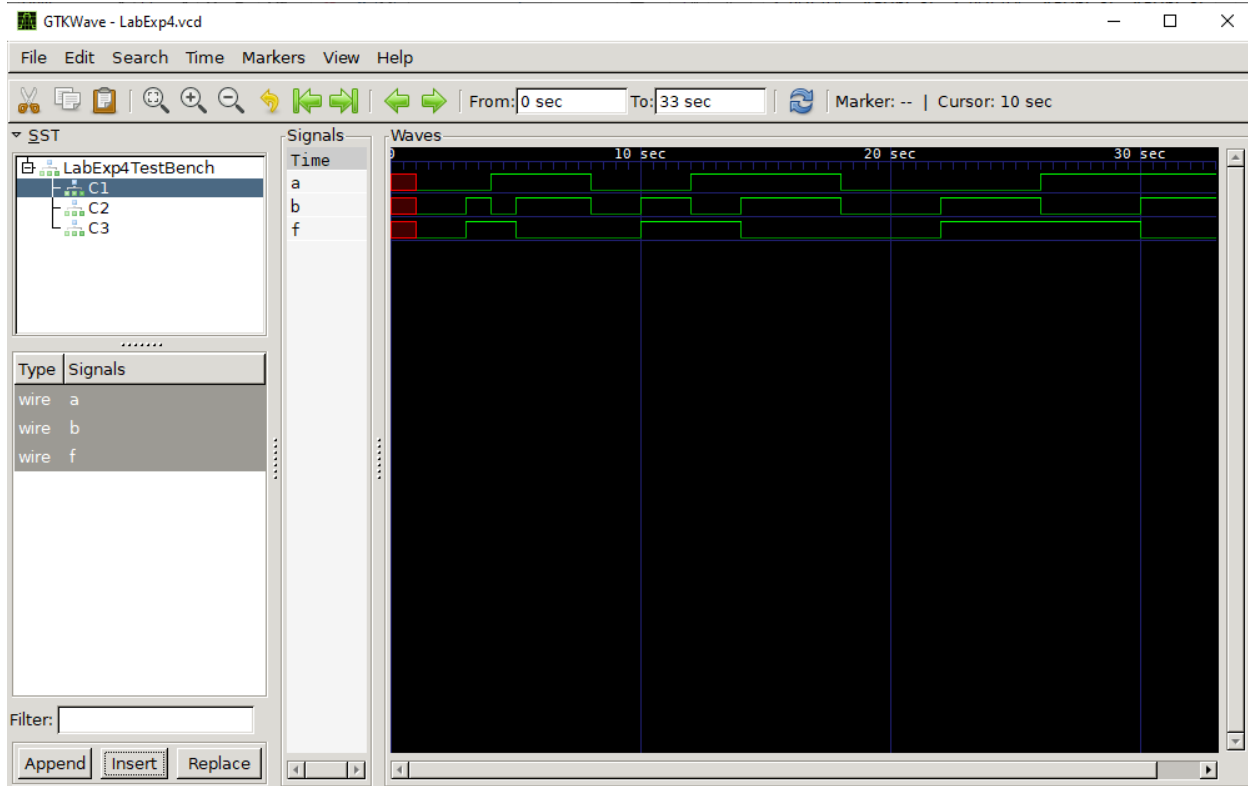
Circuit 2: AC + B!C + AB
a=0, b=0, c=0 : F=0
a=0, b=0, c=1 : F=0
a=0, b=1, c=0 : F=1
a=0, b=1, c=1 : F=0
a=1, b=0, c=0 : F=0
a=1, b=0, c=1 : F=1
a=1, b=1, c=0 : F=1
a=1, b=1, c=1 : F=1

Circuit 3: !((ABC) + !(C+D)) + (B!(C+D))
a=0, b=0, c=0, d=0 : F=0
a=0, b=0, c=0, d=1 : F=1
a=0, b=0, c=1, d=0 : F=1
a=0, b=0, c=1, d=1 : F=1
a=0, b=1, c=0, d=0 : F=1
a=0, b=1, c=0, d=1 : F=1
a=0, b=1, c=1, d=0 : F=1
a=0, b=1, c=1, d=1 : F=1
a=1, b=0, c=0, d=0 : F=0
a=1, b=0, c=0, d=1 : F=1
a=1, b=0, c=1, d=0 : F=1
a=1, b=0, c=1, d=1 : F=1
a=1, b=1, c=0, d=0 : F=1
a=1, b=1, c=0, d=1 : F=1
a=1, b=1, c=1, d=0 : F=0
a=1, b=1, c=1, d=1 : F=0

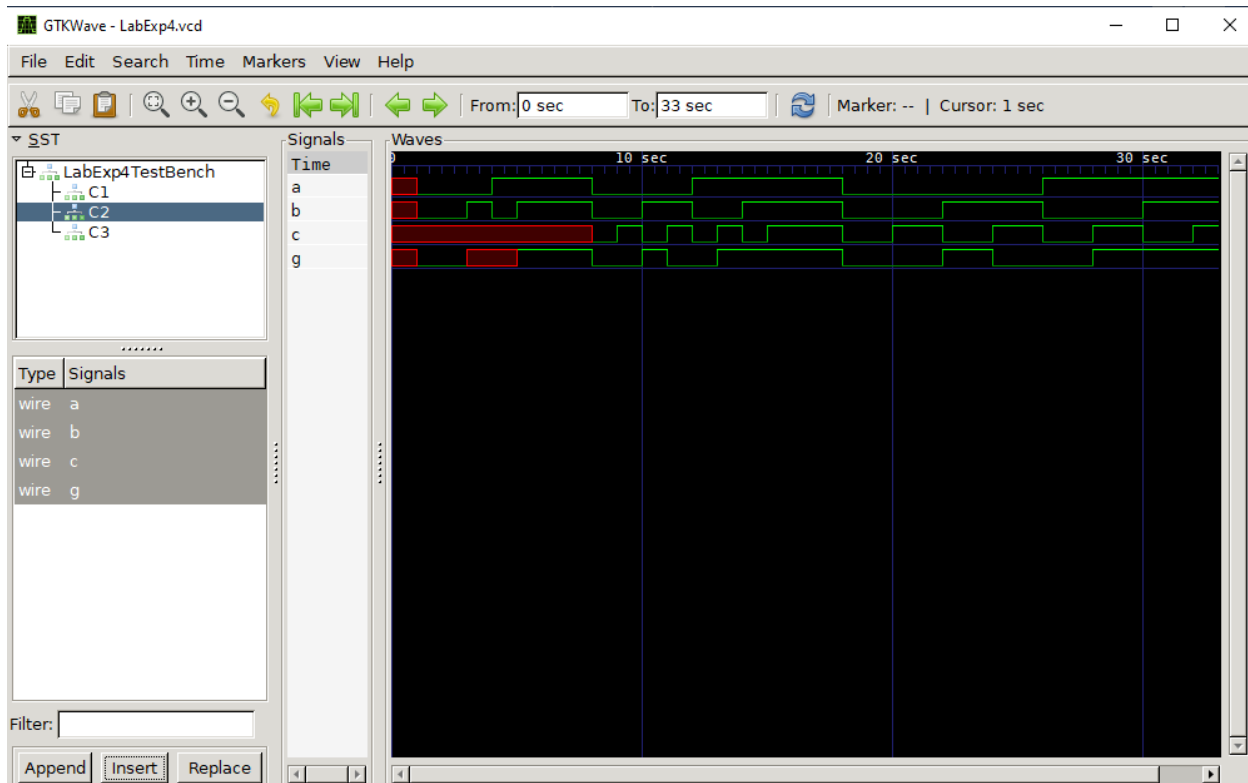
C:\iverilog\Experiments>
```



## GTKwave: Circuit 1:



## Circuit 2:





## Circuit 3:

