University of Batangas
LIPA CITY
COLLEGE OF ENGINEERING & ARCHITECTURE

UNIVERSITY OF BATANGAS – LIPA CAMPUS

COLLEGE OF ENGINEERING AND ARCHITECTURE

COMPUTER ENGINEERING

Combinational Logic Circuits

Experiment #4

Hardware Description Language

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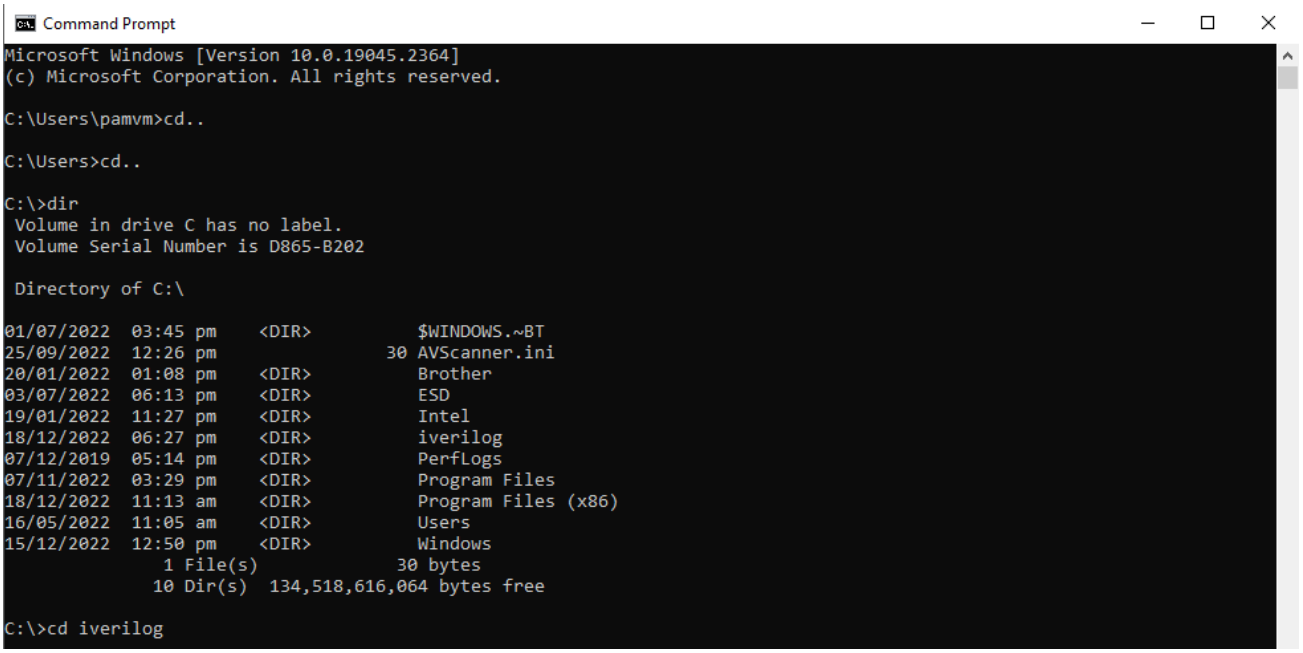
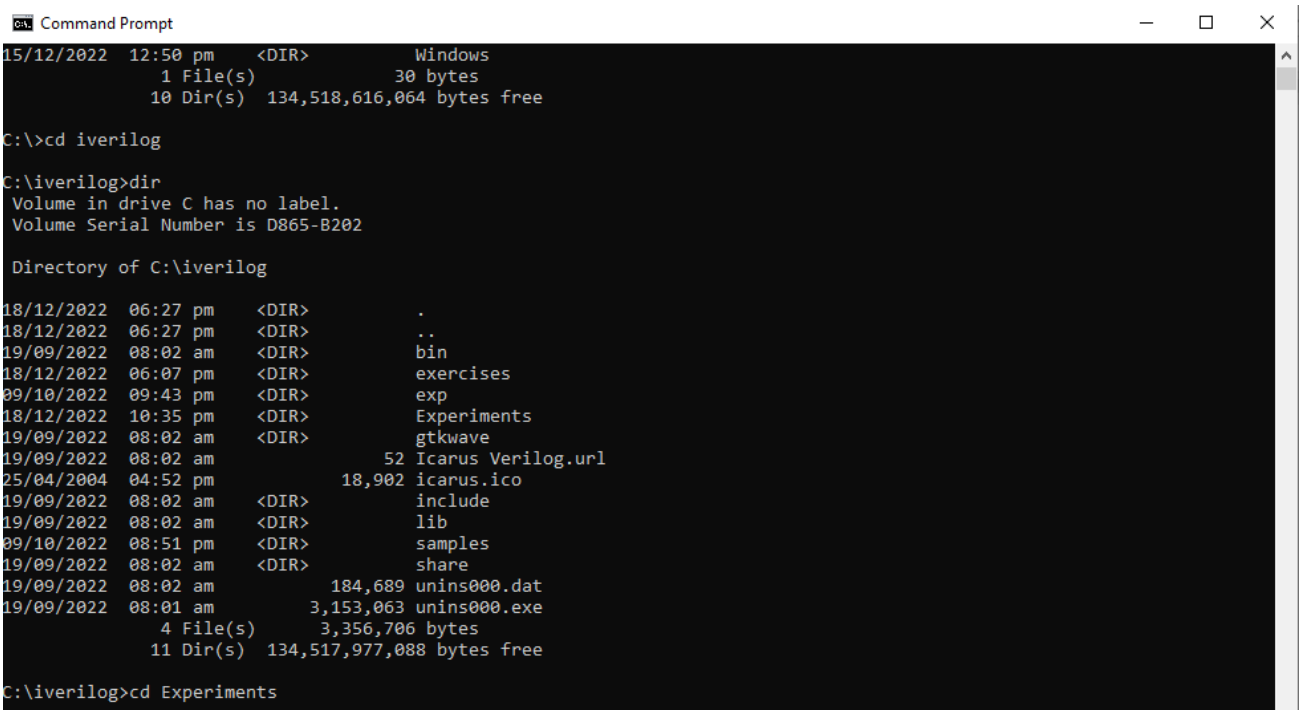
PROFESSOR

Output Screenshot:





Command Prompt

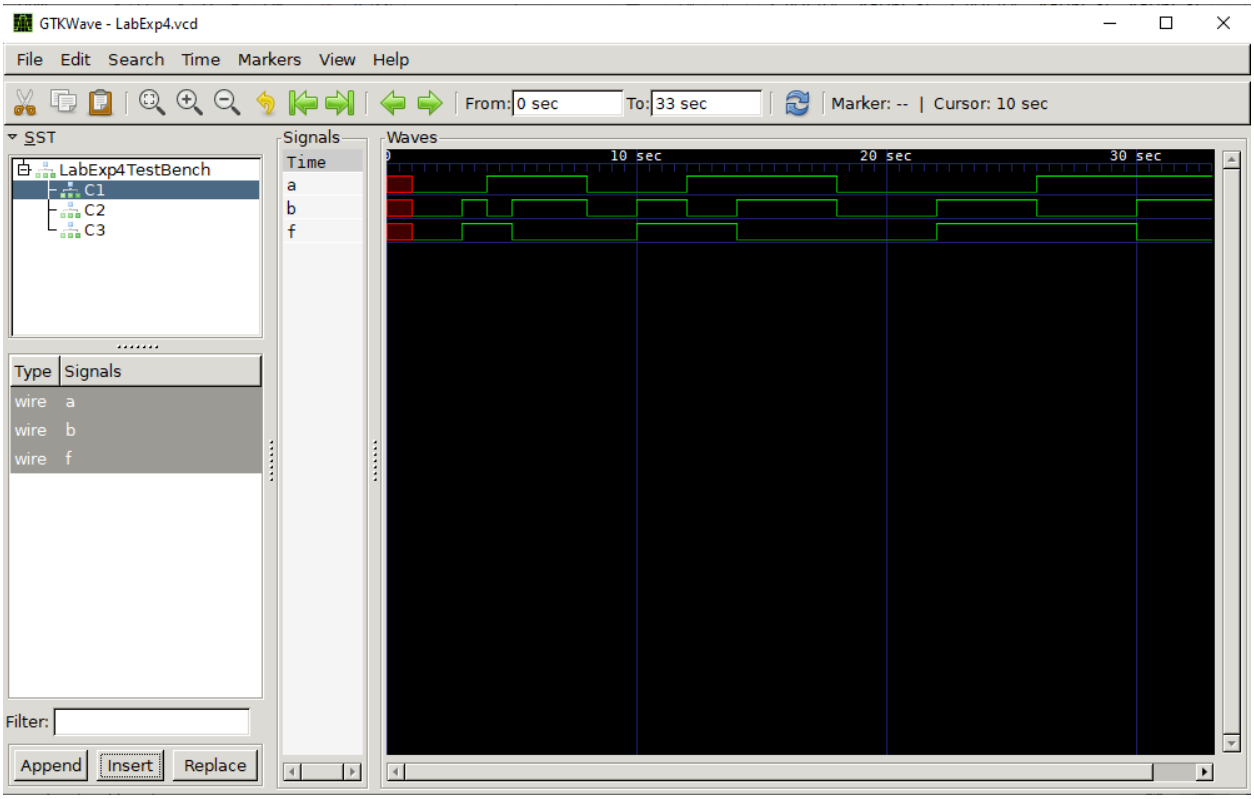
```
C:\iverilog>cd Experiments

C:\iverilog\Experiments>dir
 Volume in drive C has no label.
 Volume Serial Number is D865-B202

 Directory of C:\iverilog\Experiments

18/12/2022  10:35 pm    <DIR>          .
18/12/2022  10:35 pm    <DIR>          ..
18/12/2022  06:28 pm               948 Experiment1.v
18/12/2022  08:37 pm             3,233 Experiment2.v
18/12/2022  09:25 pm             3,996 Experiment3.v
18/12/2022  11:08 pm             1,872 Experiment4.v
18/12/2022  07:04 pm               848 LabExp1.vcd
18/12/2022  08:37 pm             1,812 LabExp2.vcd
18/12/2022  09:25 pm             4,510 LabExp3.vcd
18/12/2022  11:04 pm             1,217 LabExp4.vcd
18/12/2022  11:04 pm            14,146 test
               9 File(s)         32,582 bytes
               2 Dir(s)  134,517,977,088 bytes free

C:\iverilog\Experiments>iverilog -o test Experiment4.v

C:\iverilog\Experiments>vvp test
VCD info: dumpfile LabExp4.vcd opened for output.
```

Command Prompt

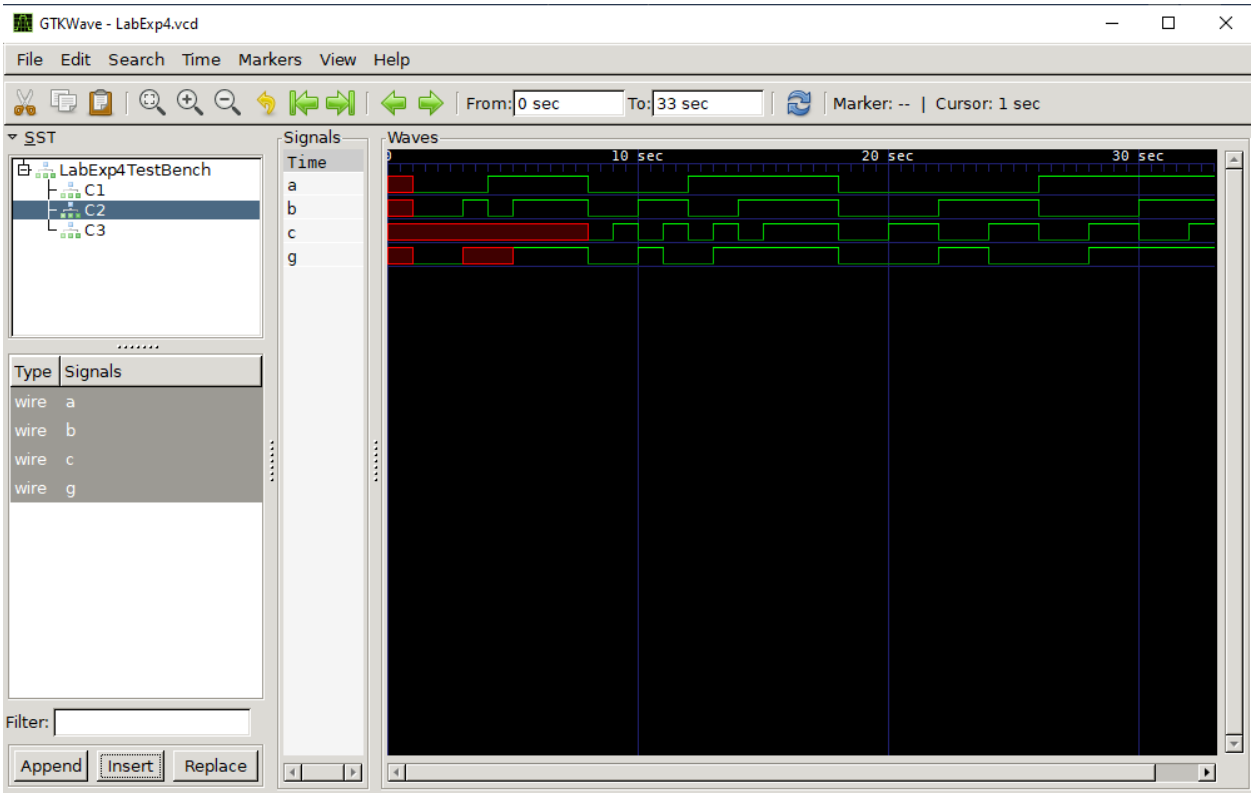
```
Circuit 1: A!B + !AB
a=0, b=0 : F=0
a=0, b=1 : F=1
a=1, b=0 : F=1
a=1, b=1 : F=0

Circuit 2: AC + B!C + AB
a=0, b=0, c=0 : F=0
a=0, b=0, c=1 : F=0
a=0, b=1, c=0 : F=1
a=0, b=1, c=1 : F=0
a=1, b=0, c=0 : F=0
a=1, b=0, c=1 : F=1
a=1, b=1, c=0 : F=1
a=1, b=1, c=1 : F=1

Circuit 3: !((ABC) + !(C+D)) + (B!(C+D))
a=0, b=0, c=0, d=0 : F=0
a=0, b=0, c=0, d=1 : F=1
a=0, b=0, c=1, d=0 : F=1
a=0, b=0, c=1, d=1 : F=1
a=0, b=1, c=0, d=0 : F=1
a=0, b=1, c=0, d=1 : F=1
a=0, b=1, c=1, d=0 : F=1
a=0, b=1, c=1, d=1 : F=1
a=1, b=0, c=0, d=0 : F=0
a=1, b=0, c=0, d=1 : F=1
a=1, b=0, c=1, d=0 : F=1
a=1, b=0, c=1, d=1 : F=1
a=1, b=1, c=0, d=0 : F=1
a=1, b=1, c=0, d=1 : F=1
a=1, b=1, c=1, d=0 : F=0
a=1, b=1, c=1, d=1 : F=0

C:\iverilog\Experiments>
```

GTKwave:

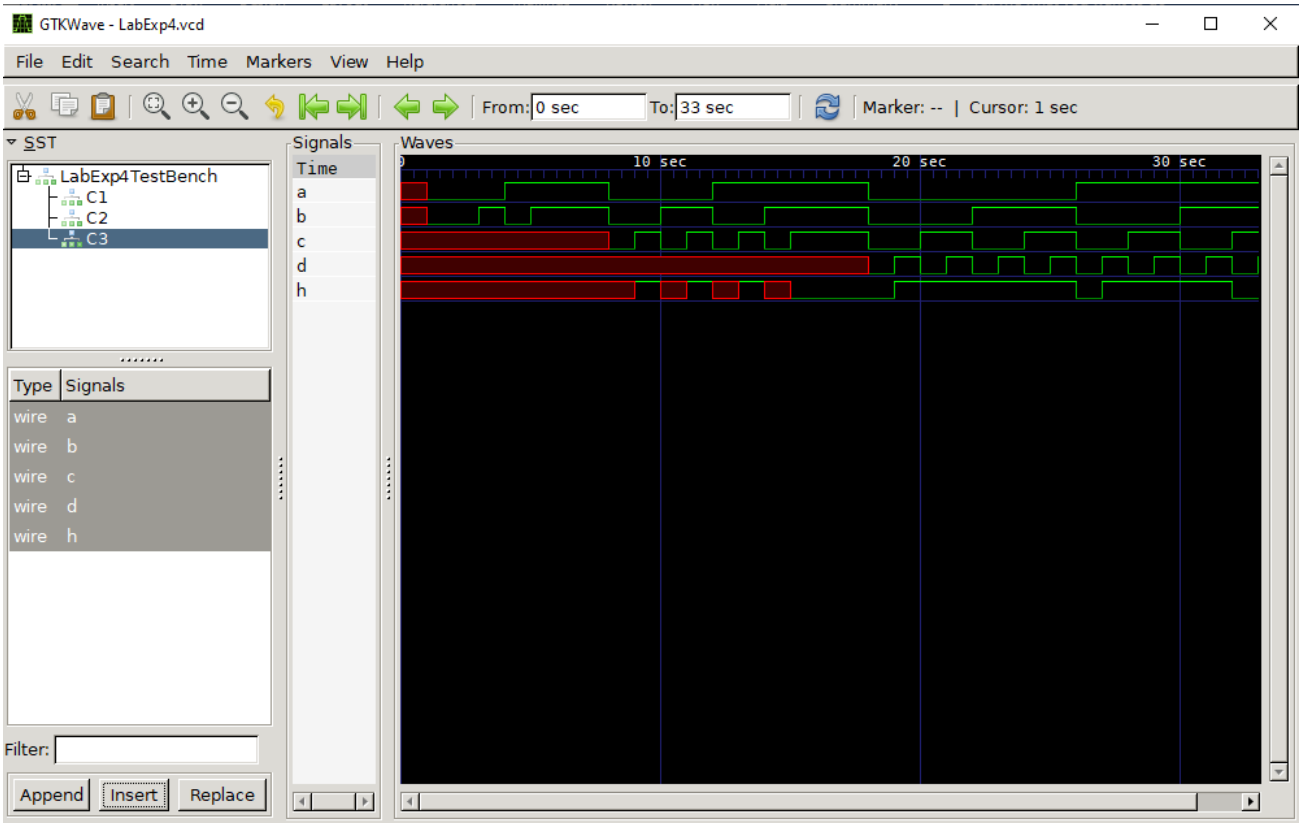
Circuit 1:



Circuit 2:



Circuit 3:


GTKWave - LabExp4.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 33 sec
Marker: -- | Cursor: 1 sec
SST
LabExp4TestBench
C1
C2
C3
Type Signals
wire a
wire b
wire c
wire d
wire h
Filter:
Append Insert Replace
Signals
Time
a
b
c
d
h
Waves
10 sec
20 sec
30 sec