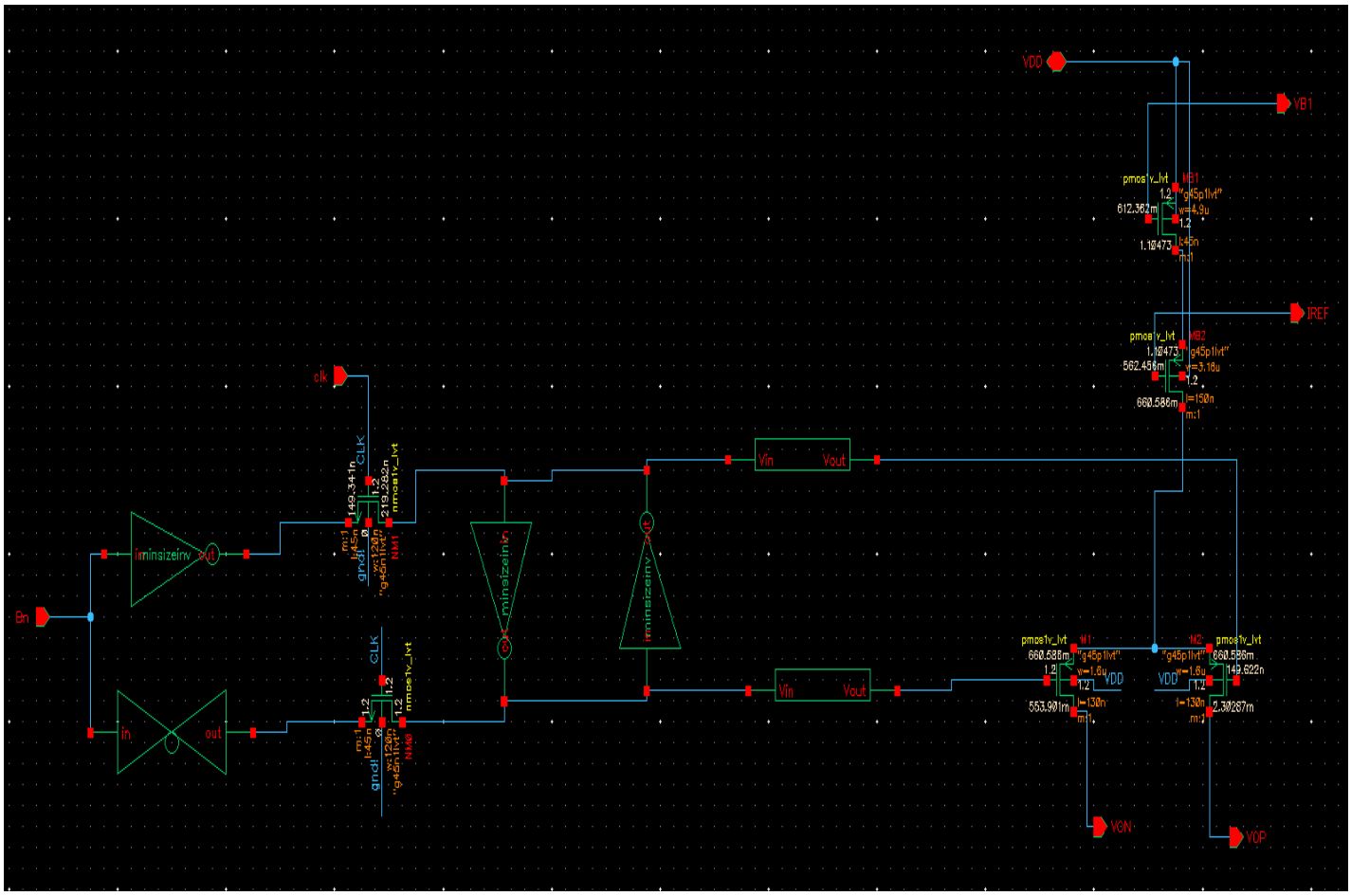
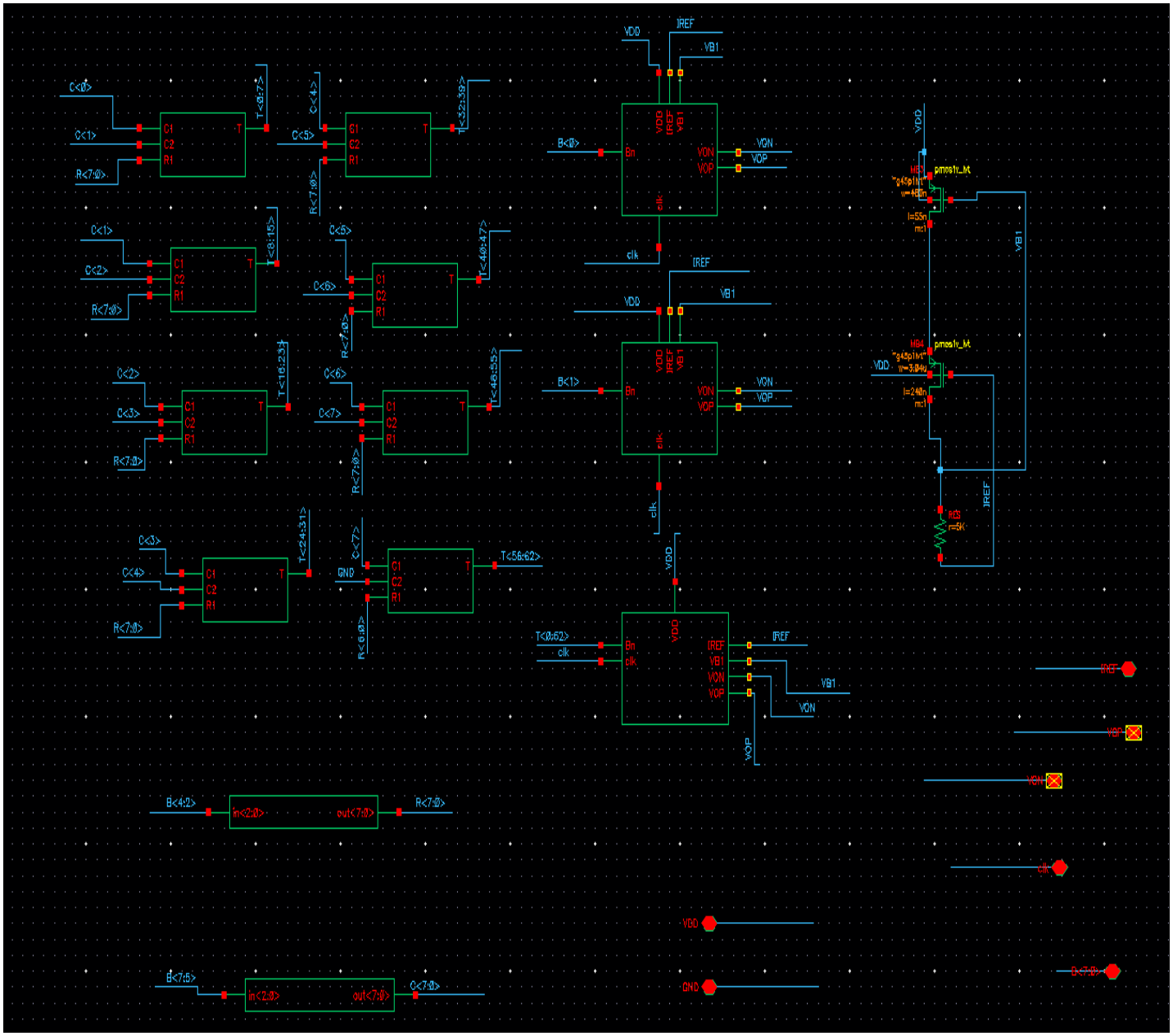
MIXED SIGNAL VLSI DESIGN (EE719)
VENKATESWAR REDDY MURIKINATI (213070088)
PART-3

3A)

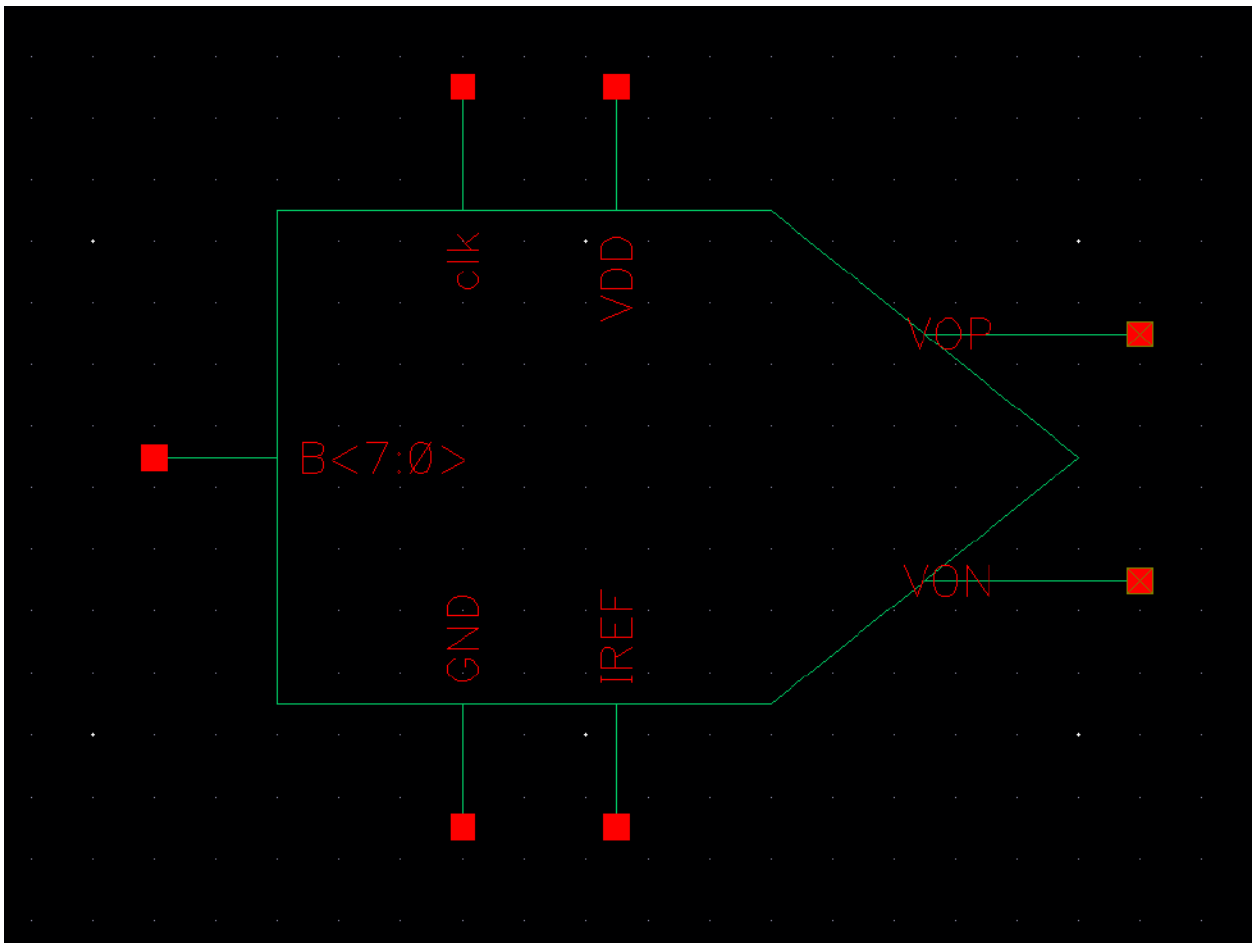
UNIT CELL_1x



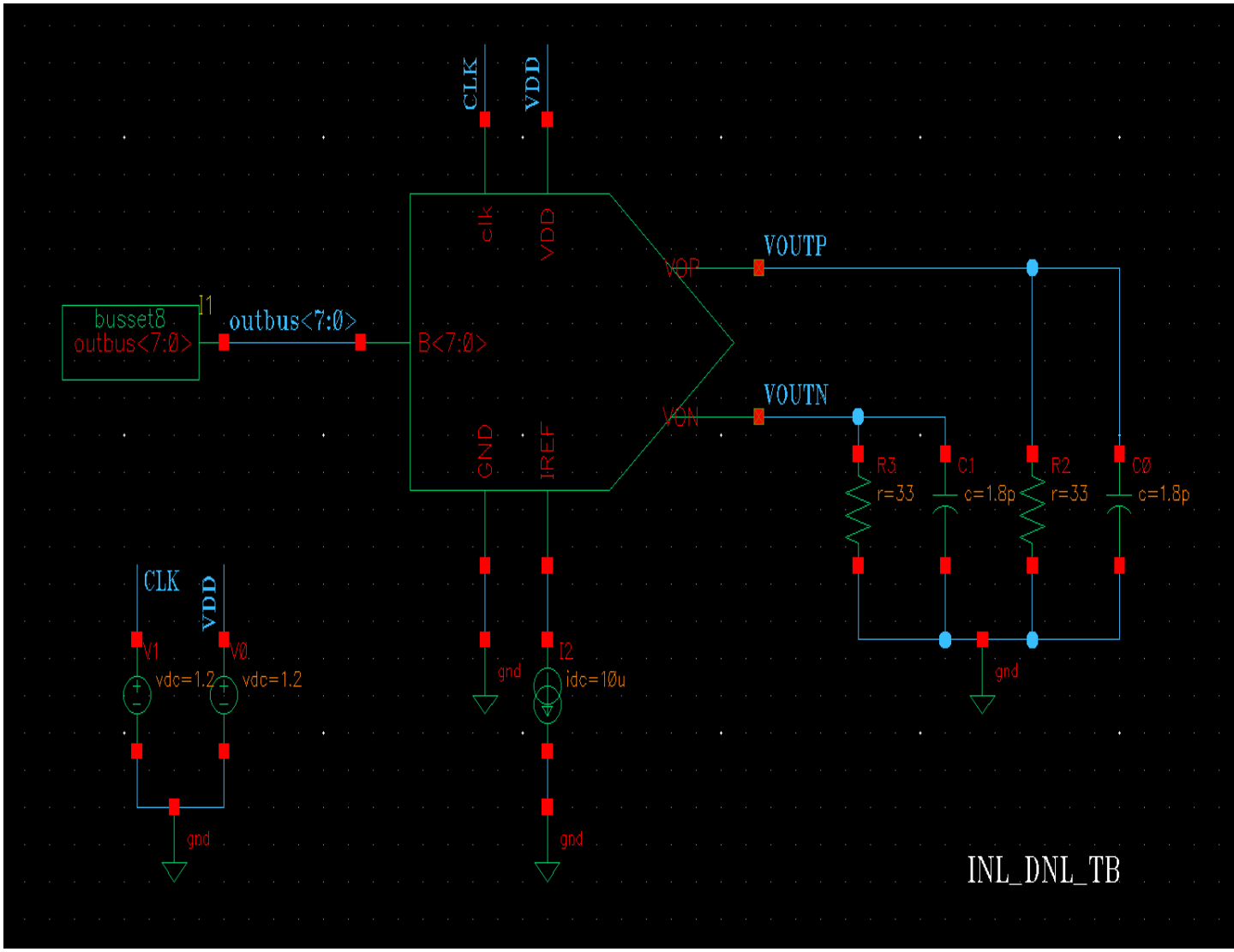
DAC:


VDD
IREF
VB1
C<0>
C<1>
R<7:0>
T<0:7>
C<4>
C<5>
T<32:39>
B<0>
Bn
VON
VOP
clk
pmos1v_lvt
C<2>
C<3>
T<8:15>
C<6>
T<40:47>
B<1>
T<16:23>
T<46:55>
C<7>
T<24:31>
GND
T<56:62>
T<0:52>
B<4:2>
in<2:0>
out<7:0>
B<7:5>
D<7:0>
RES
r=5K

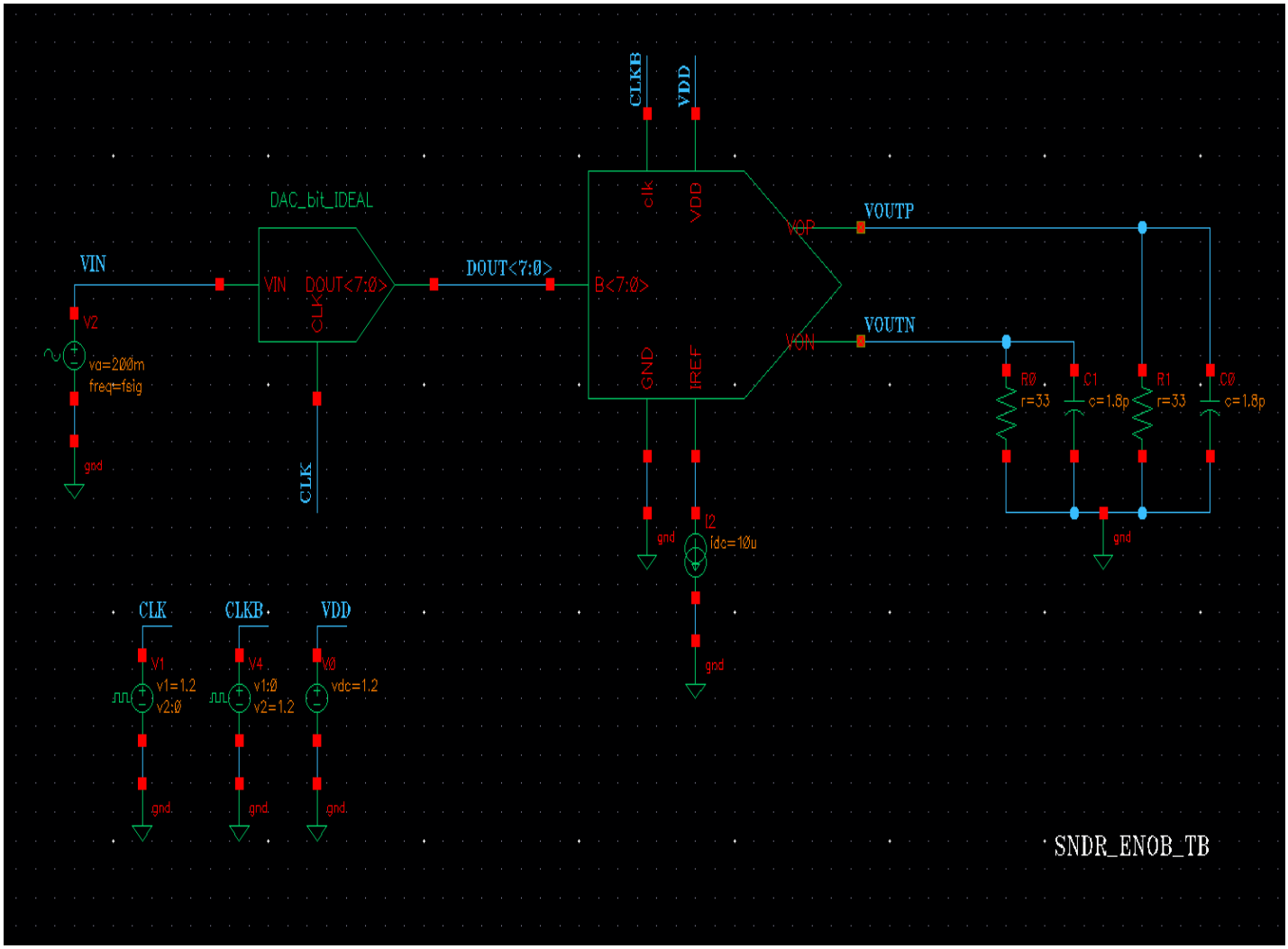
DAC_DUT:



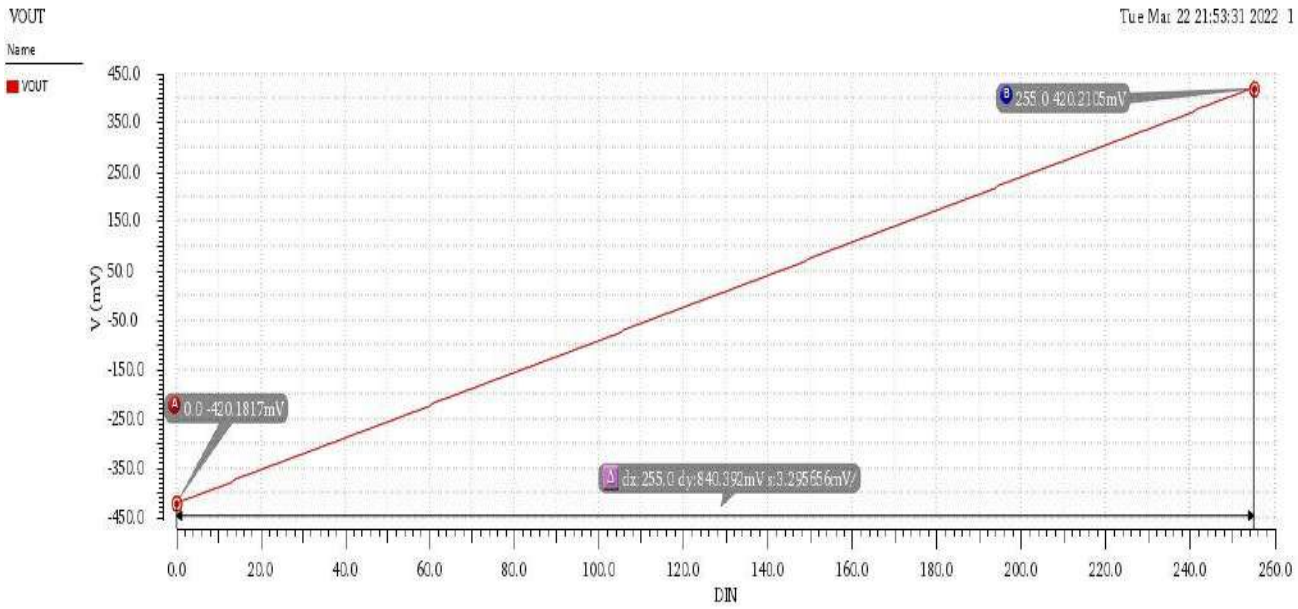
Test Setup for DC Simulations:



Test Setup for AC simulations:



3B)


VOUT
Tue Mar 22 21:53:31 2022 1
Name
VOUT
450.0
350.0
250.0
150.0
50.0
-50.0
-150.0
-250.0
-350.0
-450.0
V (mV)
255.0 420.2105mV
0.0 -420.1817mV
dx: 255.0 dy:840.392mV s:3.295556mV/
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
DIN

From the above differential output plot,we got minimum voltage as Vmin=-420.1817mV at DIN=0 and Vmax =+420.2105mV at DIN=255
And we have take VFS(differential peak-to-peak)=840mV
So Vmin_ideal=-0.5*VFS=-420mV and Vmax_ideal=+0.5*VFS=420mv
VLSB=(840mV)/255=3.2941mV

Offset=Vmin-Vmin_ideal=-420.1817mV-(-420mV)=-0.1817mV
Offset(in LSB)=-0.1817/3.2941=-0.05515LSB

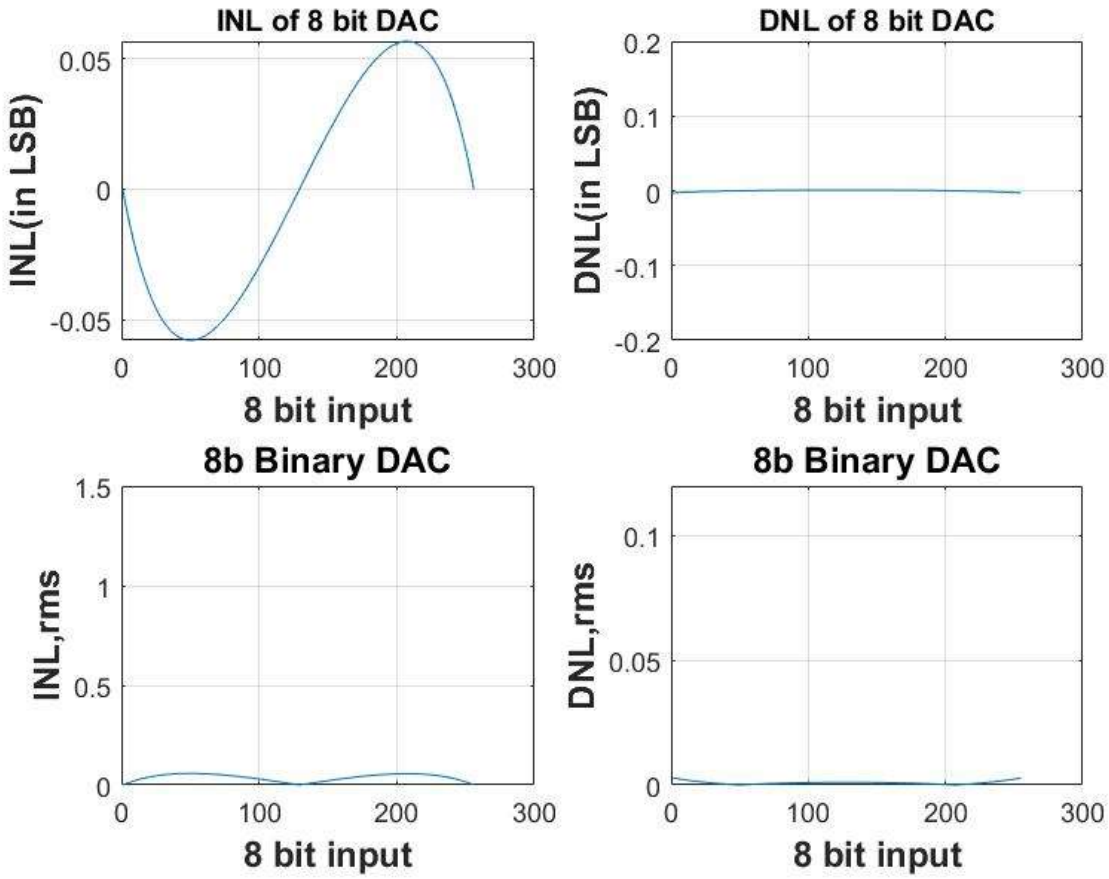
Full Scale Error=Vmax-Vmax_ideal=420.2105mV-420mV=+0.2105mV
Full Scale Error (in LSB)=0.2105/3.2941=0.0639LSB

Gain error is the difference at the full scale value between the ideal and actual when offset has been reduced to zero.So we subtract the offset value from all data points.

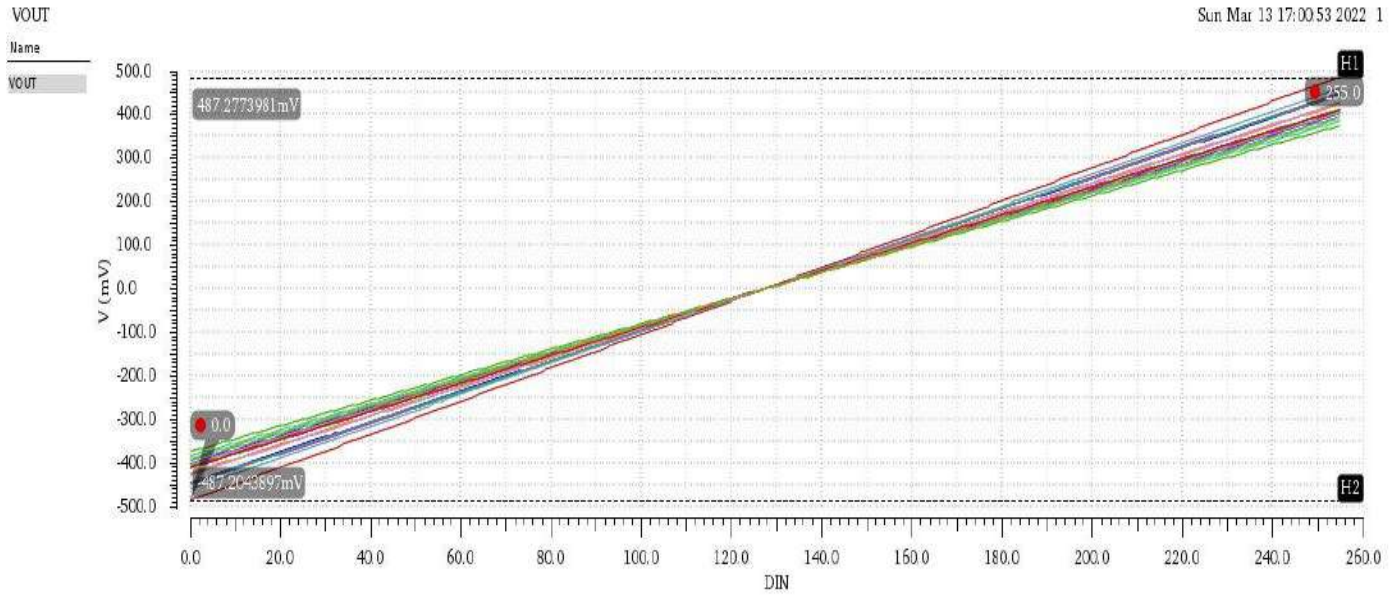
Gain Error=((Vout @DIN=255)-(Vout @DIN=0))/VLSB - 255
=(420.2105mV-Voffset)-((-420.1817mV-Voffset))/3.2941mV - 255
=0.329

Offset(in LSB)	-0.05515
Full Scale Error(in LSB)	0.0639
Gain Error(in LSB)	0.329

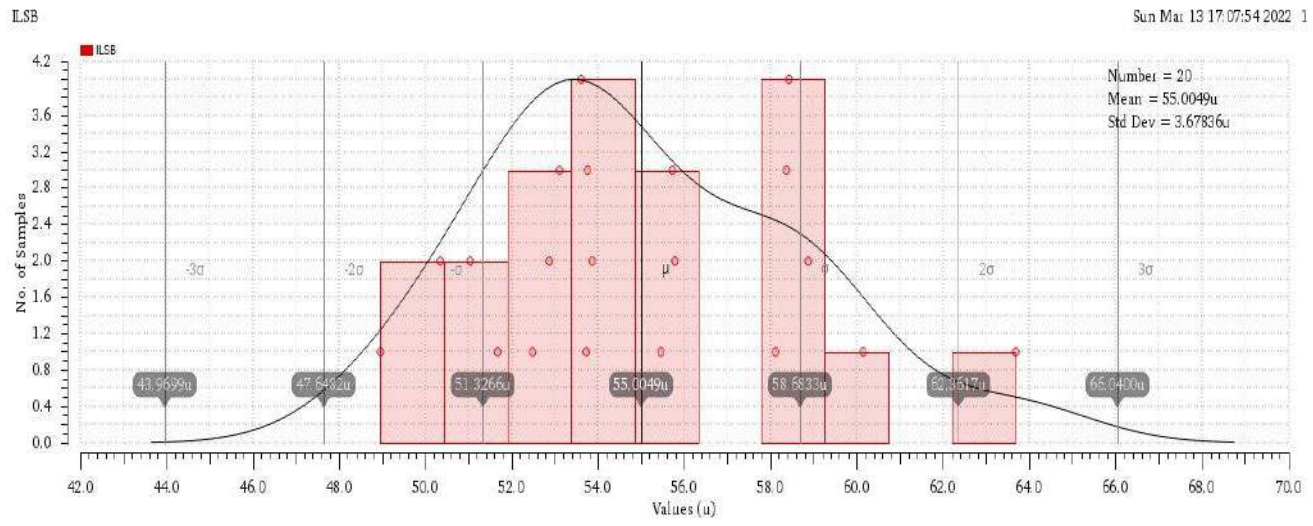
From MATLAB,


INL of 8 bit DAC
INL(in LSB)
0.05
0
-0.05
0
100
200
300
8 bit input
DNL of 8 bit DAC
DNL(in LSB)
0.2
0.1
0
-0.1
-0.2
0
100
200
300
8 bit input
8b Binary DAC
INL,rms
1.5
1
0.5
0
0
100
200
300
8 bit input
8b Binary DAC
DNL,rms
0.1
0.05
0
0
100
200
300
8 bit input

3C) I have performed the Monte Carlo simulations for 20 samples.

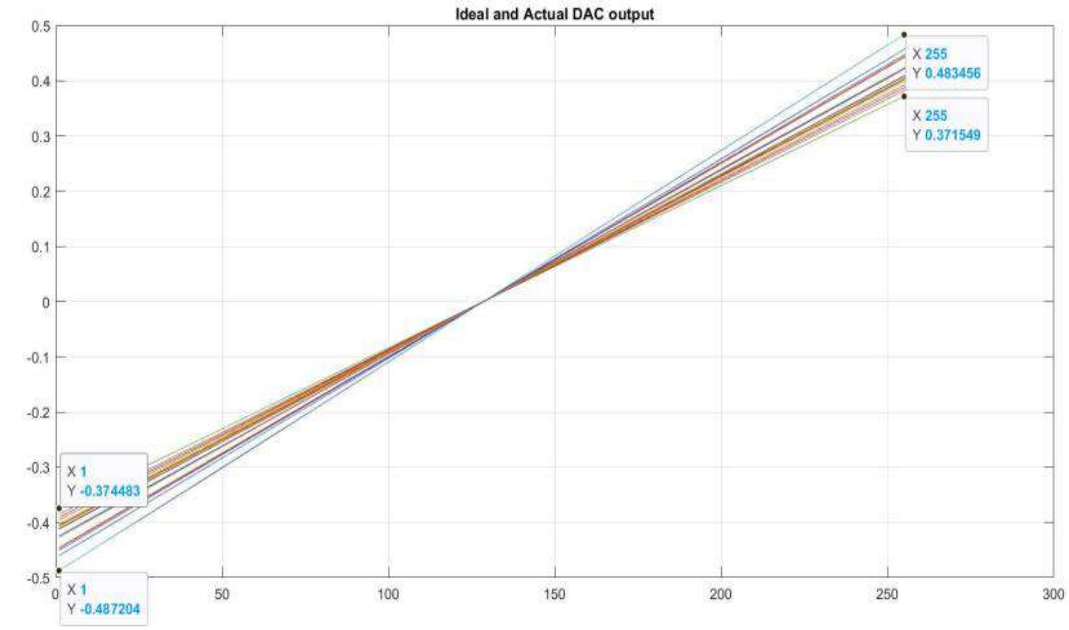


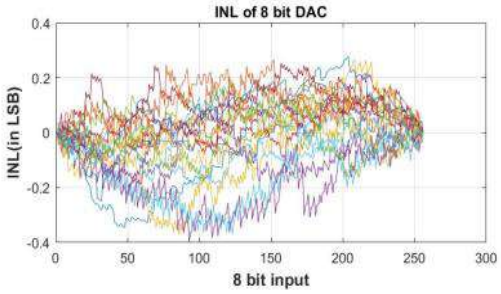
From the above,we got that maximum and minimum voltages are +487.27mV and –487.204mV ,and of the designed specifications are of +420mV and –420mV.

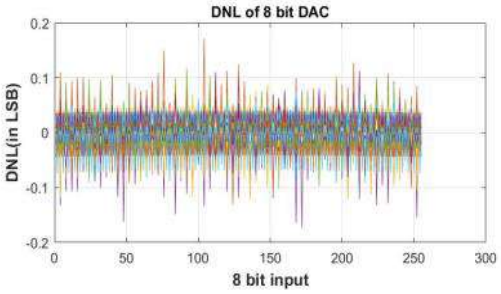


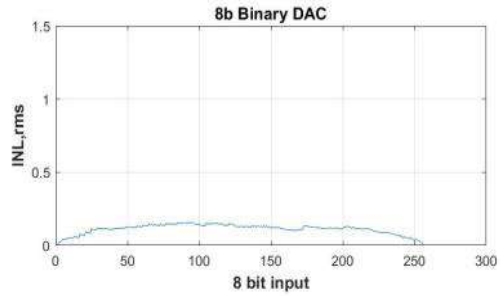
From the above histogram,we got that ILSB has a mean=55.0049uA and a standard deviation=3.6783uA.

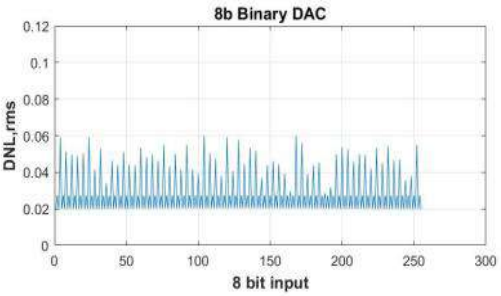
And from MATLAB,we got

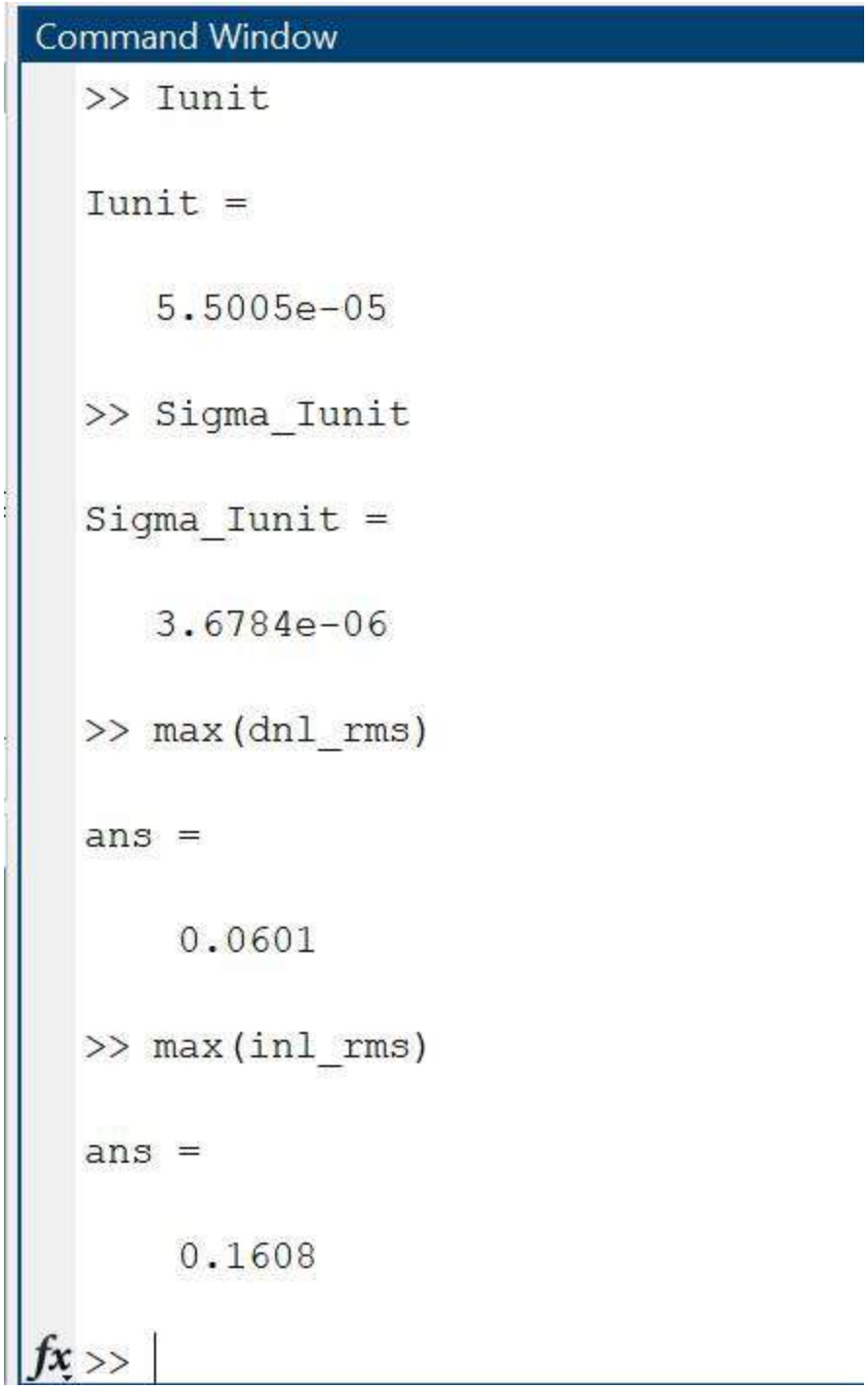












From the above Command window, we got DNL_RMS|max=0.0601 and INL_RMS|max=0.1608 and also Sigma=3.6784*e-6.
Observe that both DNL and INL specification is met.
desired.

From command window, $\sigma_I = 3.67836\mu$

and Mean $I_{LSB} = 55.0049\mu$

$\therefore \sigma_u = 0.06687$

Segmented DAC, we have taken as $B_5 = 2$ & $B_t = 6$ bits

also $\sigma_{DNL} = 2^{(B_5+1)/2} \sigma_u$

$\sigma_{INL} = 2^{(B/2-1)} \sigma_u$

$\Rightarrow \sigma_{DNL} = 2^{1.5} \sigma_u = 0.18857$

& $\sigma_{INL} = 0.53496$

for 99% yield (3σ)

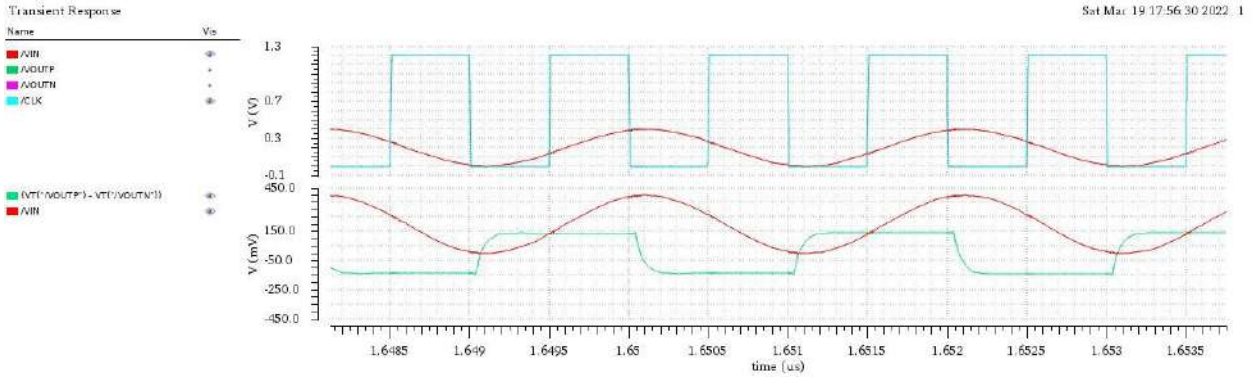
$\sigma_{DNL} = \frac{0.18857}{3} = 0.06285$

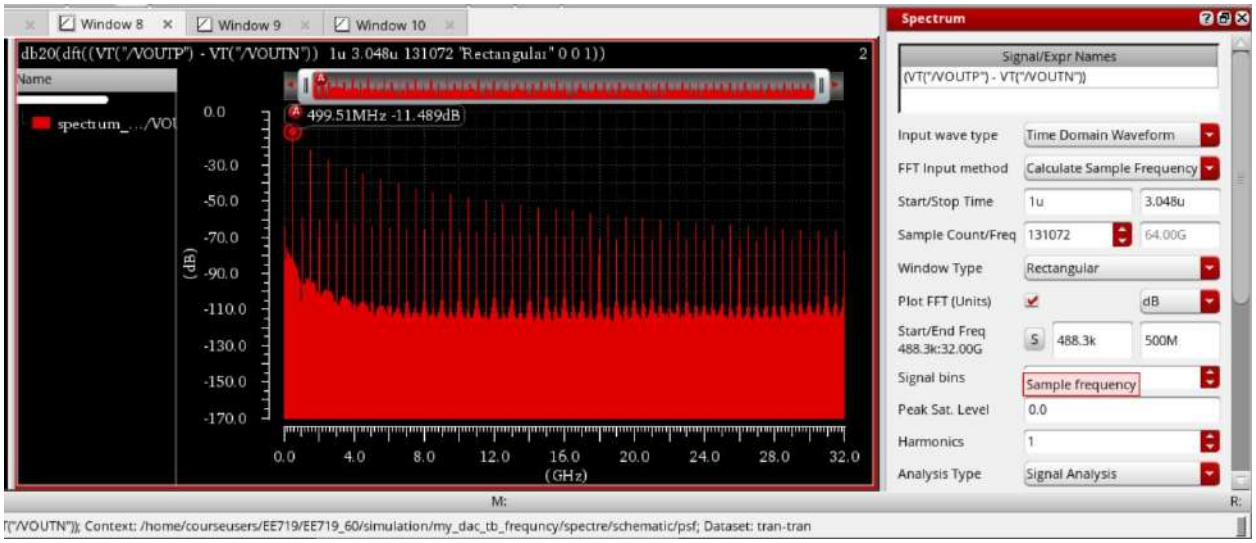
$\sigma_{INL} = \frac{0.53496}{3} = 0.17832$

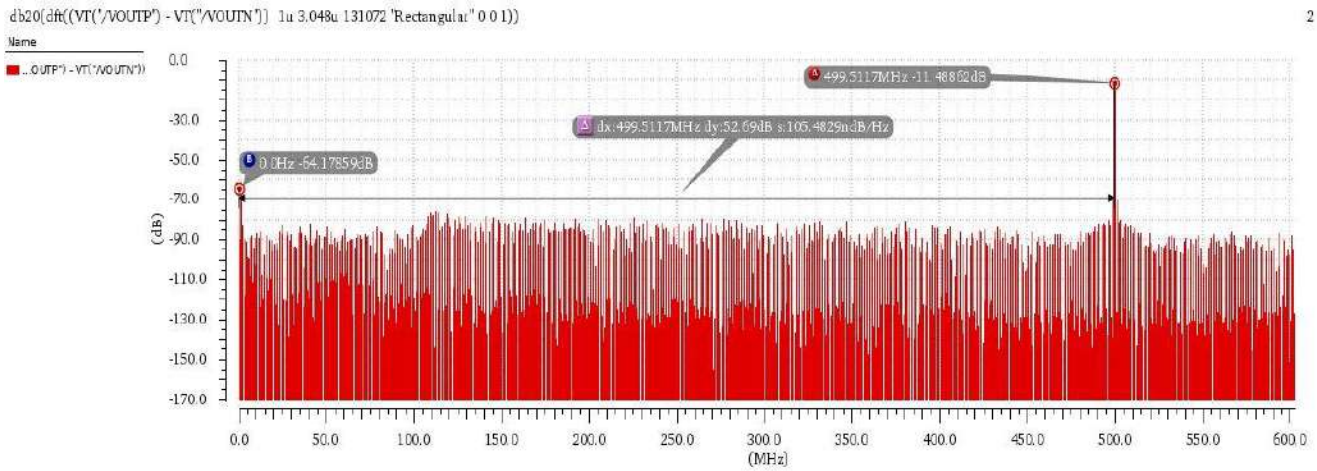
Actual(in LSB)	Theoretical(in LSB for 99% yield)
0.063	0.06285
0.178	0.17832

3D)

We have performed transient analysis with N=2048 and M=199 which corresponds to an input signal of 1000*(199/2048) MHz = 97.16MHz

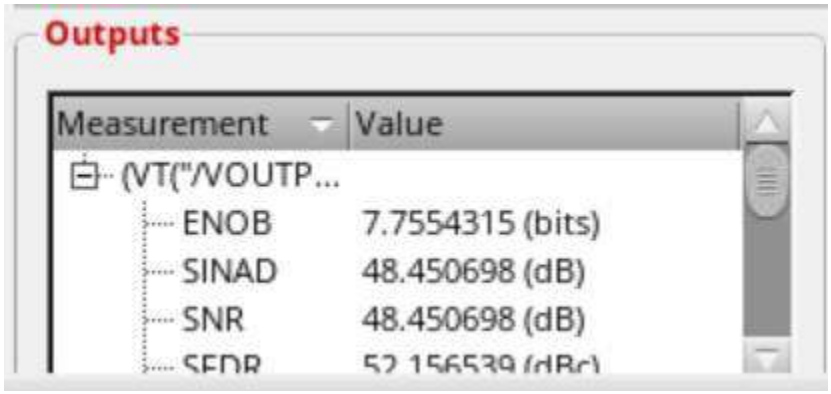


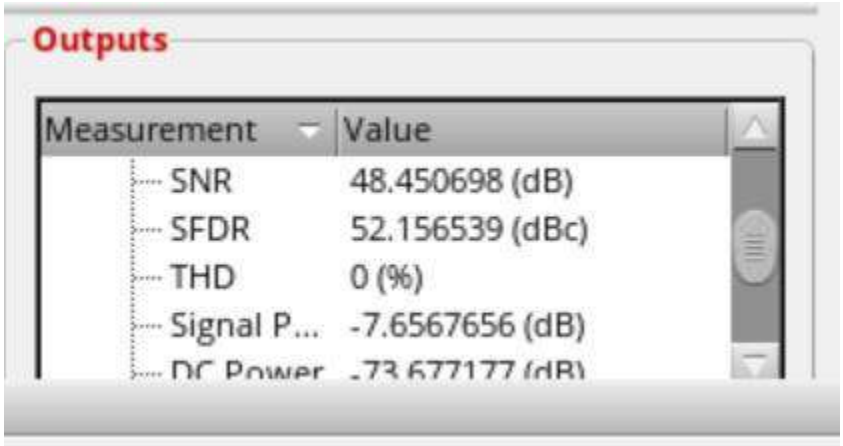


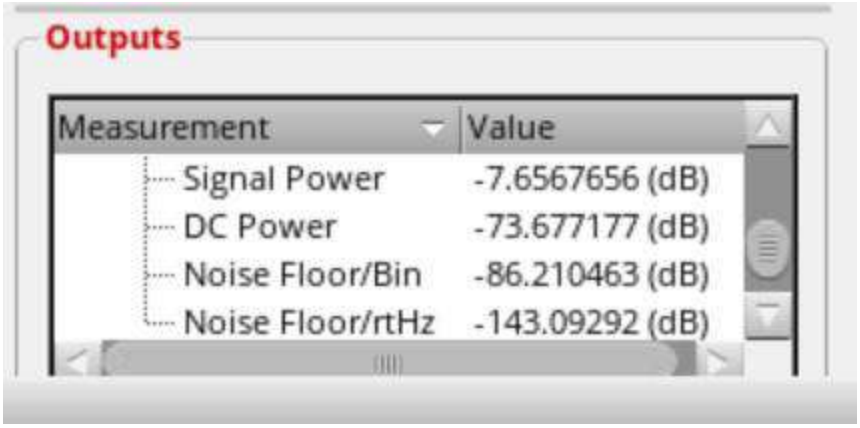


From the above FFT plot, we notice that there is a highest peak at 97.16 MHz and the next highest Peak is at 194.32 MHz (2nd harmonic).

Reason:The harmonics are due to capacitive coupling which causes distortion during transitions.



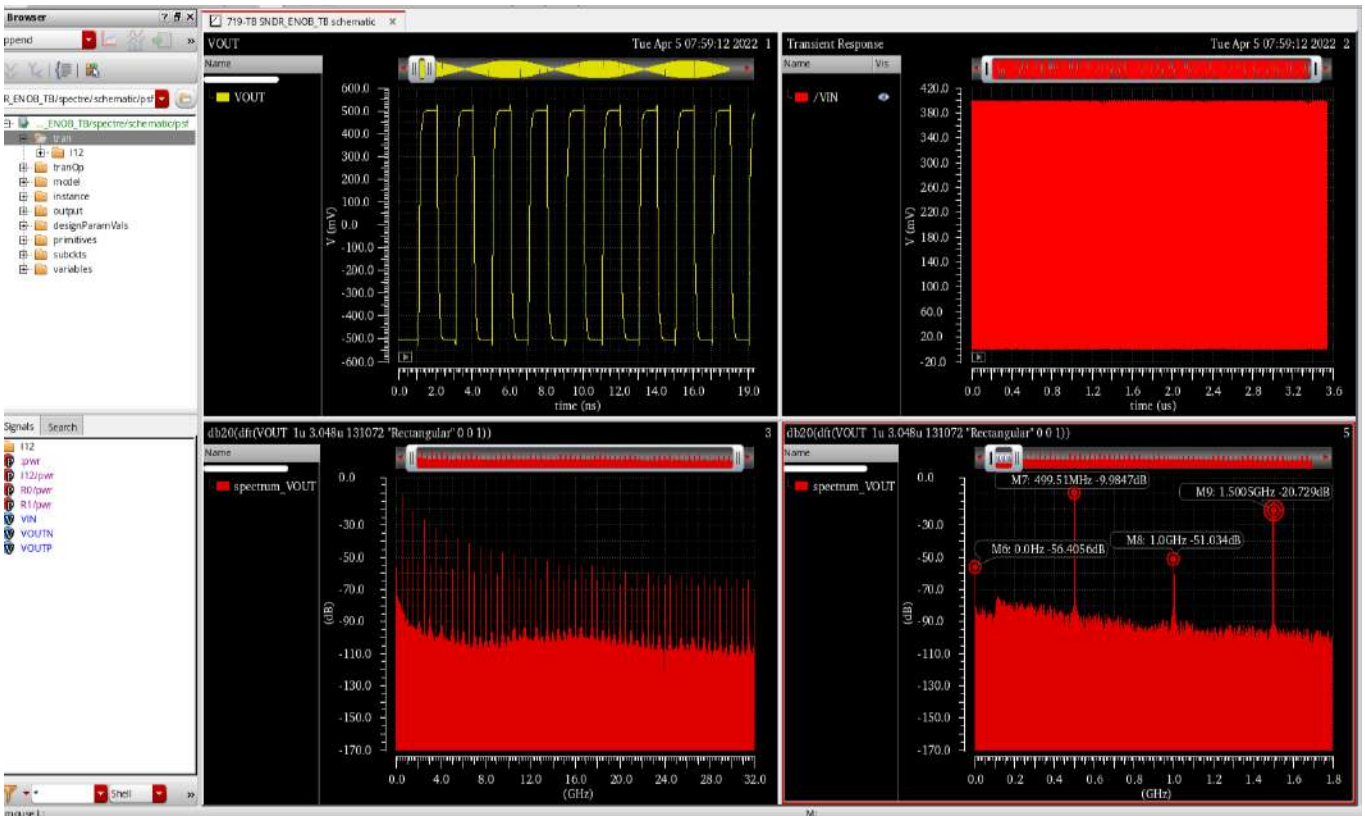


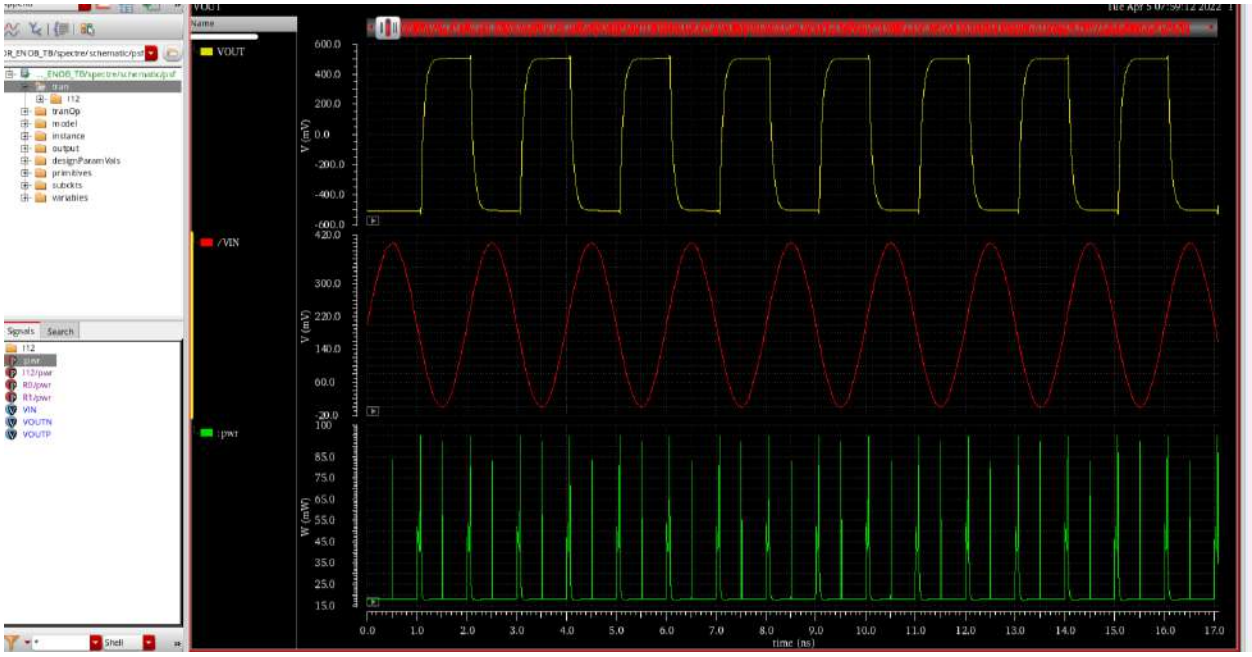


To improve the SNDR we need to minimize the capacitance at the drain of cascode current source in unit cell.

3E)

We have performed transient analysis with N=2048 and M=1023 which corresponds to an input signal of 1000*(1023/2048) MHz = 499.511MHz.





From the above FFT plot, we found a highest peak at 499.5117 MHz which corresponds to the input sinusoid and a second highest peak at around DC.
There are no harmonics here since the signal frequency is close to Nyquist frequency, so only the fundamental tone lies within the band

Outputs

Measurement	Value
VOUT	
ENOB	6.9970271 (bits)
SINAD	43.885103 (dB)
SNR	43.885103 (dB)
SFDR	49.808308 (dBc)
THD	0 (%)
Signal P...	-9.9846801 (dB)
DC Power	-56.40559 (dB)
Noise Fl...	-83.972783 (dB)
Noise Fl...	-140.85524 (dB)

3F)

For part 3D

SFDR	52.156dBc
SNDR	48.45dB
ENOB	7.755bits

For part 3E

SFDR	49.80dBc
SNDR	43.88dB
ENOB	6.997bits

3G)
I have done for part 3E i.e.,frequency>400MHz.
The average power that I got from the below image(done using cadence pwr) is Pavg=20.13mW.

getData(":pwr" ?result "tran") avera...

	time (s)	getData(...an") (W)	Expression	Value
1	0.000	18.38E-3	average(getData...	20.13E-3
2	39.06E-15	18.38E-3		
3	117.2E-15	18.38E-3		
4	273.4E-15	18.38E-3		
5	585.9E-15	18.39E-3		
6	1.211E-12	18.39E-3		
7	2.461E-12	18.39E-3		
8	4.961E-12	18.42E-3		
9	7.480E-12	18.45E-3		
10	10.00E-12	18.46E-3		
11	10.08E-12	18.45E-3		
12	10.39E-12	18.43E-3		
13	11.02E-12	18.41E-3		
14	12.28E-12	18.39E-3		
15	14.61E-12	18.39E-3		
16	17.92E-12	18.38E-3		
17	23.10E-12	18.38E-3		
18	31.74E-12	18.38E-3		
19	46.96E-12	18.38E-3		
20	77.39E-12	18.38E-3		
21	138.3E-12	18.38E-3		
22	260.0E-12	18.38E-3		
23	380.0E-12	18.38E-3		
24	500.0E-12	18.38E-3		
25	500.0E-12	18.38E-3		
26	500.2E-12	18.39E-3		
27	500.5E-12	18.39E-3		
28	501.1E-12	18.40E-3		
29	502.4E-12	18.43E-3		
30	504.6E-12	18.45E-3		
31	505.0E-12	18.45E-3		
32	505.5E-12	18.45E-3		
33	506.0E-12	18.45E-3		
34	506.1E-12	18.46E-3		
35	506.3E-12	18.51E-3		
36	506.4E-12	18.57E-3		
37	506.7E-12	18.88E-3		
38	507.0E-12	19.23E-3		
39	507.1E-12	19.18E-3		
40	507.2E-12	19.12E-3		
41	507.4E-12	19.07E-3		
42	507.4E-12	19.04E-3		
43	507.6E-12	18.98E-3		
44	508.0E-12	18.89E-3		
45	508.2E-12	18.83E-3		
46	508.4E-12	18.78E-3		
47	508.7E-12	18.73E-3		