# EE-719 Project Part-2

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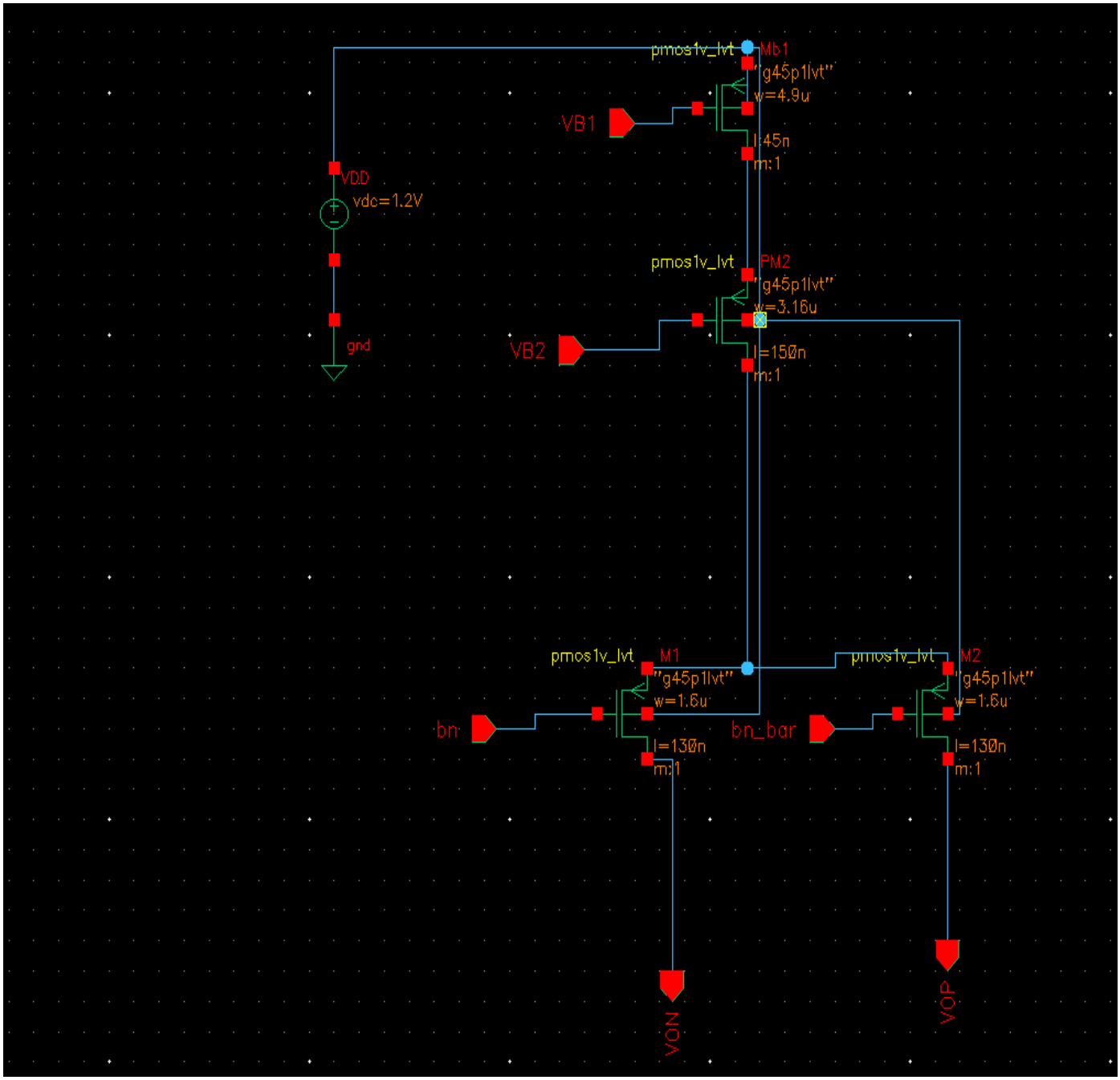
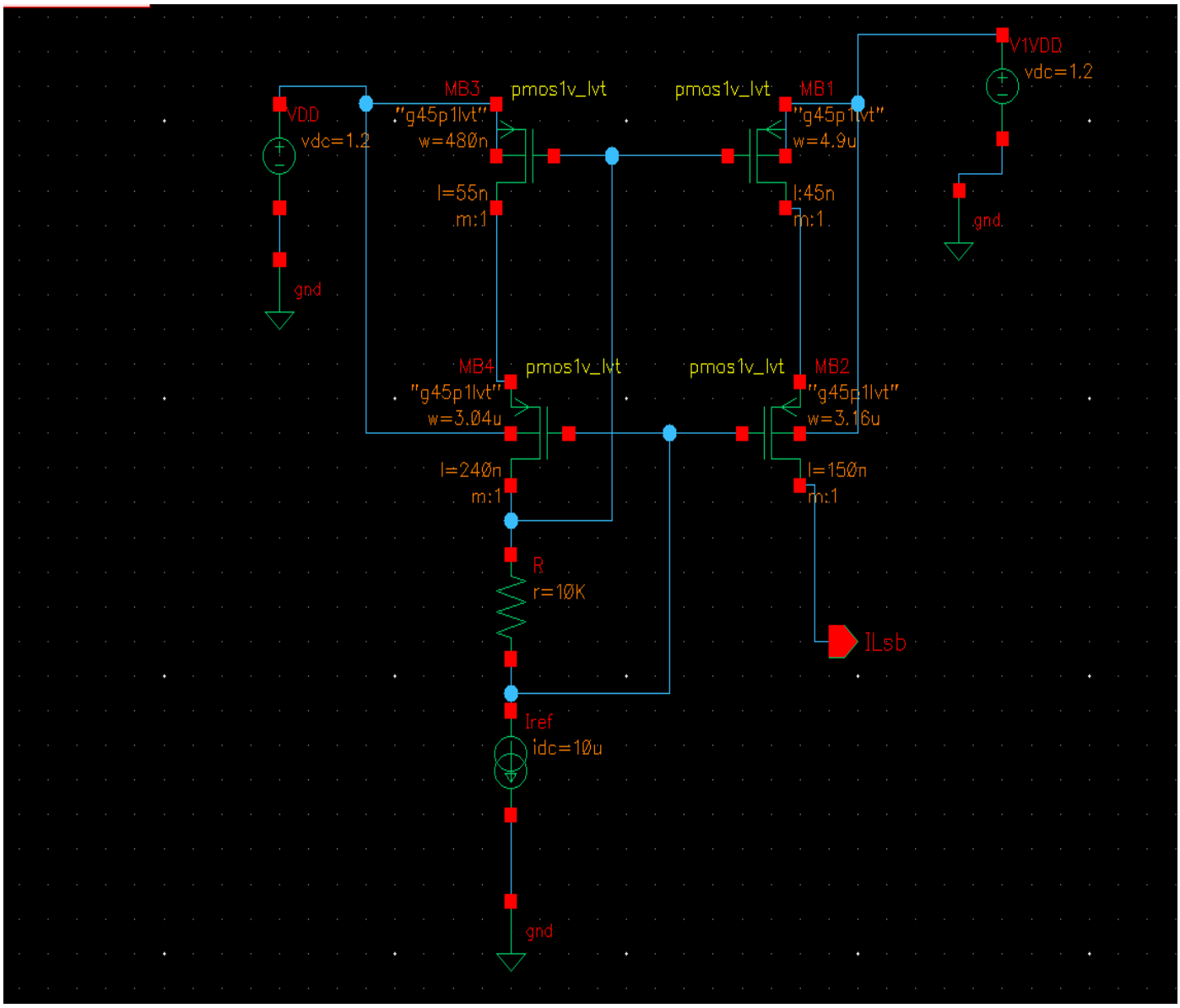
2a)

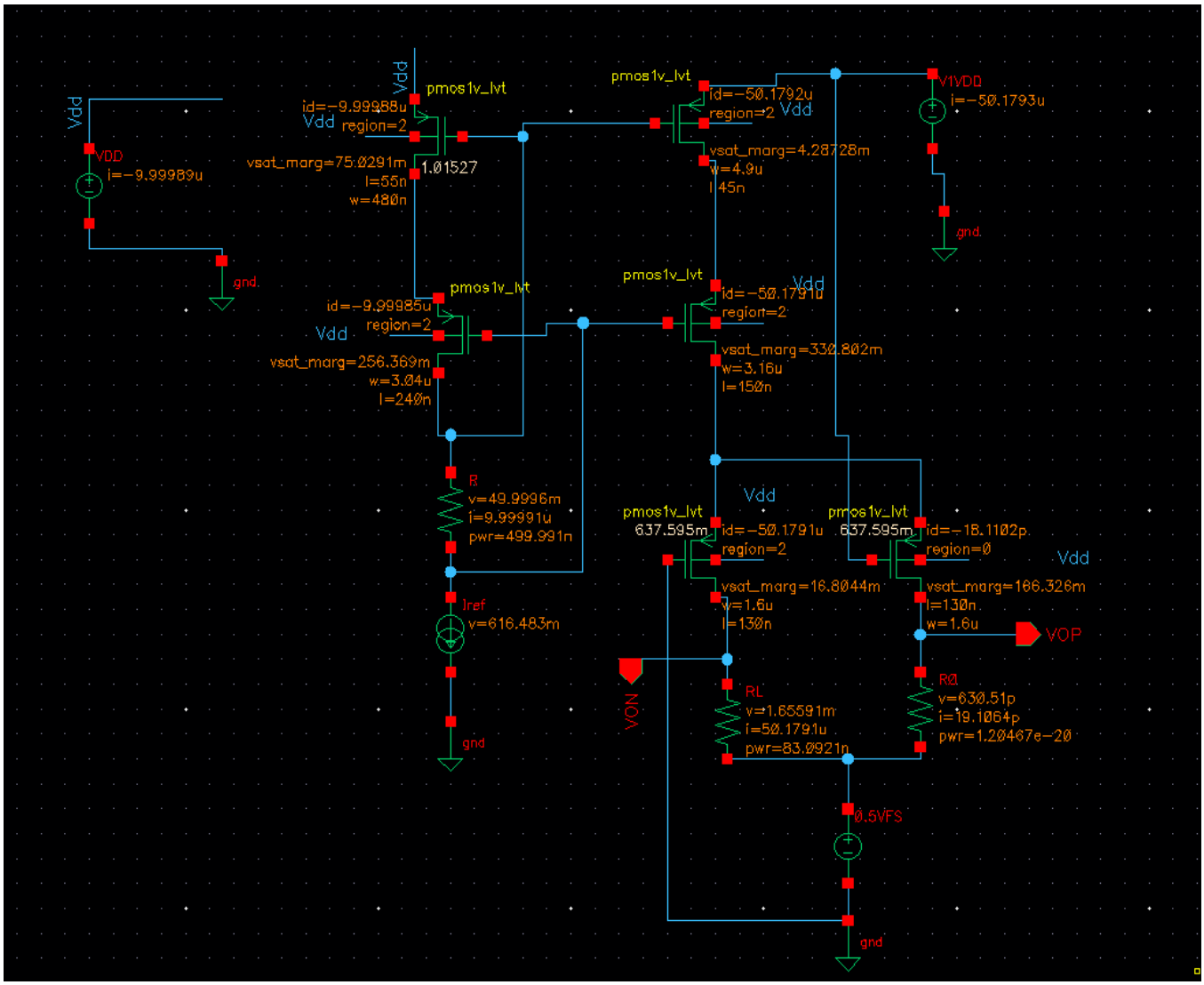
Schematic of Fig.2:



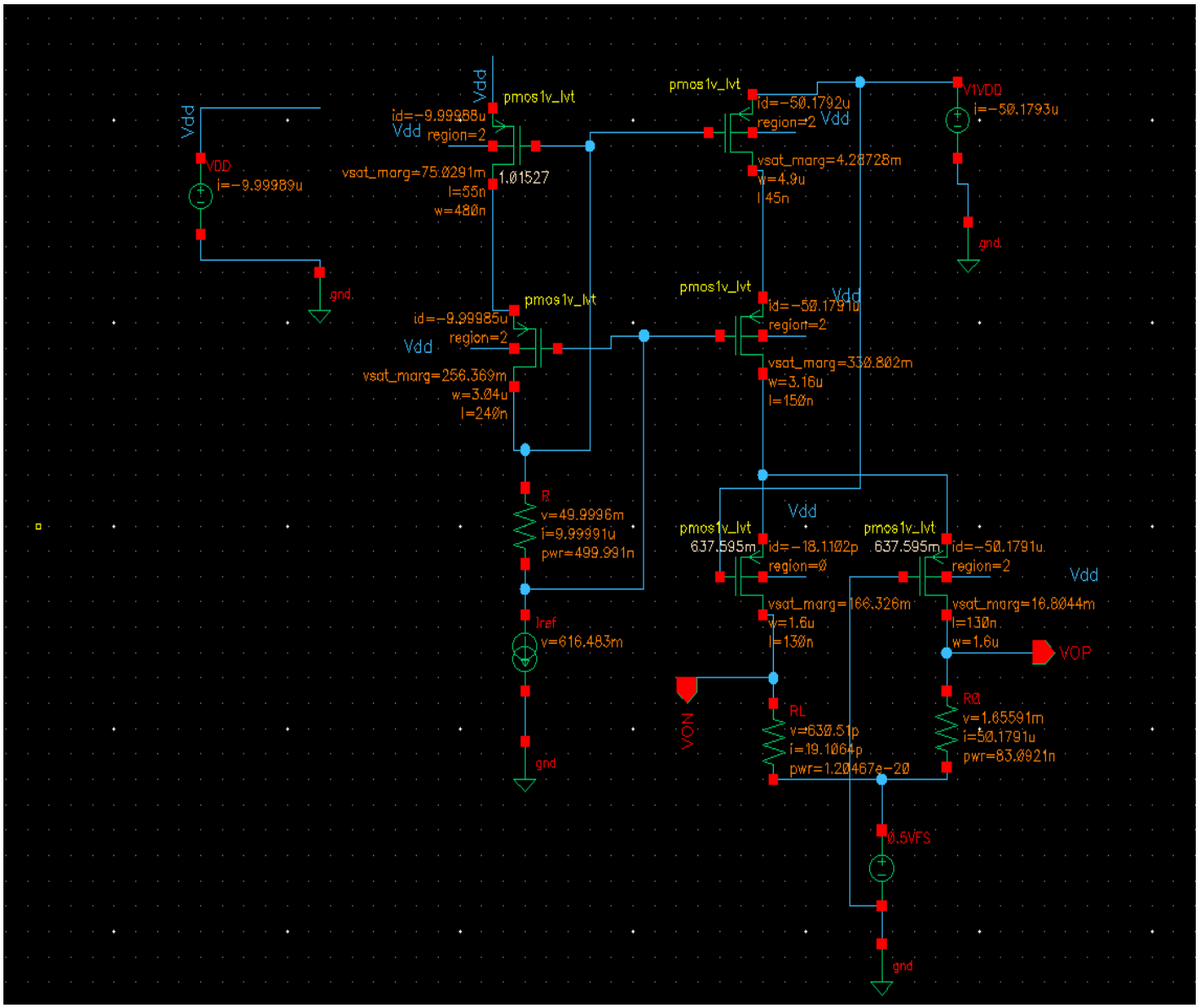
Schematic of fig.3:



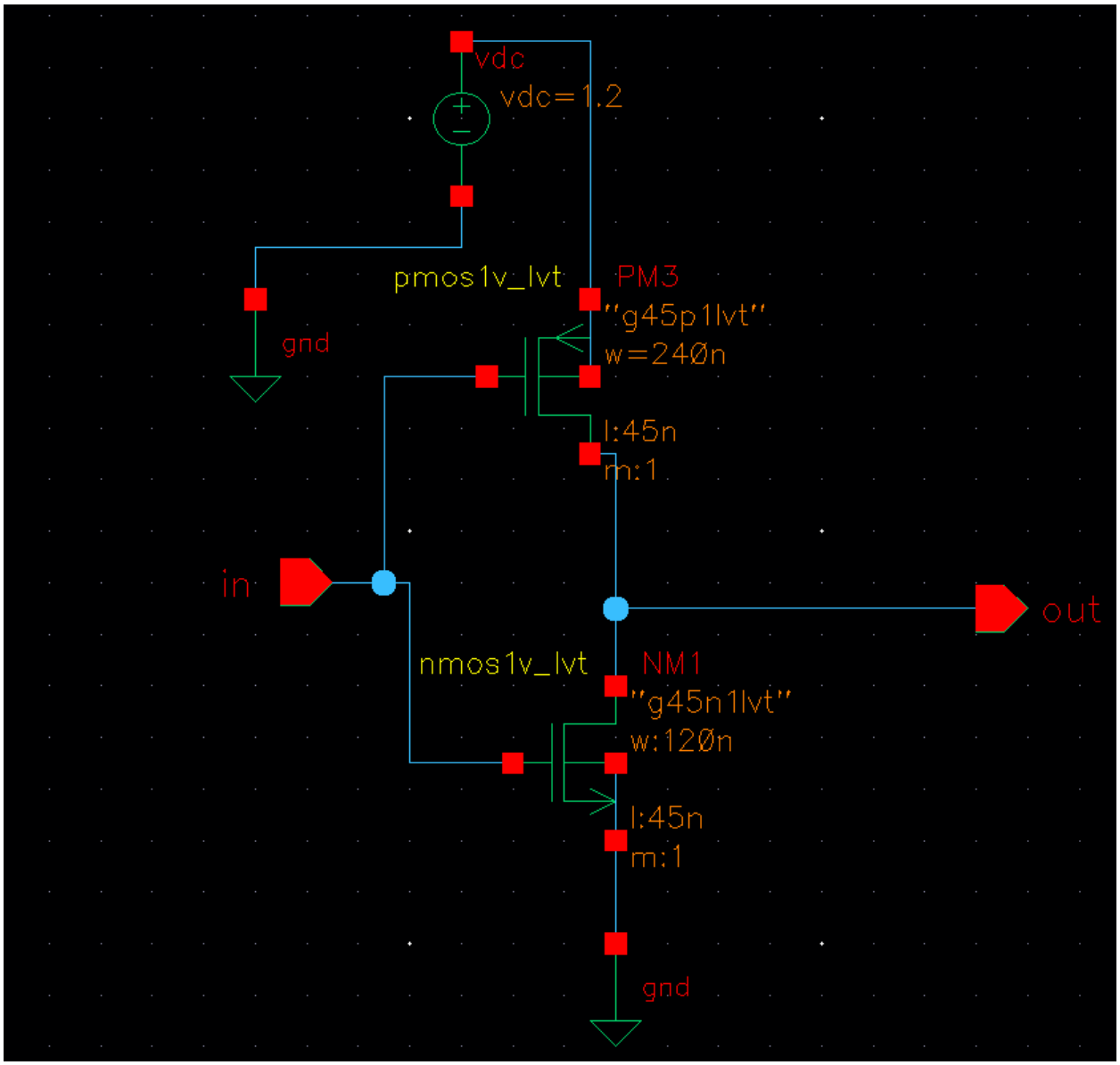
Schematic of fig.6 for bn=0:



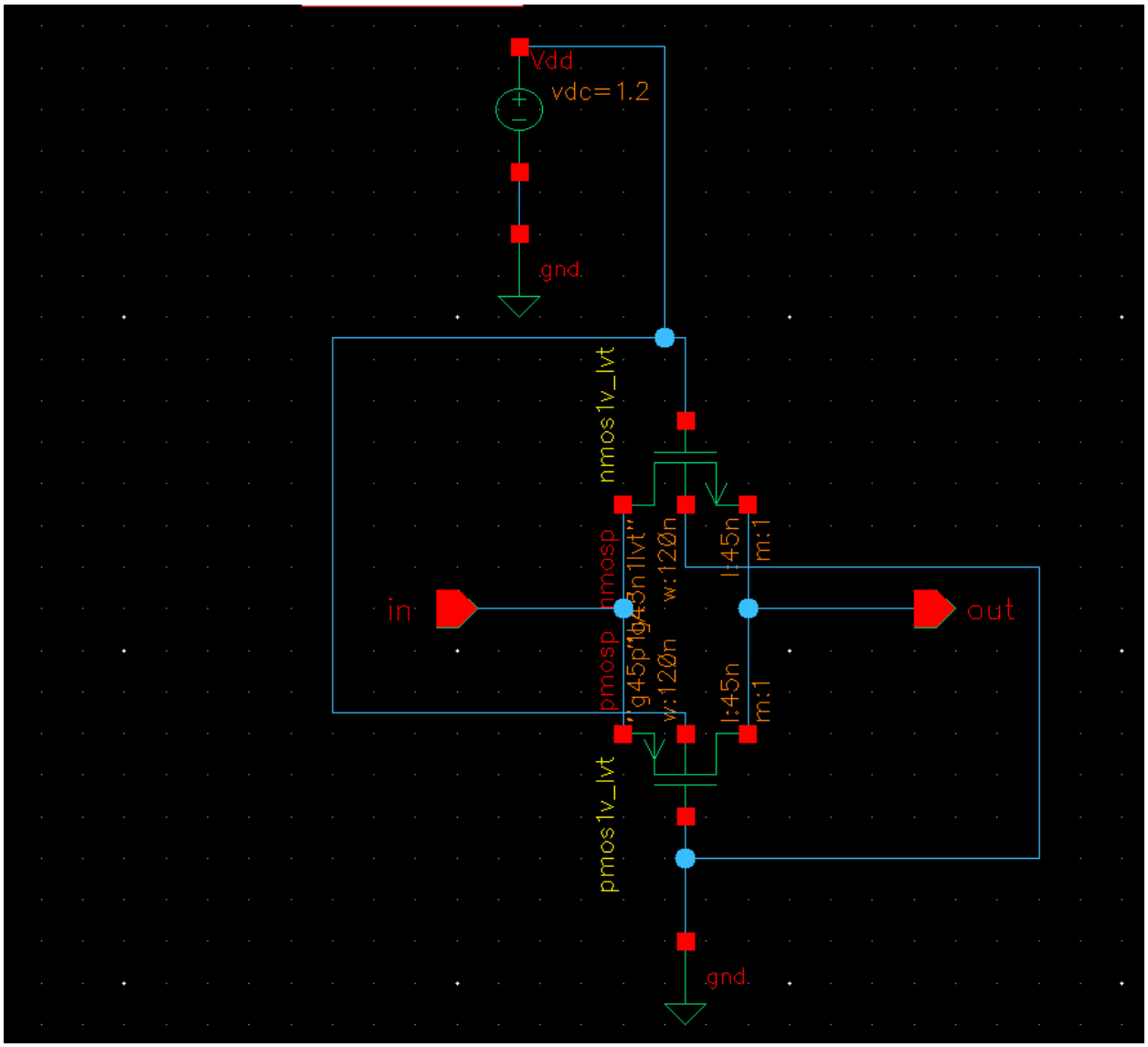
Schematic of fig.6 for bn=1:



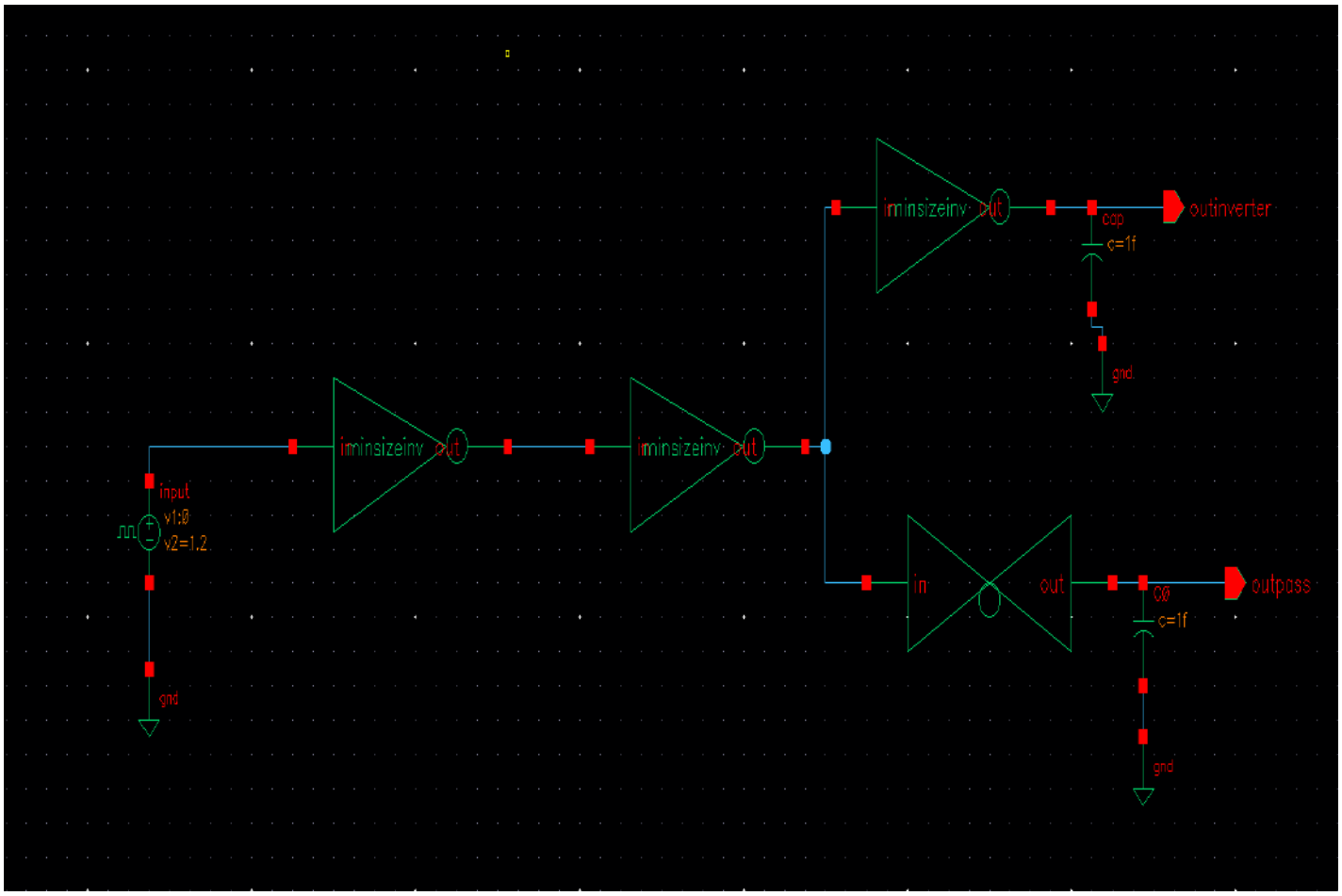
2b)
Min. size inverter:



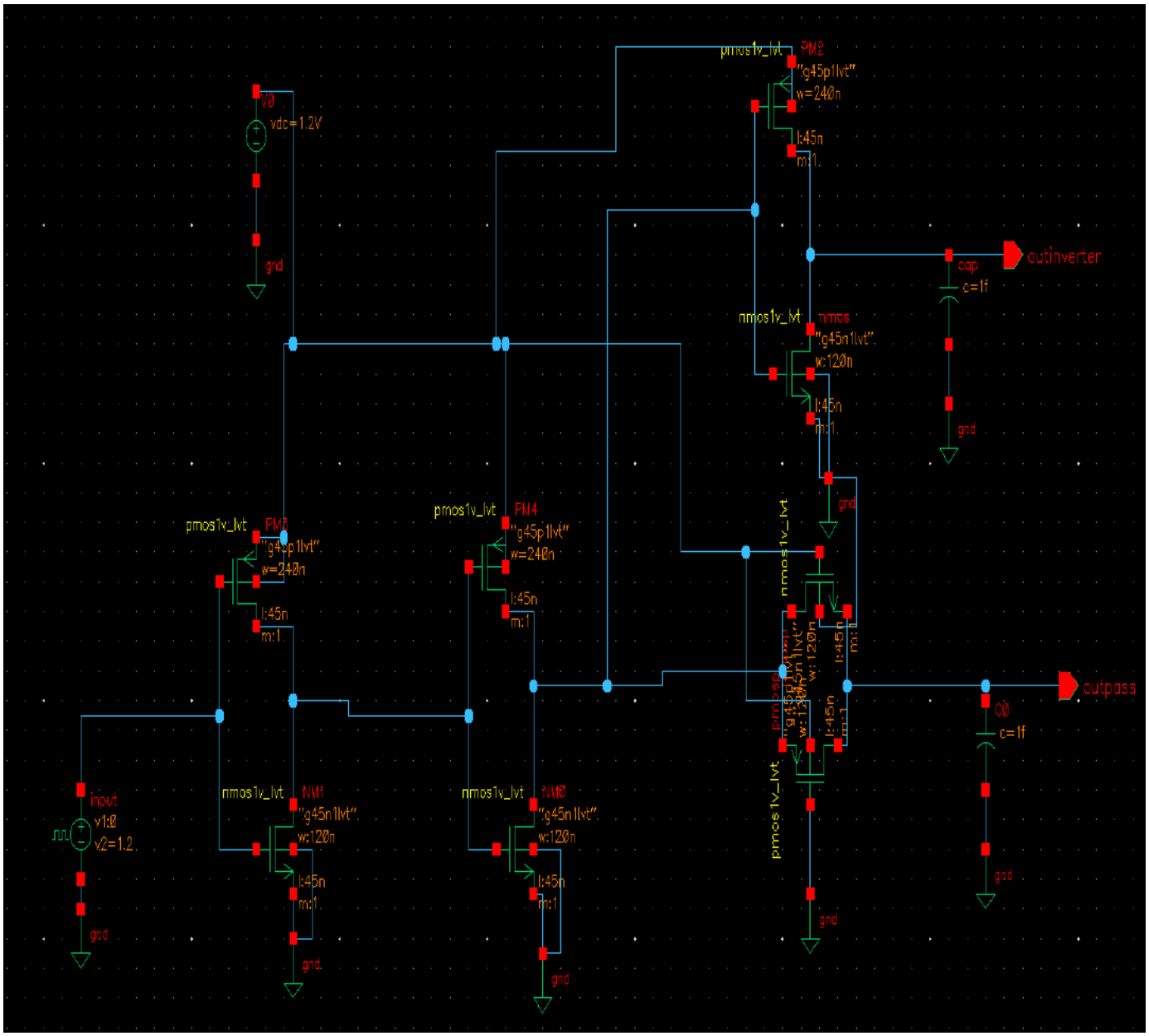
Pass inverter:

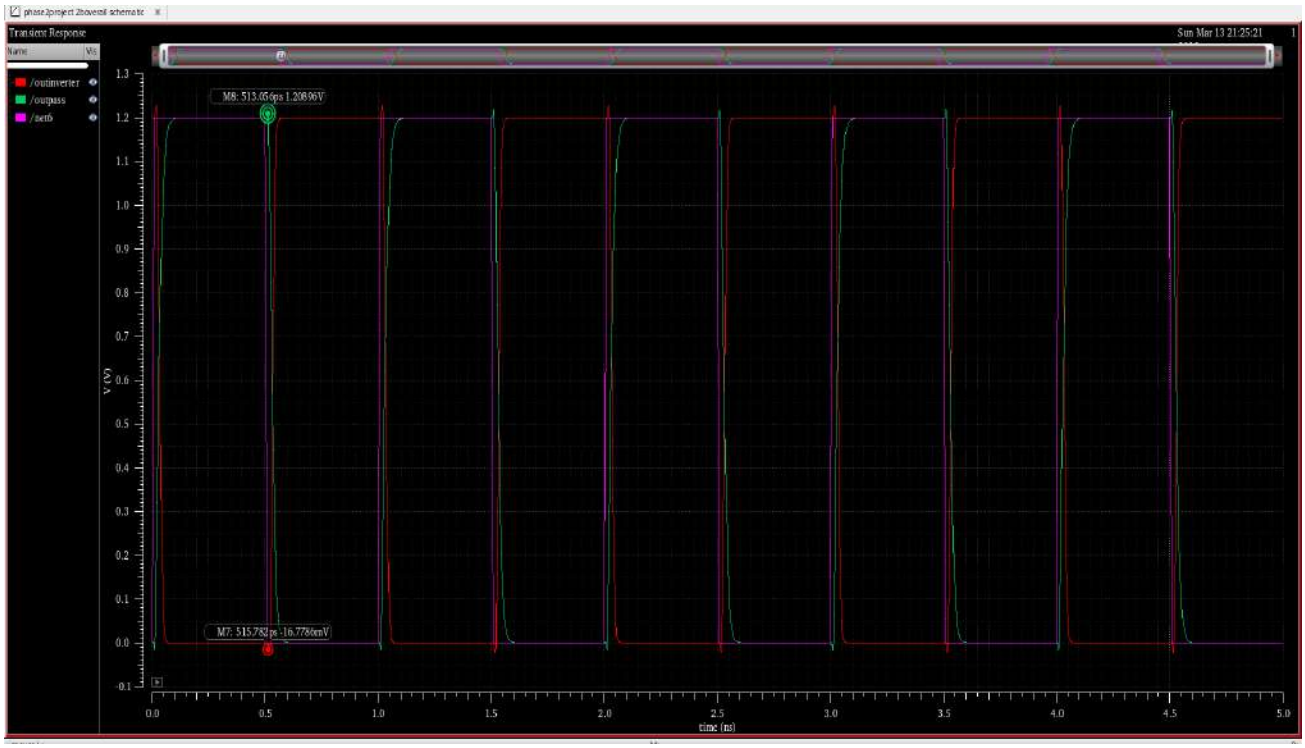


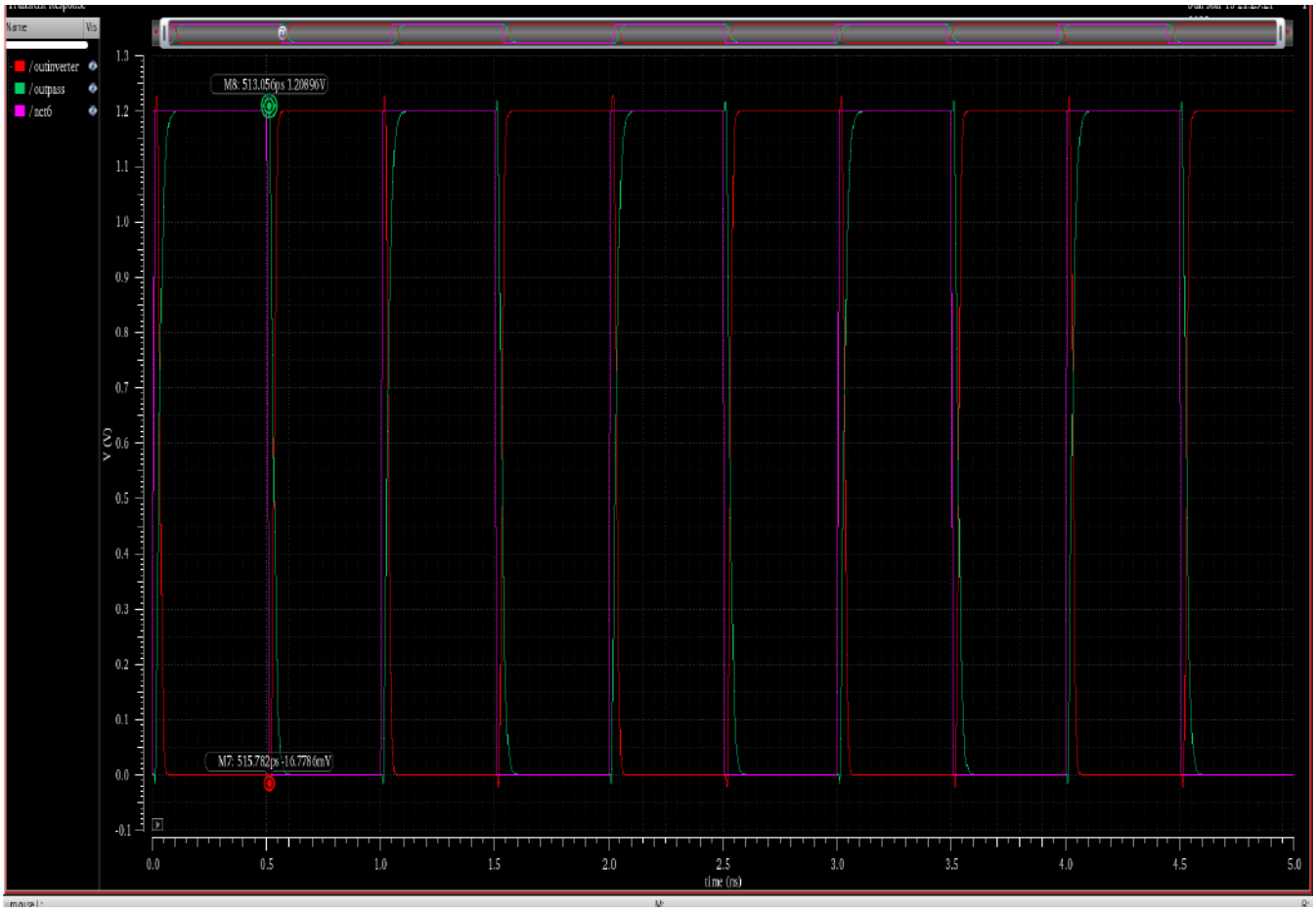
Pass transistor setup:

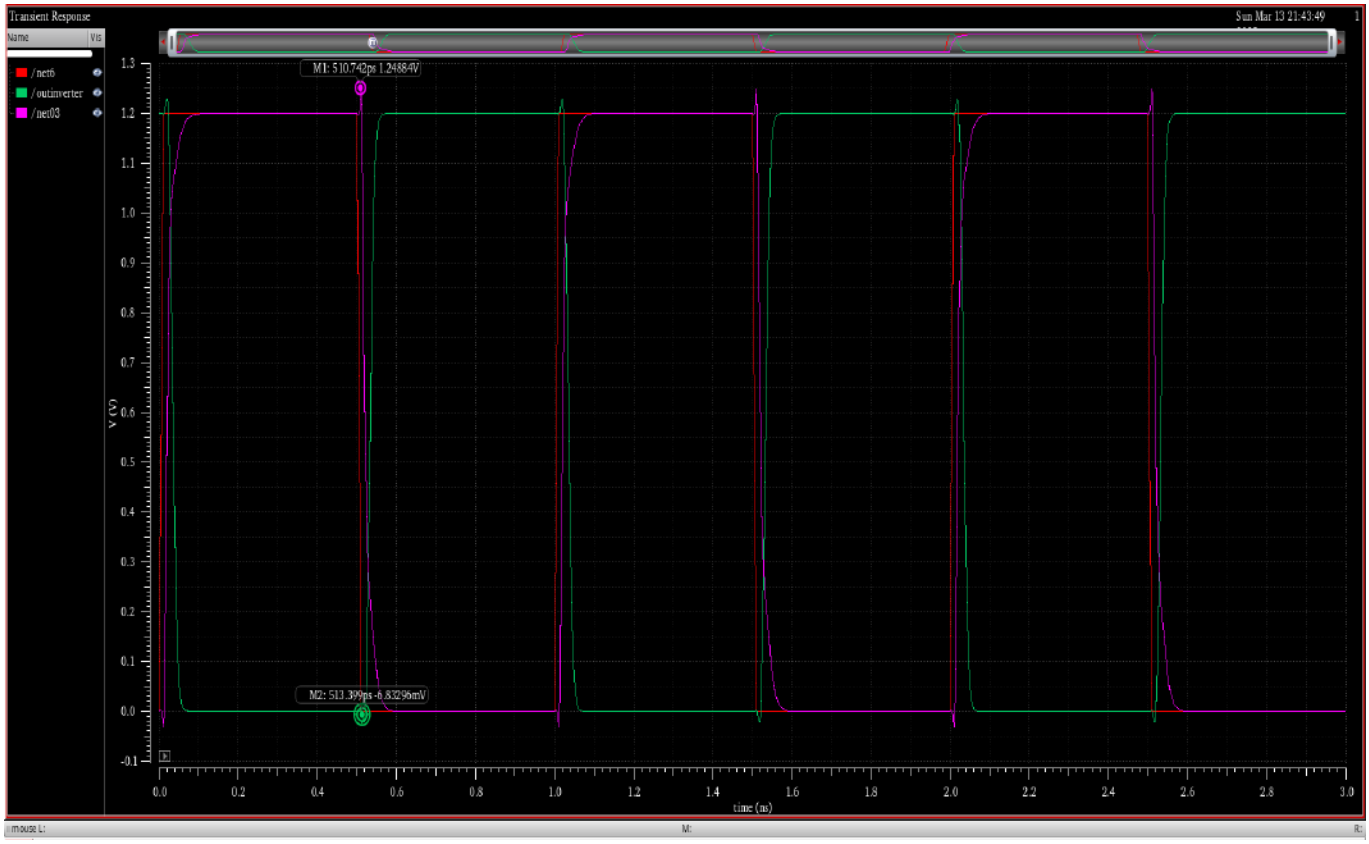


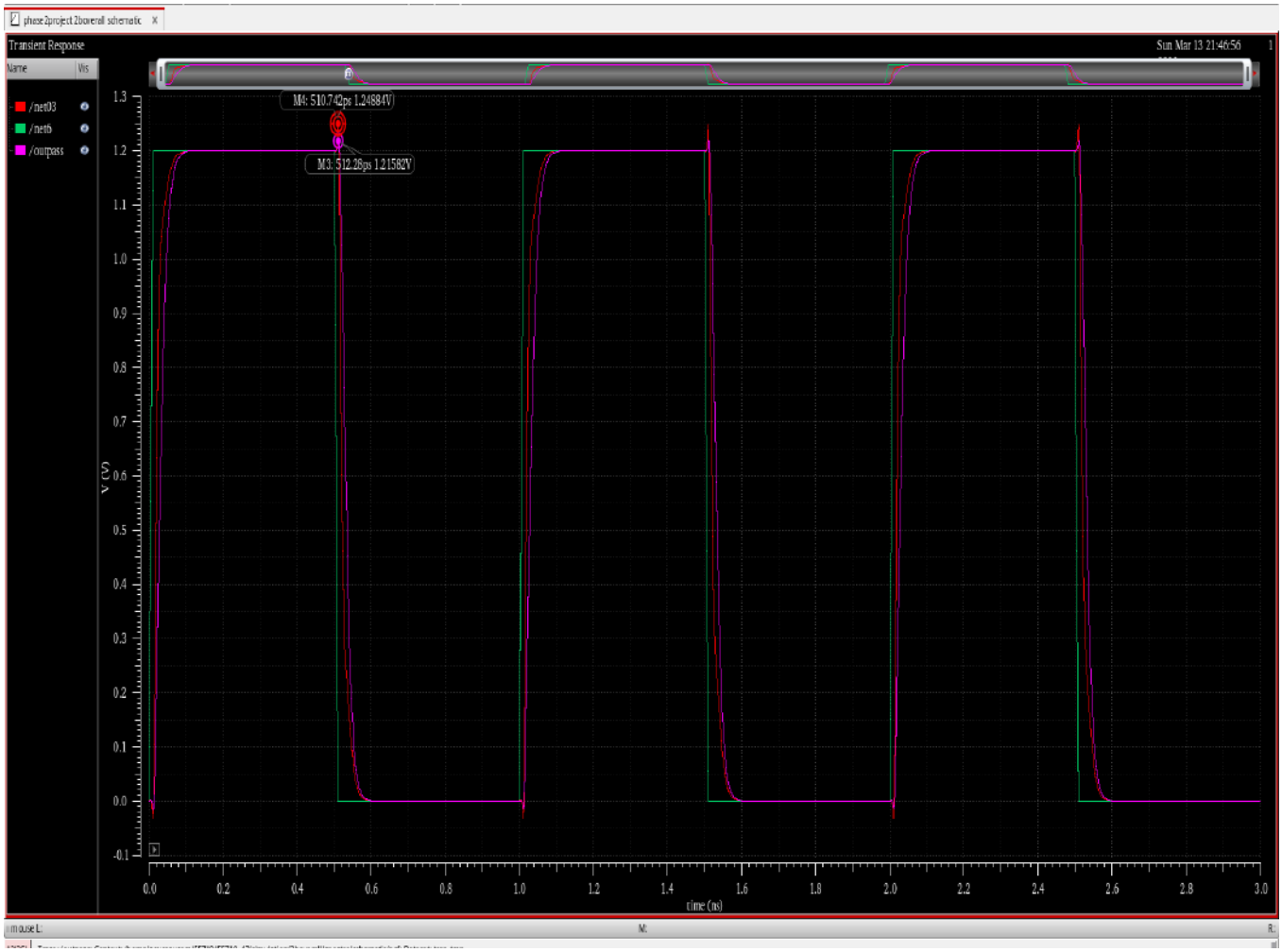
2b_schematic:




phase2project 2boverall schematic
Transient Response
Sun Mar 13 21:25:21
/outinverter
/outpass
/set6
M8: 513.056ps 1.2089V
M7: 515.782ps -16.7786mV
V (V)
time (ns)


Name
Vis
/outinverter
/outpass
/net6
M8: 513.056ps 1.20896V
M7: 515.782ps -16.7786mV
V (V)
time (ns)
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0


Transient Response
Sun Mar 13 21:43:49
Name
Vis
/ net6
/ outinverter
/ net03
M1: 510.742ps 1.2488mV
M2: 513.399ps -6.83296mV
V (V)
time (ns)
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0


phase2project 2boverall schematic
Transient Response
Sun Mar 13 21:46:56
Name
Vis
/net03
/netb
/outpass
M4: 510.742ps 1.24884V
M3: 512.26ps 1.21582V
V (V)
Time (ns)
mouse L:
M:
R:

min. size inverter

PMOS
W = 240n
L = 45n

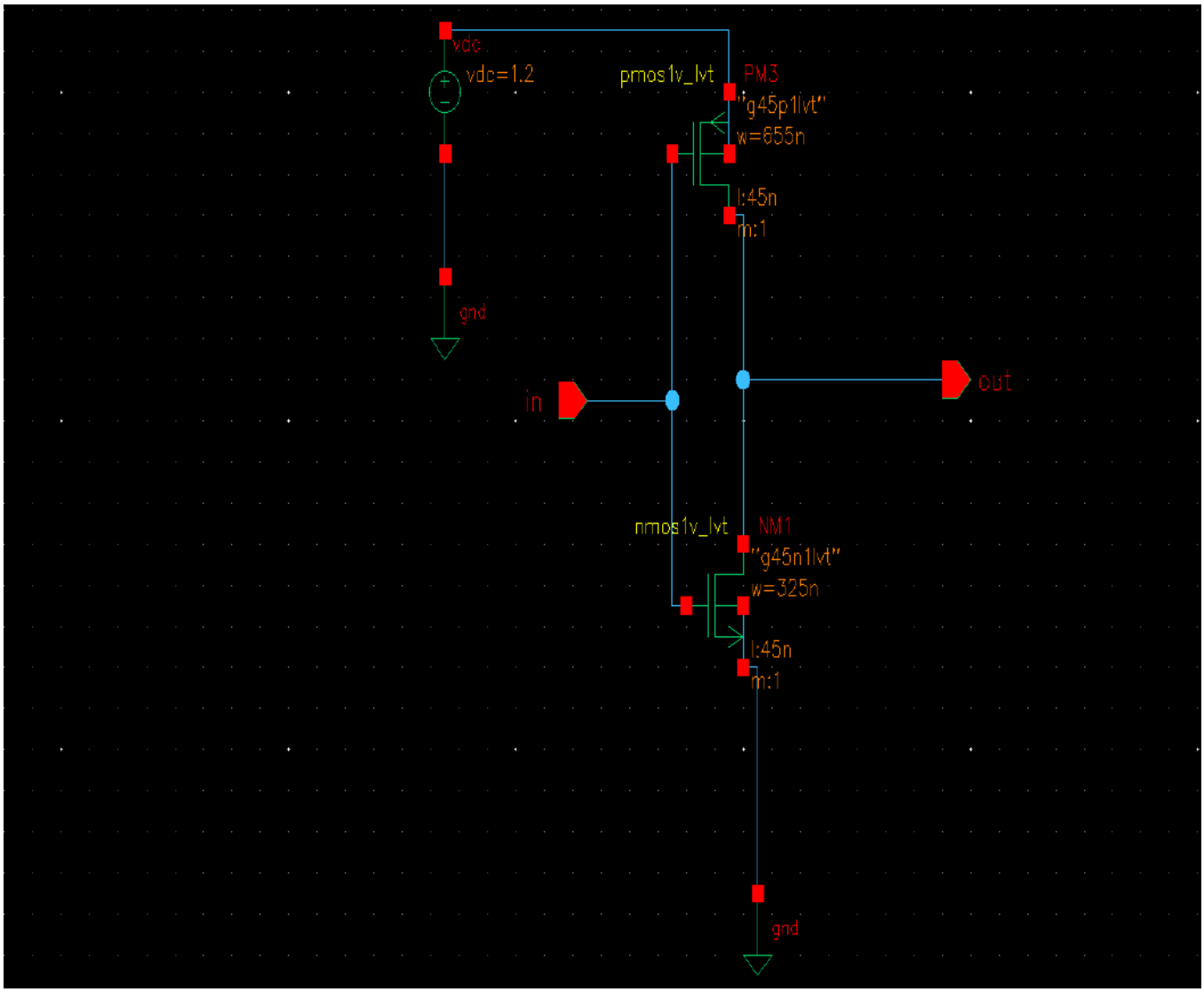
NMOS
W = 120n
L = 45n

pass txor

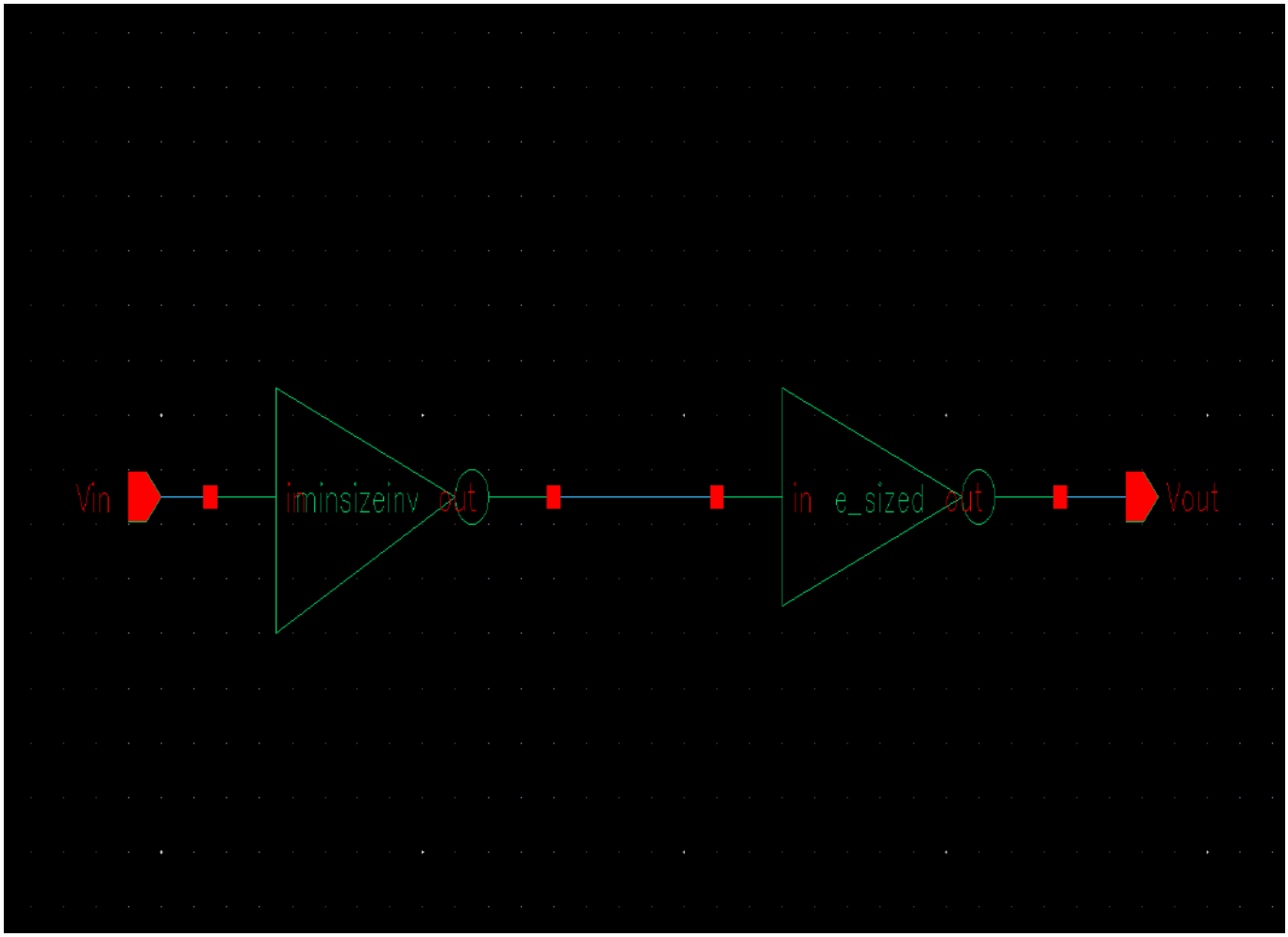
PMOS
W = 120n
L = 45n

NMOS
W = 120n
L = 45n

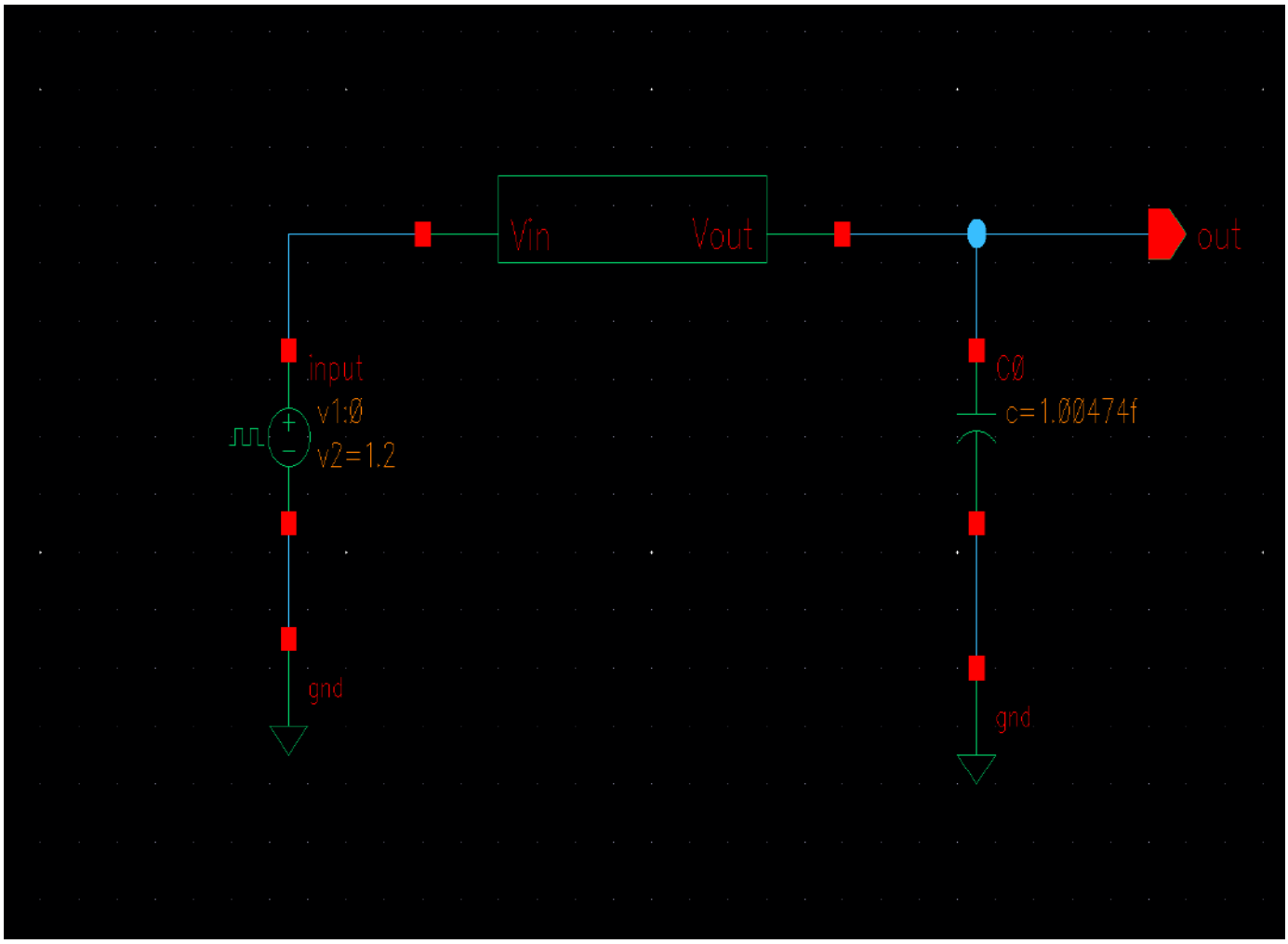
2c)
Scaled inverter

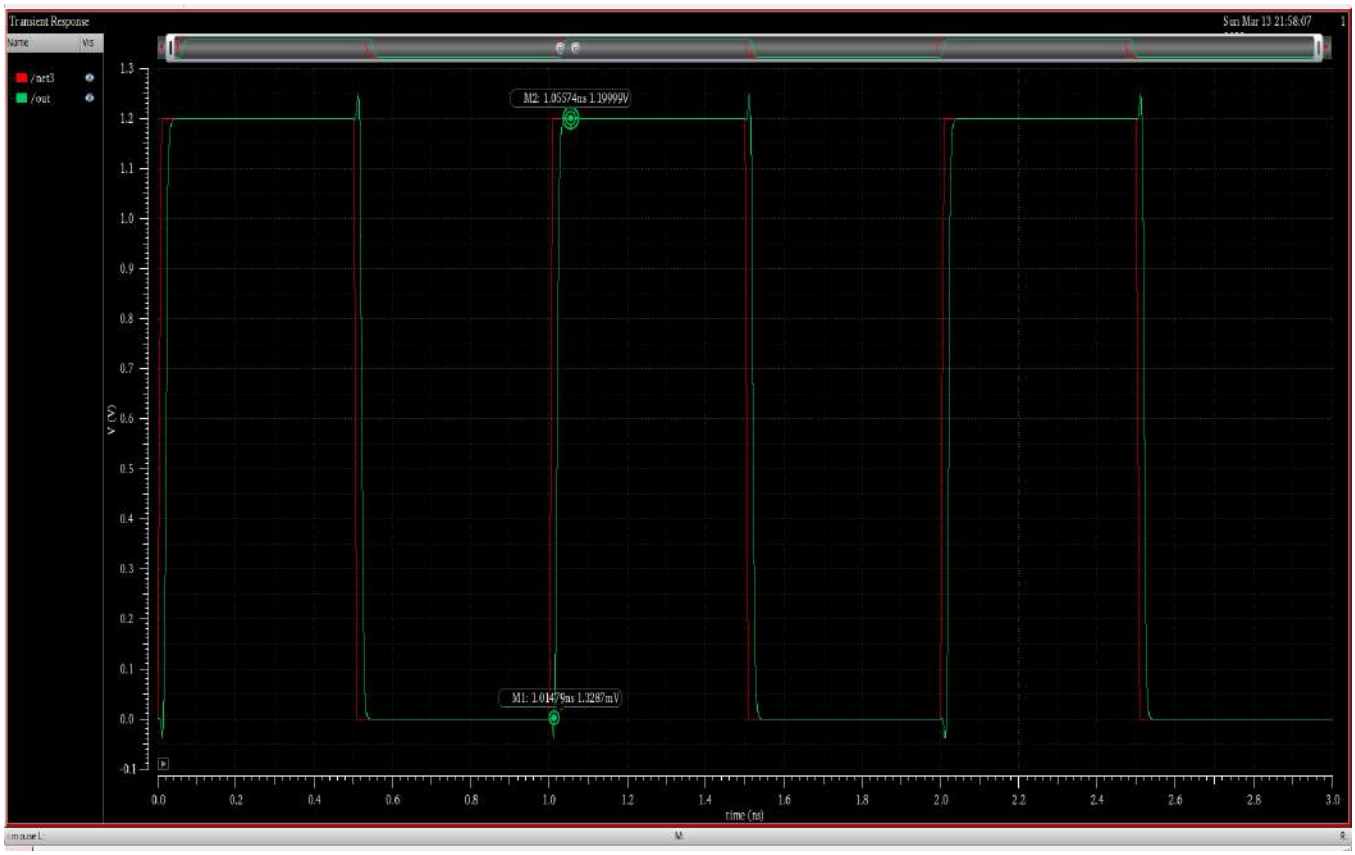


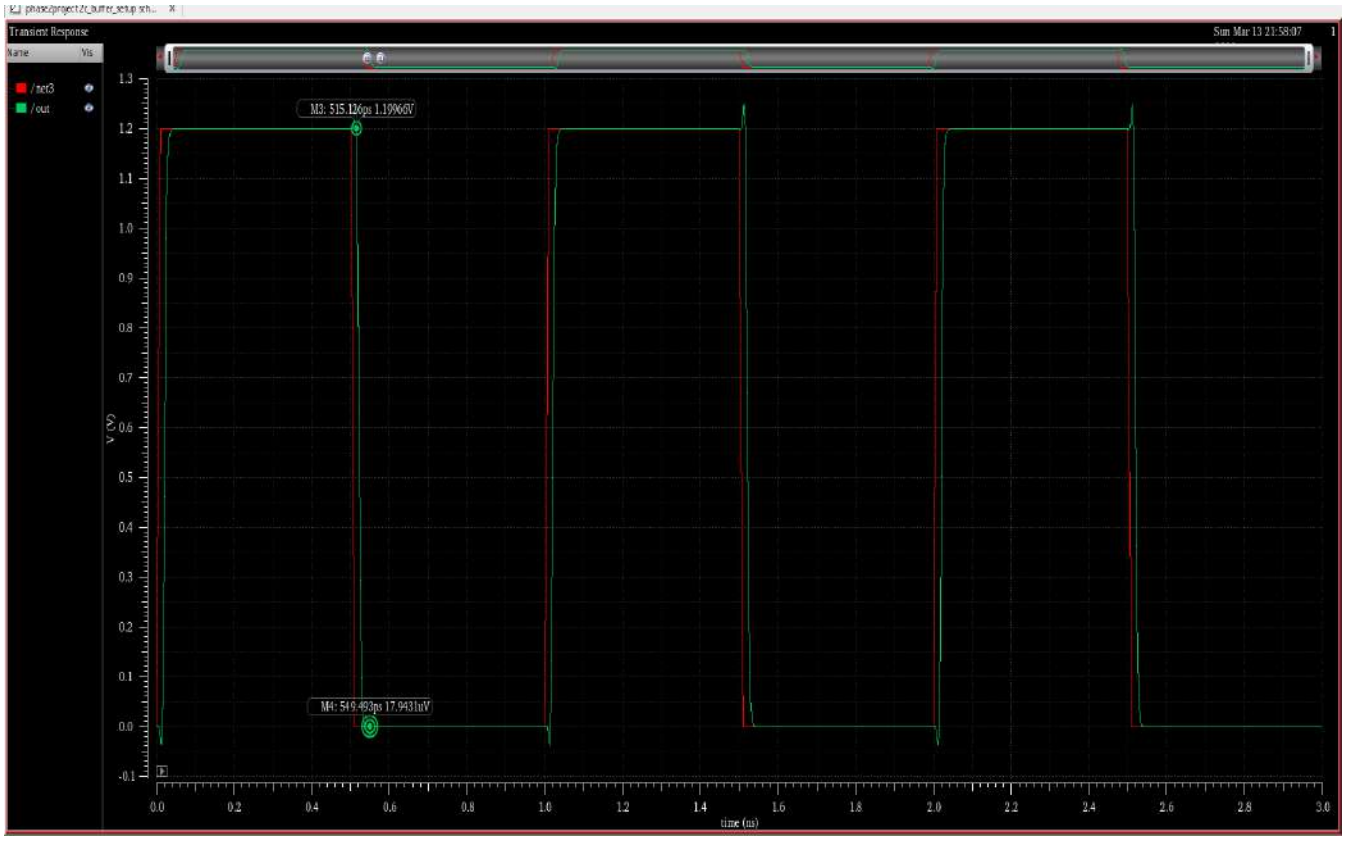
Buffer chain:



Test bench:




Transient Response
Sun Mar 13 21:58:07
Name
Vis
/net3
/out
M2: 1.05574ns 1.19999V
M1: 1.01479ns 1.3287mV
V (V)
time (ns)
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0


Transient Response
Sun Mar 13 21:58:07
Name
Vis
/net3
/out
M3: 515.126ps 1.19966V
M4: 549.493ps 17.943uV
V (V)
time (ns)
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0

$$n = \frac{\ln\left(\frac{C_L}{C_i}\right)}{\ln(\beta)}$$

$C \propto$ Area

$C_L \propto$ Area of $M_1$

$C_i \propto$ Area of min sized inverter

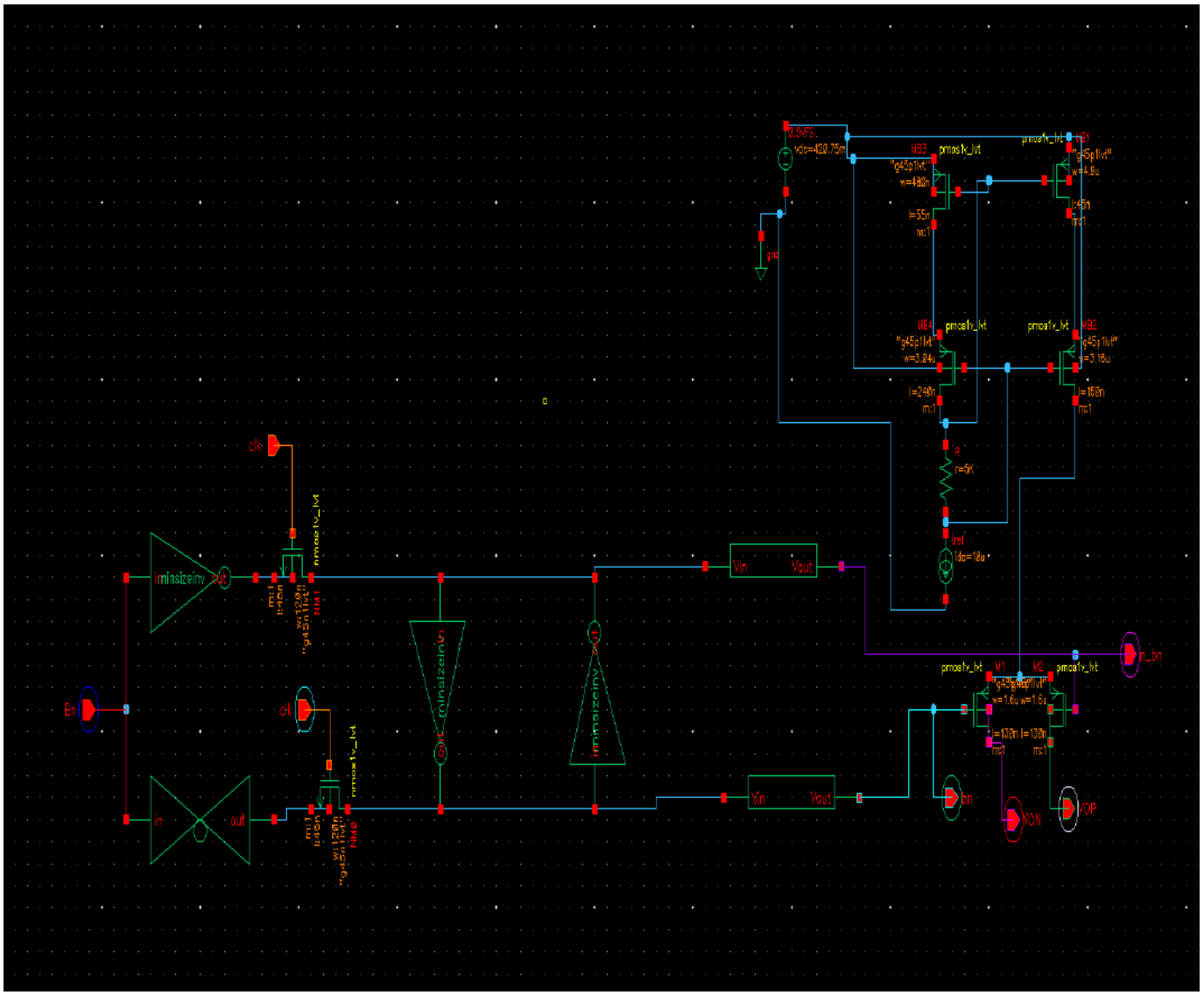
$\beta = e$

$$n = \ln\left(\frac{1.6\times10^{-6}\times120\times10^{-9}}{(120\times45 + 240\times45)10^{-18}}\right)$$

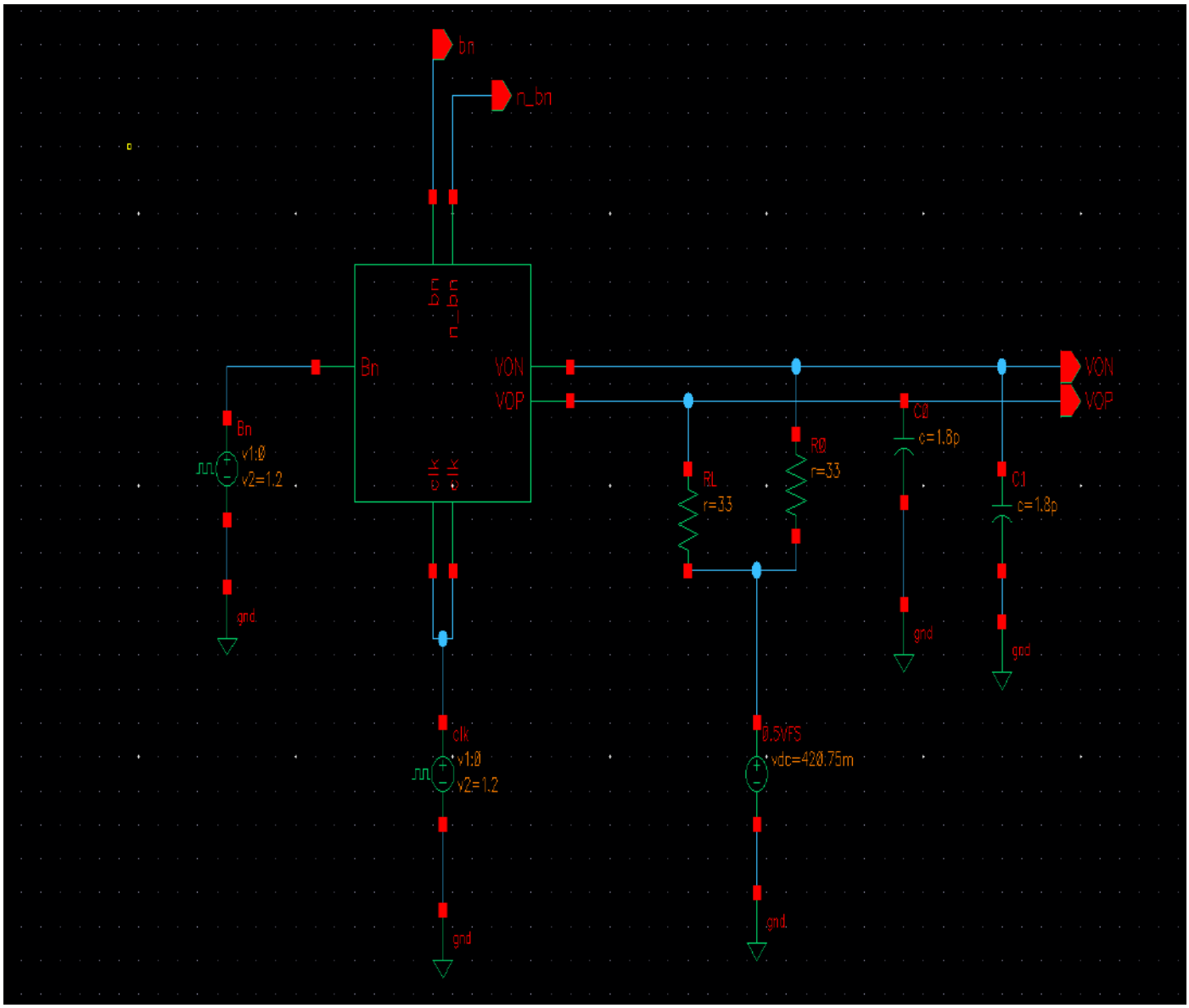
$$= 2.552$$

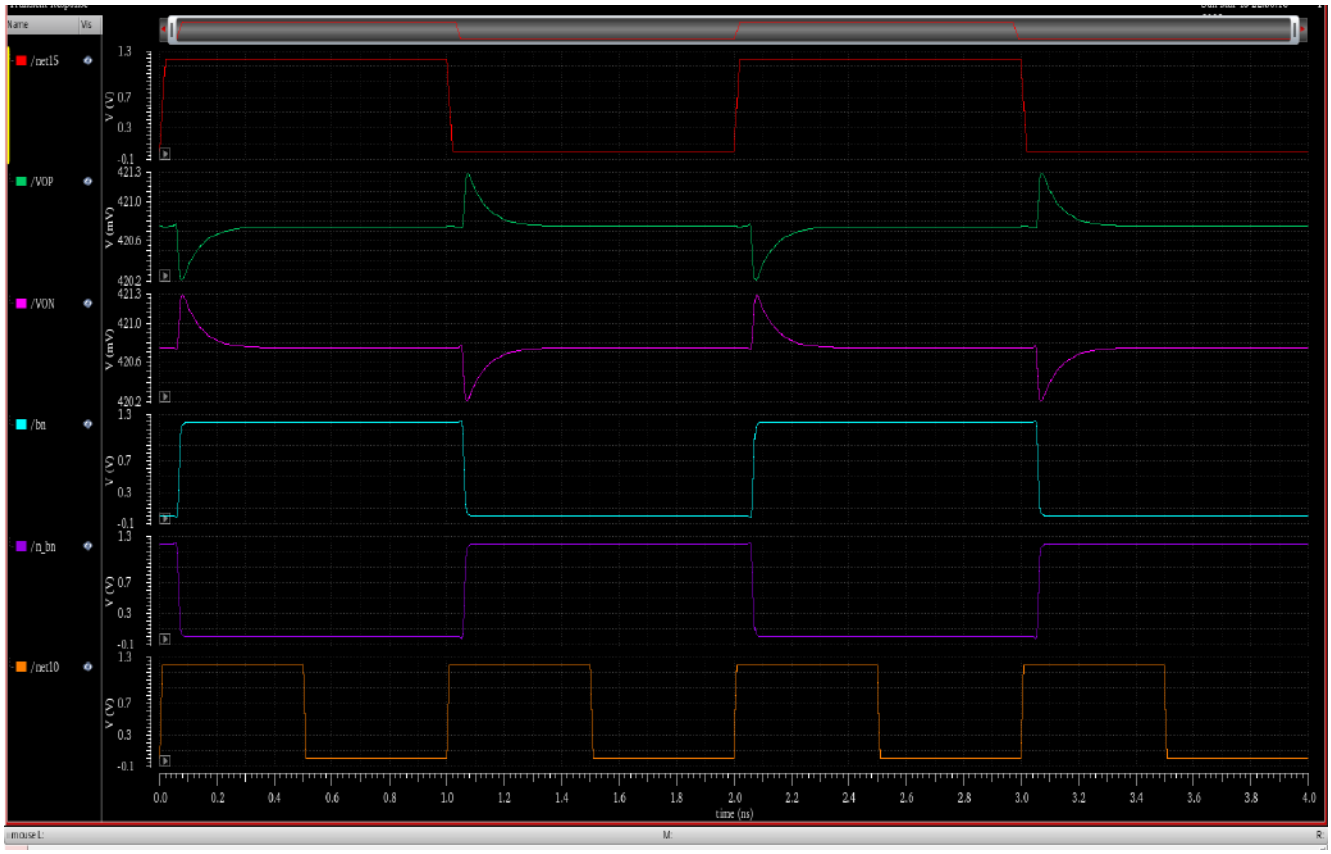
$\therefore$ No. of Stages = 2

2d)unitcell:


clk
iminsizeinv
out
Bn
in
out
Vin
Vout
Vin
Vout
bn
YON
YOP
pl_bn

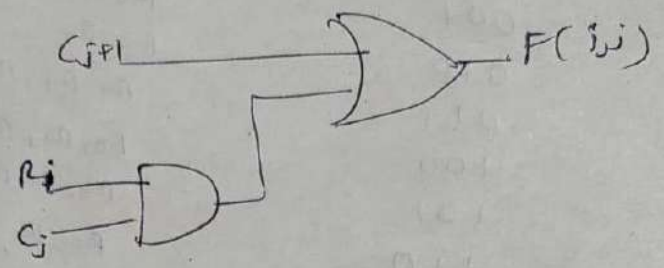
Testbench:


bn
n_bn
Bn
VON
VOP
Bn
v1:0
v2=1.2
gnd
RL
r=33
R0
r=33
C0
c=1.8p
C1
c=1.8p
VON
VOP
gnd
gnd
clk
v1:0
v2=1.2
gnd
0.5VFS
vdc=420.75m
gnd


Name
Vis
/net15
/VOP
/VON
/bn
/n_bn
/net10
V (V)
V (mV)
421.3
421.0
420.6
420.2
1.3
0.7
0.3
-0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
3.2
3.4
3.6
3.8
4.0
time (ns)
mouse L:
M:
R:

(2)

c)




$F(i,j) = C_{j+1} + R_i \times C_j$

working of column decoder:-

B<7:5>

∵ Co is connected to VDD ∴ Co is always ON

According to given code

| when B<7:5> | Columns active |
|---|---|
| 000 | Co |
| 001 | Co, C1 |
| 010 | Co, C1, C2 |
| 011 | Co, C1, C2, C3 |
| 100 | Co, C1, C2, C3, C4 |
| 101 | Co, C1, C2, C3, C4, C5 |
| 110 | Co, C1, C2, C3, C4, C5, C6 |
| 111 | Co, C1, C2, C3, C4, C5, C6, C7 |

working of Row decoder:-

B<4:2>

∵ R7 is connected to ground ∴ Ro is always OFF.

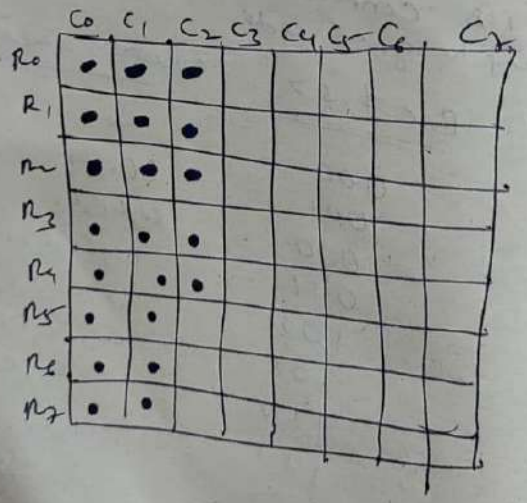
Accordeing to given code,

| when B<4:2> | Rows active |
|---|---|
| 000 | R0 |
| 001 | R0, R1 |
| 010 | R0, R1, R2 |
| 011 | R0, R1, R2, R3 |
| 100 | R0, R1, R2, R3, R4 |
| 101 | R0, R1, R2, R3, R4, R5 |
| 110 | R0, R1, R2, R3, R4, R5, R6 |
| 111 | |

FOR 01010100:-

B<7:5> : 010 ⇒ C0, C1, C2 are active.

B<4:2> : 101 ⇒ R0, R1, R2, R3, R4 are active.



For 01110100 :-

$B<7:5>$ : 011 ⇒ $C_0, C_1, C_2, C_3$ are active

$B<4:2>$ : 101 ⇒ $R_0, R_1, R_2, R_3, R_4$ are active