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Report for E-design 344

by

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*E-Design report # 2*

# Declaration

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# Nomenclature

## Constants

$$g = 9.81 \text{ m/s}^2$$

## Variables

$C$	Capacitance	.....	[F]
$Q$	Charge	.....	[C]
$i$	Current	.....	[A]
$P$	Power	.....	[W]
$R$	Resistance	.....	[ $\Omega$ ]
$\Theta$	Thermal resistance	.....	[ $^{\circ}\text{C}/\text{W}$ ]
$V$	Voltage	.....	[V]

## Abbreviations

BJT	.....	Bipolar Junction Transistor
MOSFET	.....	Metal Oxide Semiconductor Field Effect Transistor
AC	.....	Alternating Current
DC	.....	Direct Current
ADC	.....	Analog-to-Digital Converter
op-amp	.....	Operational Amplifier
XOR	.....	Exclusive Or Logic Gate
PWM	.....	Pulse-Width Modulation

# Chapter 1

## Signal conditioning system design

### 1.1 System overview

The TLC2272 rail-to-rail op amps were selected for all three transducers. This is due to their compact nature (2 op amps in one package as compared to the 1:1 ratio of the TL081), as well as their ability to produce output voltages much closer to the rails, which improves the resolution of the final values. Each TLC2272 op amp draws approximately 2.4[3] from the  $\pm 5V$  supplies. As the system uses 8 op-amps, as well as an XOR gate, this amounts to a draw of approximately 20 mA. This is well within the specification they were designed for.

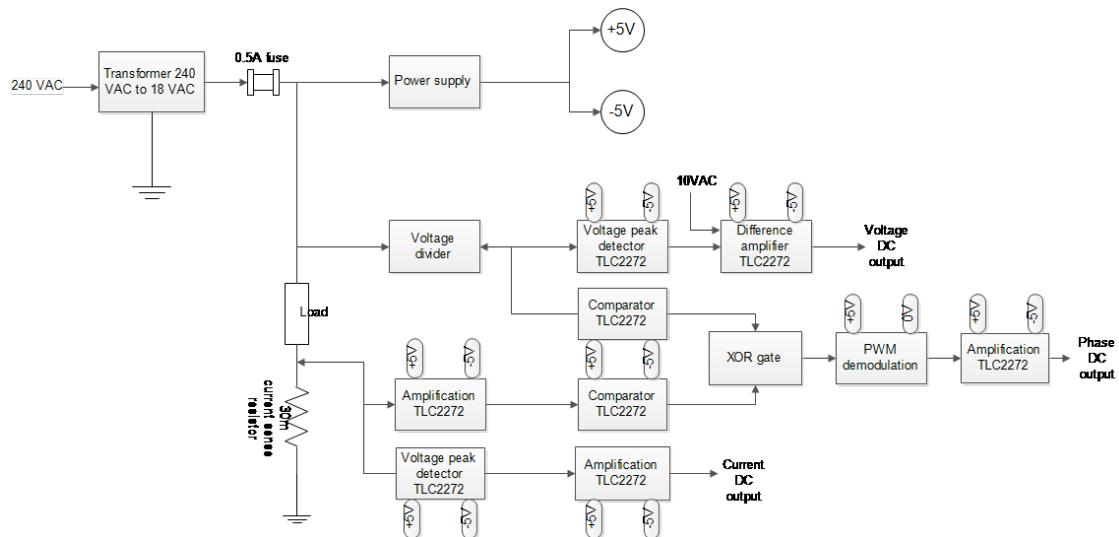


Figure 1.1: System diagram

# Chapter 2

## Voltage peak transducer

### 2.1 Theory and related work

A transducer is defined as a device that transforms one form of energy into another form[4]. AC voltage transducers convert an AC voltage signal to a DC voltage output which is directly proportional to the input signal value. For the purpose of this project, only the maximum value of the input signal is required,hence, the voltage transducer can be implemented using a peak detector circuit.

A standard peak detector usually consists of a diode and a capacitor[4]. The typical configuration is given in Figure 2.1a. This circuit, however, has the side effect of introducing a voltage drop over the diode. Having an ideal diode that avoids this is thus key to implementing a voltage transducer. This "ideal diode" configuration can be achieved by using a precision rectifier as shown in Figure 2.1b. The circuit will perform rectification, similar to a diode, but without introducing a voltage drop[5].

The DC voltage output of the transducer is to be sampled by an ADC in an Arduino Beetle board. Thus, it should be amplified to provide sufficient resolution. There are various op-amp configurations for this purpose. The main one that is considered is a difference amplifier, shown in Figure 2.1c. As the name suggests, it amplifies the difference between two inputs, one of which is usually a reference/constant signal[6].

### 2.2 Design

For the purpose of this project, two types of op-amps were provided: a standard TL081 op-amp, and a TLC2272 precision rail-to-rail op-amp. Thus, the first part of the design involves choosing which op-amp to use for each application. Table 2.1 gives some of the characteristics of both op-amps to aid in this choice.

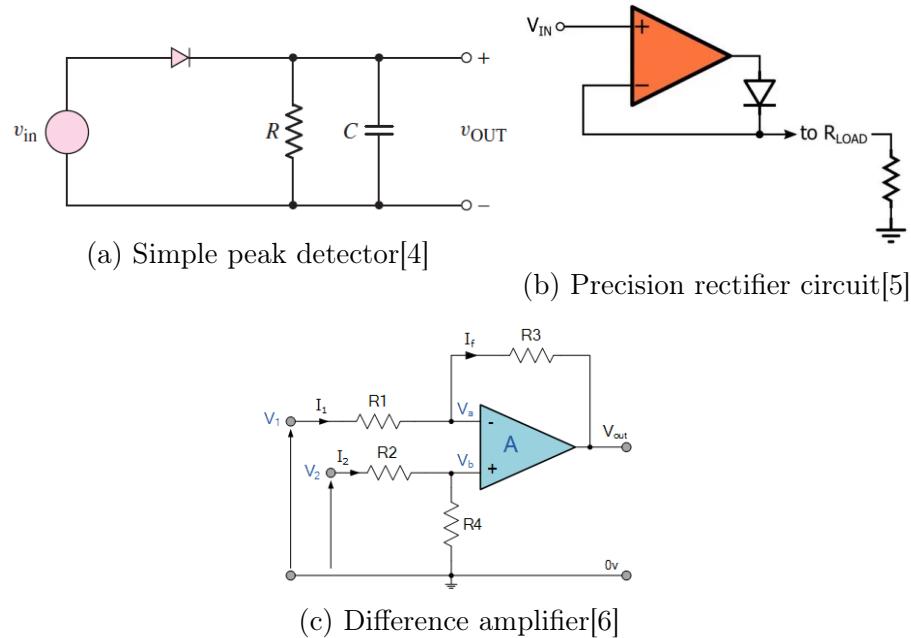


Figure 2.1: Reference circuits for a voltage transducer.

Table 2.1: TL081[2] vs TLC2272[3]

	TL081	TLC2272
Input voltage	$\pm 15$ V	-5.3 to 5.0V
Common-mode input voltage	$\pm 1.0$ V	-5.0 to 3.5V
Differential input voltage	$\pm 30$ V	$\pm 16$ V
Maximum output voltage	4.0 V	4.85V

As seen above the rail-to-rail op-amp has a higher maximum common-mode input, as well as output voltage. It also contains 2 op-amps within a single package as opposed to the TL081. For these reasons, it is chosen for all applications in the voltage transducer, as well as the current and phase shift transducers in Section 3.2 and 4.2.

Due to the common-mode specification, the voltage from the transformer must be scaled down before it is input to the precision rectifier. A voltage divider circuit is used to scale down the maximum expected 20VAC signal to a level less than the 3.5 V common-mode limit.

$$\begin{aligned}
 V_{in} &\leq \frac{R_2}{R_1 + R_2} V_{max} \\
 0.11 &\leq \frac{R_2}{R_1 + R_2} \\
 R_1 &= 22 \text{ k}\Omega \quad R_2 = 1 \text{ k}\Omega
 \end{aligned} \tag{2.1}$$

The implemented voltage divider circuit will give an output of 1.23V at 20VAC, which is also within the maximum input voltage limit. The differential voltage can also be calculated as:  $V_{d(max)} = (-1.23) - 1.23 = -2.46\text{V}$ , which is also within the op-amp limits.

A capacitor can now be chosen for the peak detector circuit. Since the transducer should be accurate to 150 mV, the maximum ripple voltage should be less than the expected change in the output for an input change of 150 mV. This is given by[4]:  $V_r = \frac{150\text{m}}{23} \times 5.6 = 36.52\text{mV}$ . As the output stage has a gain of 5.6, the peak detector ripple should be less than 6.522 mV. The capacitor can thus be chosen as:  $C = \frac{V_{pk}}{fRV_r} = 3.77 \mu\text{F}$ . However, for accuracy during sampling, the ripple should be much less than this maximum, so the capacitor is chosen to be ten times larger. Thus, a 33  $\mu\text{F}$  capacitor is chosen.

The second part of the transducer is an output amplification stage. 20VAC should be mapped to 4.5V for maximum resolution, while still leaving room for higher than expected inputs from the transformer. However, on the lower end, 12VAC would not be mapped close to zero if a non-inverting amplifier was used. To try achieve this, a difference amplifier is used. By mapping 10VAC to 0V, the resolution of the circuit is significantly reduced. Looking at the peak detector circuit, 10VAC would map to 0.615V, so, this is set as the reference to connect to the inverting input of the amplifier. To obtain this reference voltage, a voltage divider is connected to the +5V supply. Using a 1k and 10k resistor as shown, the inverting input has a voltage of 0.45V, which is close enough to the designed 10VAC. To calculate the gain of the amplifier, we consider that 1.23V must be mapped to 4.5V. With the current configuration the gain is calculated as  $4.5/(1.23-0.45) = 5.77$ . Using resistors 5.6k and 1k, a gain of 5.6 is achieved.

As a 10-bit ADC is to be used, the resolution is given as 4.883mV/bit. Reversing this to the input of the transducer gives a resolution of 20.05mV/bit. This is much less than our specified accuracy, and allows significant external noise to not affect the circuit operation.

The final voltage peak transducer is given below.

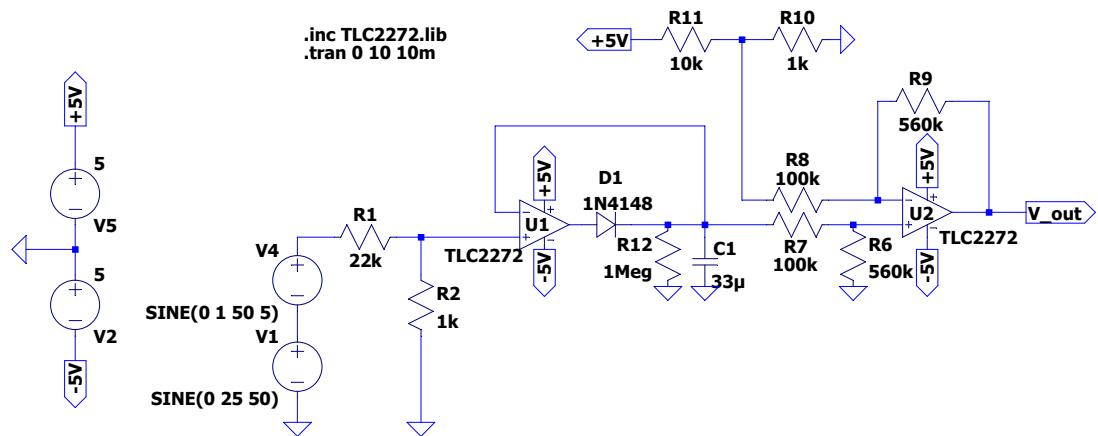


Figure 2.2: Voltage transducer circuit.

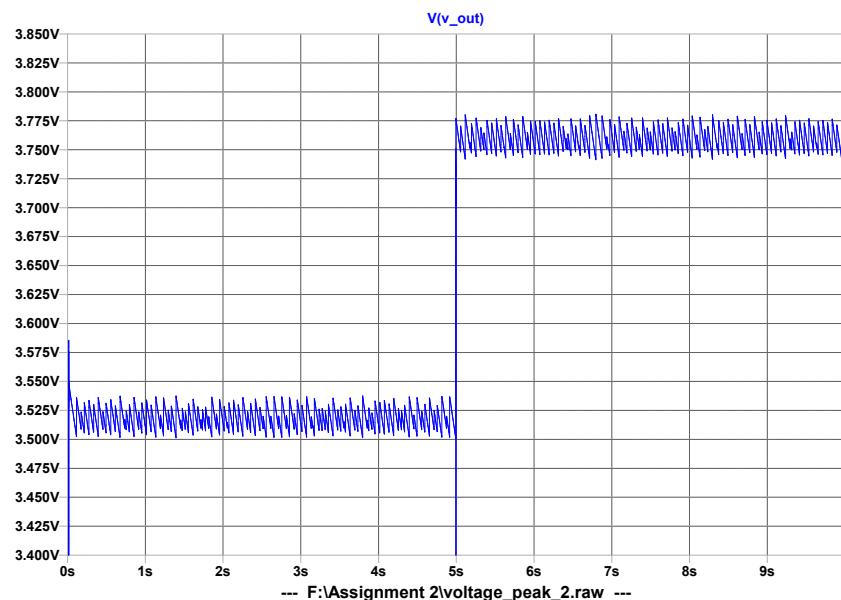
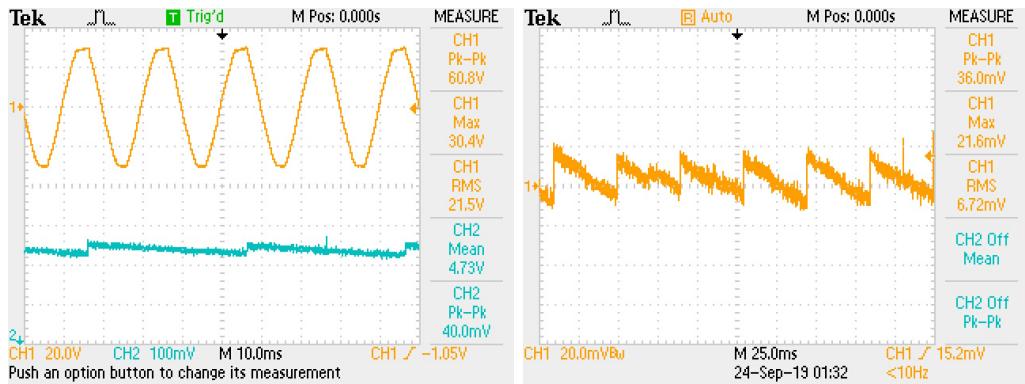


Figure 2.3: Voltage transducer circuit.



(a) AC input and DC output for mid range load.  
(b) Voltage transducer noise levels for a mid sized load.

## 2.3 Simulation

## 2.4 Measurements

The deduced input in Tables 2.2 and 2.3 is derived from the circuit in Figure 2.2.

$$V_{out} = \left( V_{in} \times \frac{1k}{1k+22k} - 5 \times \frac{1k}{1k+10k} \right) \times 5.6$$

Table 2.2: Voltage transducer unit test results

Emulated level [V <sub>peak</sub> ]	Signal generator [mV <sub>peak</sub> ]	Signal generator [mV <sub>peak</sub> ]	Analogue output [VDC]	Deduced input [V <sub>peak</sub> ]	Difference [mV]
16.00	695.65	712	1.40	16.41	409.9
21.00	913.04	932	2.65	21.3795	379.54
21.15	919.56	936	2.68	21.544	393.83
21.30	926.09	944	2.72	21.626	367.04
26.00	1130.04	1180	4.03	27.006	1.006

Table 2.3: Voltage transducer unit test results

Measurement	Load R [Ω]	Load C [μF]	Measured input [V <sub>peak</sub> ]	Analogue output [VDC]	Deduced input [V <sub>peak</sub> ]	Difference [mV]
No load	open	none	29.8	4.76	30.005	204.54
Full load	100	none	28.4	4.45	28.73	331.33
Mid range	1k	none	29.6	4.73	29.88	281.33

# Chapter 3

## Current peak transducer

### 3.1 Theory and related work

A current transducer converts the current flowing through some part of a circuit to a DC voltage output. From this definition, it is clear to see that its operation will mimic that of the voltage peak transducer implemented in Section 2.1. An AC voltage signal can be obtained by using a current sense resistor (that is small enough to have negligible effect on the voltage and current through the load). This can now serve as the input to a modified voltage transducer.

The precision rectifier shown in Figure 2.1b is used as part of a peak detector circuit. This is combined with a non-inverting amplifier, shown in Figure 3.1[1]. This reduces the gain needed for the output amplification stage. Thus, the influence of noise (especially ripple voltage) through the peak detector is minimised in the output. As this project requires the entire current input spectrum to be mapped, a standard non-inverting amplifier can be used instead of the difference amplifier previously used.

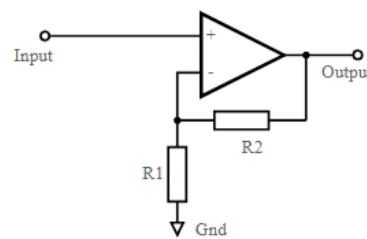


Figure 3.1: Non-inverting amplifier[1]

## 3.2 Design

The first consideration for the transducer is what size of current sense resistor to use. Two are provided: a  $5\text{ m}\Omega$  and a  $30\text{ m}\Omega$ . The larger resistor is chosen as it will provide larger input voltages for the same current, while still being much smaller than the maximum sized load ( $100\text{ }\Omega$ ).

The peak detector is designed to also amplify the input voltage peak. The gain is chosen to be large enough that the output gain stage is relatively small, but small enough as to not exceed the output op-amp limits. The maximum common-mode input is 3.5 V. Ideally, we would want the output gain to be less than 10. So:  $53.33 \leq Gain \leq 388.89$ . A gain of 181 is chosen, using  $180\text{ k}\Omega$  and  $1\text{ k}\Omega$  resistors.

With this gain, the output gain can be calculated by mapping 285 mA to 4.5 V. This gives a gain of 2.9078.  $Gain = 1 + \frac{R_2}{R_1}$  from Figure 3.1. Setting  $R_2$  as  $5.6\text{ k}\Omega$  and  $R_1$  as  $3.3\text{ k}\Omega$  gives a gain of 2.7 which is sufficient.

The capacitor value for the peak detector is chosen, as before, to produce ripple less than the change expected for accuracy of the transducer. In this case, 1 mA is required, so the capacitor is obtained as follows[4]:

$$\begin{aligned} V_r &= 1\text{ m} \times 30\text{ m} \times 181 = 5.43\text{ mV} \\ V_r &= \frac{V_{pk}}{fRC} \\ C &= \frac{285\text{ m} \times 30\text{ m} \times 181}{5.43\text{ m} \times 1M \times 50} \\ &= 5.7\text{ }\mu\text{F} \end{aligned} \tag{3.1}$$

Once again, for maximum accuracy during sampling, a capacitor ten times larger is chosen. Thus, a  $47\text{ }\mu\text{F}$  capacitor is used.

As a 10-bit ADC is to be used, the resolution is given as 4.883mV/bit. Reversing this to the input of the transducer gives a resolution of  $10\text{ }\mu\text{V}/\text{bit}$  or  $0.3334\text{ mA}/\text{bit}$ . This is less than our specified accuracy, but close enough as to affect the accuracy of the transducer.

The complete current peak transducer circuit is provided in Figure 3.2.

## 3.3 Simulation

## 3.4 Measurements

The deduced input in Tables 3.1 and 3.2 is derived from the circuit in Figure 3.2.

$$V_{out} = \left(1 + \frac{5.6k}{3.3k}\right) \times 181 \times 30\text{ m} \times I = I(14.6445)$$

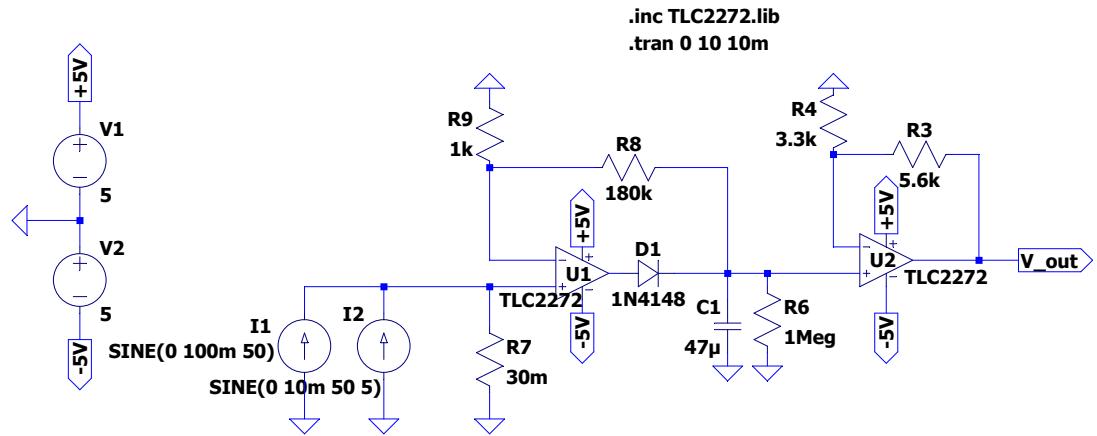


Figure 3.2: Current transducer circuit.

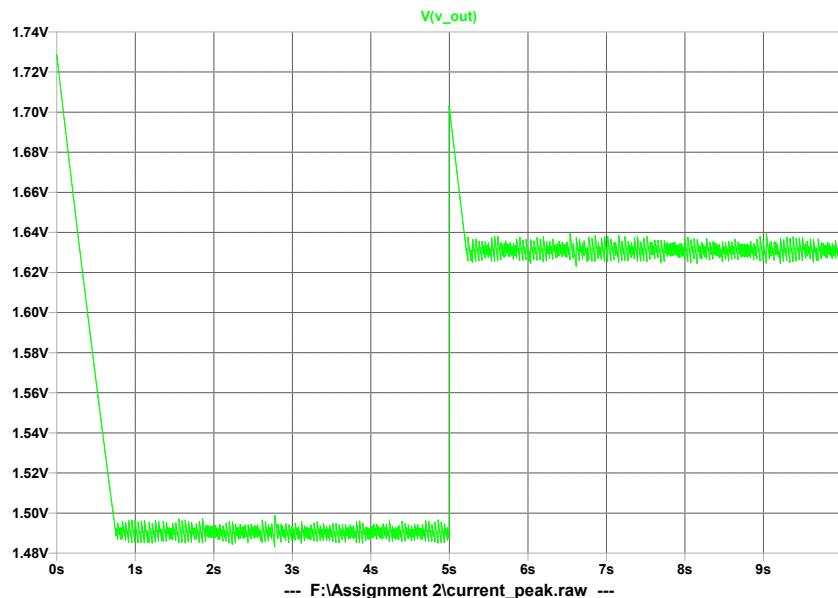
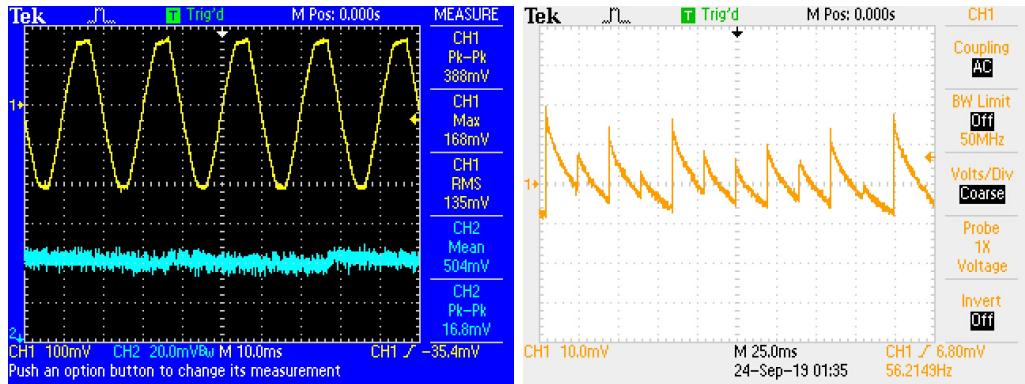


Figure 3.3: Current transducer simulation.



(a) AC input and DC output for mid range load.  
(b) Current transducer noise levels for a mid sized load.

Table 3.1: Current transducer unit test results

Emulated level [VmA <sub>peak</sub> ]	Signal generator [mV]	Signal generator [mV]	Analogue output [VDC]	Deduced input [mA <sub>peak</sub> ]	Difference [mA]
0	0	3.84	0.115	7.853	7.853
50	16.5	19.4	0.780	53.26	3.26
100	33.0	36.4	1.52	103.79	3.79
101	33.3	36.6	1.53	104.47	3.47
102	33.7	37.2	1.55	105.84	3.84
200	66.0	69.8	3.00	204.85	4.85
285	94.0	98.0	4.27	291.57	6.57

Table 3.2: Current transducer unit test results

Measurement	Load R <sub>1</sub> [Ω]	Load R <sub>2</sub> [Ω]	Measured V <sub>R</sub> [mV <sub>peak</sub> ]	Actual input [mA <sub>peak</sub> ]	Analogue output [VDC]	Deduced input [mA <sub>peak</sub> ]	Difference [mA]
No load	open	-	43.4	7.993	0.114	7.78	0.213
Full load	100	-	1620	298.34	4.35	297.04	1.30
Mid range	1k	-	199	36.648	0.499	34.074	2.574
Mid + δ	1k	24k	207	38.12	0.516	35.235	2.885
Mid + 2δ	1k	12k	215	39.595	0.538	36.737	2.858

# Chapter 4

## Phase shift transducer

### 4.1 Theory and related work

A phase shift transducer converts the phase shift between two signals to an analog DC output. For the purpose of this project, an XOR-gate based phase detector is used to implement this transducer. The presence of a phase shift between two signals introduces an equivalent time delay between them. An XOR gate produces a logical high when its two inputs have different logical states, which would occur during this time delay. The resultant output is a square signal with a duty cycle equal to the time shift between the two original signals. Thus, the width of the pulse of the output signal changes proportionally to the phase difference between the input signals and is said to be pulse-width modulated (PWM)[7]. The XOR phase detector can only be used for phase shifts of  $\pm 90^\circ$ , thus, it is sufficient for this project.

Since the input signals (voltage and current) are sinusoidally varying, they must be modified before being supplied to the XOR gate. To obtain the required digital signals, a comparator can be used. By having the same reference for both comparators, the XOR inputs will be offset by the same time delay as the sinusoidal signals as required.

However, the XOR phase detector outputs a digital signal. To convert this to an analog value, a demodulator for the PWM signal must be considered. The simplest of these is a low pass RC filter[8]. By setting the RC constant to be much larger than the PWM signal period, the filter acts as an integrator. Its output is then the average of the XOR gate output signal. The behaviour of the phase transducer can thus be described as:  $V_{out} = V_{DD} \times \frac{\Delta\Theta}{180^\circ}$  [7]

Since the range of the phase detector is up to  $180^\circ$ , the resolution may be impacted. To improve this an amplification stage is added to map  $45^\circ$  closer to the maximum range. While this would cause clipping for higher phase shifts, it is

not a major concern given this project's specifications. A standard non-inverting amplifier, as shown in Figure 3.1 can be used for this.

## 4.2 Design

The design of the transducer begins with the two comparators for the voltage and input signals. The TLC2272 op-amps are chosen for this, as they produce sufficiently high voltage, so as to be seen as a logical high by an XOR gate[9]. The reference for both is also chosen to be 0V as it is easily obtained by connecting to the ground plane. The voltage signal to the comparator must first be scaled down to be within the common-mode and input voltage limits of the op-amp. Equation 2.1 shows the ratio of the voltage divider to be used for this purpose. The same voltage divider is used for the input of the voltage comparator as it complies with the common-mode, differential and input limits as shown in Section 2.2.

For the current signal comparator, it is considered that the current sense resistor provides extremely low voltages. Some of these are even less than the op-amp's input offset voltage and would therefore affect the comparator's performance. A non-inverting amplifier is therefore designed to amplify the signal to a more usable range. An amplifier for the current signal had been designed in Section 3.2, but combined with a precision rectifier. Isolating just the amplifier gives a signal that should conform to the limits(common-mode, differential and input voltages) of the op-amp used for the comparator as previously shown.

It is however observed during simulation, that the non-inverting amplifier introduces a small DC offset, such that the amplified signal is no longer centred around 0V. So, the current comparator setup would not provide the required output. To counteract this, the amplified signal is measured and found to be centred around 54mV. The inverting input of the op-amp is thus connected to a voltage approximately equal to this by passing the +5V supply through a voltage divider circuit. Selecting a  $100\text{ k}\Omega$  and  $1\text{ k}\Omega$  resistor gives:  $V_{ref} = \frac{1\text{k}}{1\text{k}+100\text{k}} \times 5 = 49.5\text{ mV}$ . As this value may vary from op-amp to op-amp, a  $1\text{ k}\Omega$  potentiometer is chosen for the final design, so that it can be manually tuned in practice.

As the XOR gate can only handle voltages greater than  $-0.5\text{ V}$  at its input[9], the outputs of the comparator are passed through a diode before the gate. The XOR gate is then supplied with the previously designed 5V supply.

As explained before, the RC filter must have a RC constant much larger than the PWM signal period. This also has the upside of reducing the ripple voltage at its output. However, making this constant too large increases the settling time of the filter, thus, a balance between the two must be achieved. Selecting a  $1\mu\text{F}$  capacitor, the resistor can be calculated to be:  $RC > 10 \times T = 0.1$ . Thus the resistor should be larger than  $100\text{ k}\Omega$ . A  $470\text{ k}\Omega$  potentiometer is used in this place

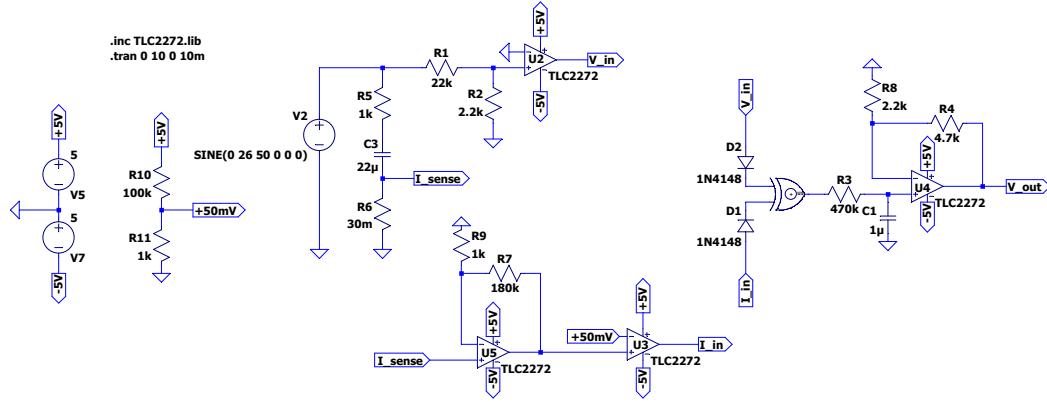


Figure 4.1: Phase shift transducer circuit.

and tuned accordingly in practice, so as to balance the above mentioned trade-off.

For the maximum specification of  $45^\circ$ , the phase detector gives an output of 1.25V. The gain of the non-inverting amplifier is chosen such that this is mapped to 4.5V, which is sufficiently close to the rails. This gives a gain of 3.6. Choosing resistors as  $5.6\text{ k}\Omega$  and  $2.2\text{ k}\Omega$  gives:  $1 + \frac{4.7k}{2.2k} = 2.14$ .

As a 10-bit ADC is to be used, the resolution is given as 4.883mV/bit. Reversing this to the input of the transducer gives a resolution of  $6.227\text{ }\mu\text{s}/\text{bit}$  or  $0.1121^\circ/\text{bit}$ .

The complete phase shift transducer circuit is given in Figure 4.1.

## 4.3 Simulation

## 4.4 Measurements

The conversion in Table 4.1 is derived from the circuit in Figure 4.1.

$$V_{out} = \left(1 + \frac{4.7k}{2.2k}\right) \times 5 \times \frac{\Delta\Theta}{180^\circ} = \Delta\Theta(0.08712)$$

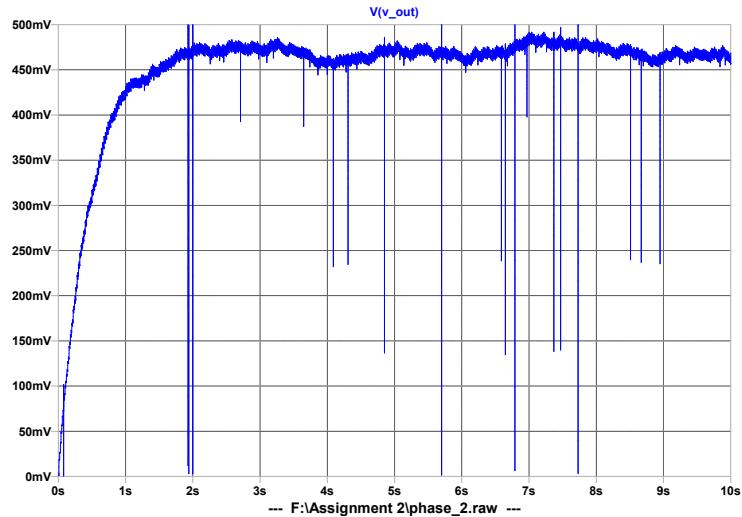
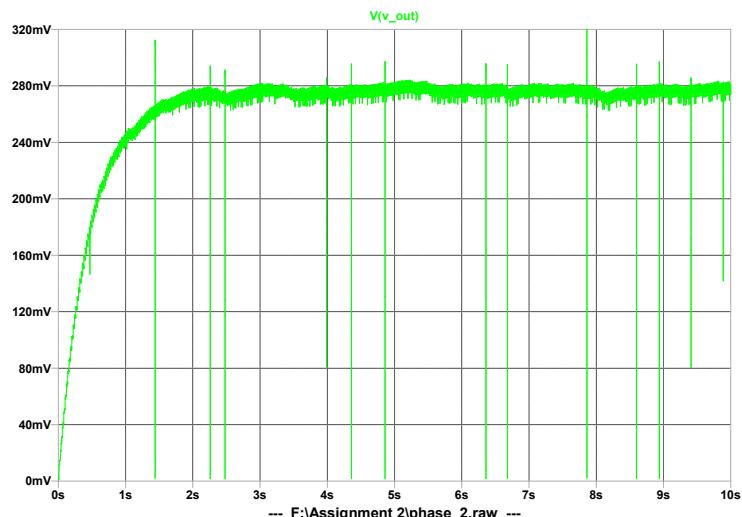
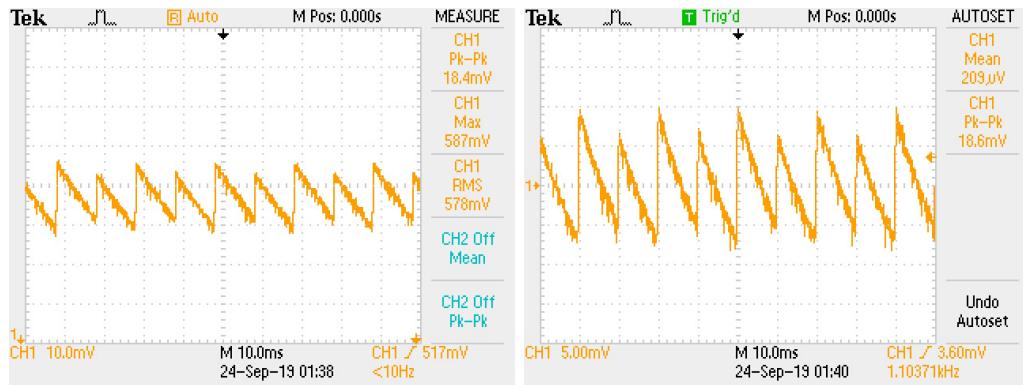
(a)  $1\text{k}\Omega$  and  $22\mu\text{F}$  load.(b)  $1\text{k}\Omega$  and  $33\mu\text{F}$  load.

Figure 4.2: Phase shift transducer simulation for nominal loads.



(a) AC input and DC output for mid range load. (b) Voltage transducer noise levels for a mid sized load.

Table 4.1: Phase shift transducer unit test results

Measurement	Load R [Ω]	Load C [μF]	Measured shift [ms]	Applied shift [°]	Analogue output [VDC]	Conversion [°]	Difference [°]
No phase shift	1k	none	0.036	0.648	0.173	1.986	1.338
Max phase shift	1k	3.3	1.92	34.56	2.834	32.53	2.03
Mid range	1k	22	0.458	8.244	0.608	6.9788	1.265
Mid + $\delta$	1k	33	0.286	5.148	0.335	3.845	1.303
Mid + $2\delta$	1k	47	0.196	3.528	0.1806	2.073	1.455

# Chapter 5

## System tests

By using a multimeter in series with both the +5V and -5V supply, it is measured that the system draws 8.38 mA from the +5V supply and 6.84 mA from the negative rail. This is lower than the estimation in Section 1.1.

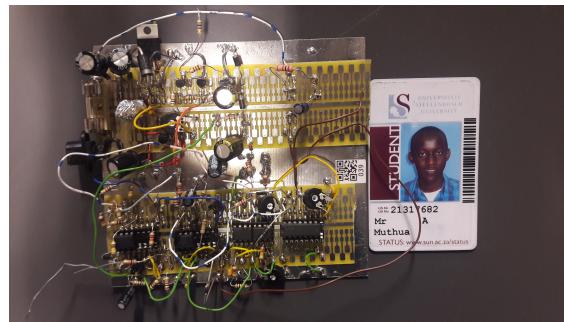
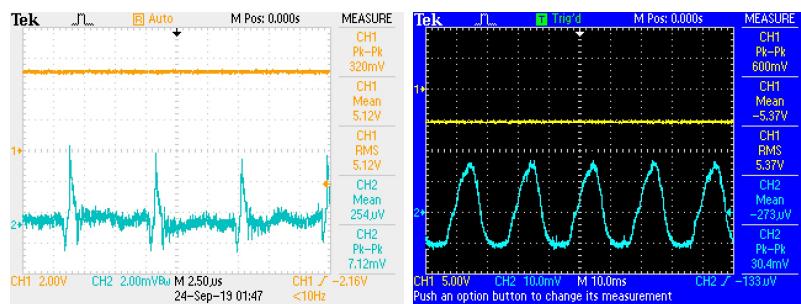


Figure 5.1: Assignment 2 PCB.



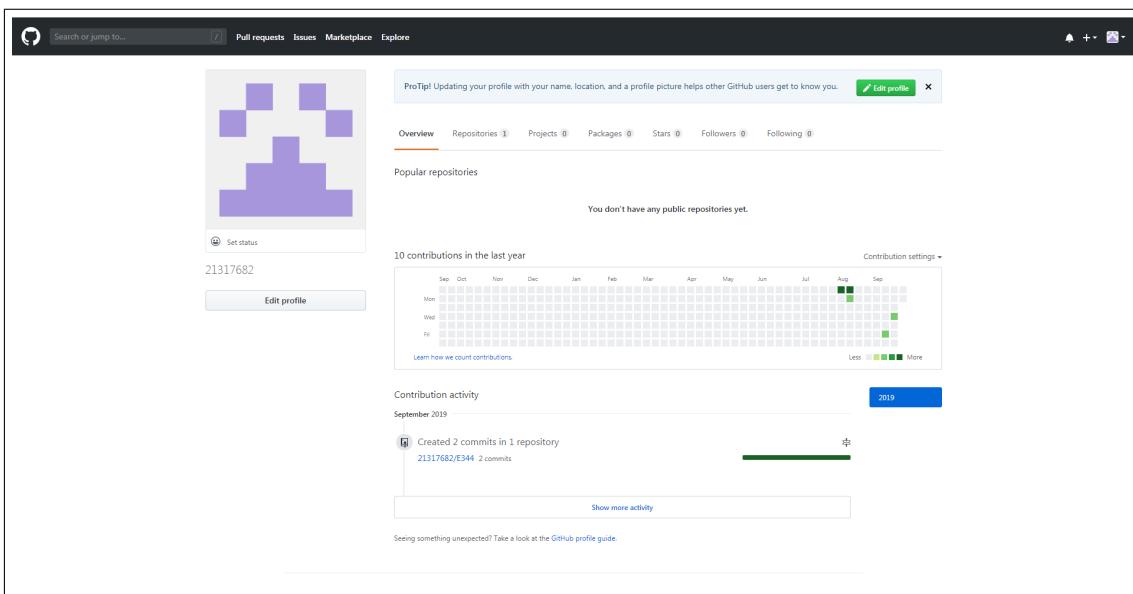
(a) +5V rail with noise level. (b) -5V rail with noise level.

Figure 5.2: Noise and rail voltages with all three systems running together.

# References

- [1] Notes, E.: Op amp non-inverting amplifier: Operational amplifier circuit. 2019.  
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# Appendix A: GitHub Activity Heatmap



## Appendix B: Stuff you want to include

## Appendix C: More stuff you want in