


Learn Git and GitHub without any code!

Using the Hello World guide, you'll start a branch, write comments, and open a pull request.

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SimonCieslar Update README.md

 History

 1 contributor

[Raw](#)[Blame](#)

142 lines (98 sloc) | 5.81 KB

Labs - 03 - Vivado

Lab assignment

1. Preparation tasks (done before the lab at home). Submit:
 - Figure or table with connection of 16 slide switches and 16 LEDs on Nexys A7 board.
2. Two-bit wide 4-to-1 multiplexer. Submit:
 - Listing of VHDL architecture from source file `mux_2bit_4to1.vhd` with syntax highlighting,

- Listing of VHDL stimulus process from testbench file `tb_mux_2bit_4to1.vhd` with syntax highlighting,
- Screenshot with simulated time waveforms; always display all inputs and outputs.

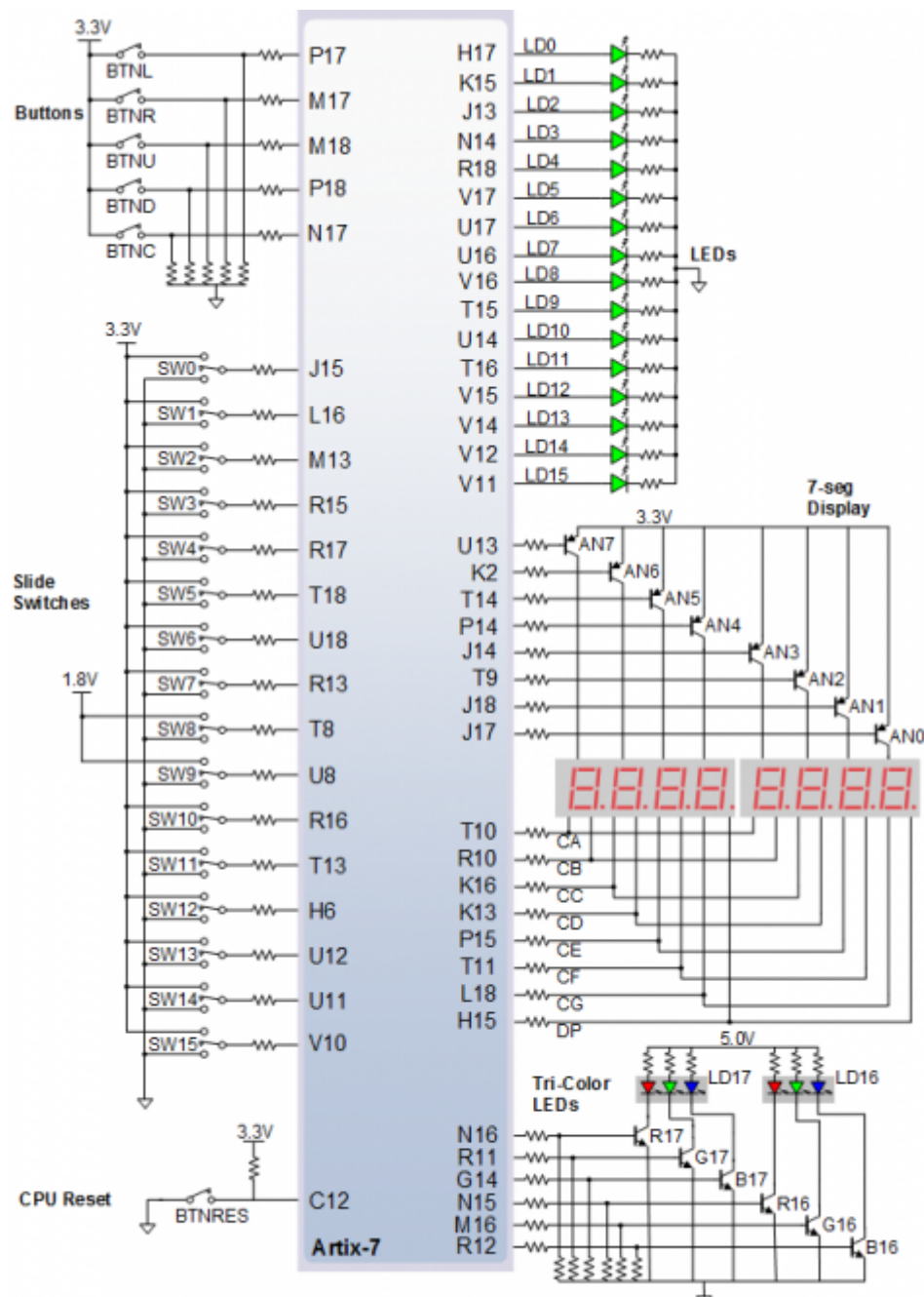
3. A Vivado tutorial. Submit:

- Your tutorial for Vivado design flow: project creation, adding source file, adding testbench file, running simulation, (adding XDC constraints file).

1. Preparation tasks (done before the lab at home).

1.1. Figure or table with connection of 16 slide switches and 16 LEDs on Nexys A7 board.

Table created from the "Nexys A7™ FPGA Board Reference Manual" and [schematic](#)



SW	SW pins	SW Connection type	****	LEDs	LED pins	SW Connection Type
1	J15	IOSTANDARD LVCMOS33		1	H17	IOSTANDARD LVCMOS33
2	L16	IOSTANDARD LVCMOS33		2	K15	IOSTANDARD LVCMOS33
3	M13	IOSTANDARD LVCMOS33		3	J13	IOSTANDARD LVCMOS33
4	R15	IOSTANDARD LVCMOS33		4	N14	IOSTANDARD LVCMOS33
5	R17	IOSTANDARD LVCMOS33		5	R18	IOSTANDARD LVCMOS33
6	T18	IOSTANDARD LVCMOS33		6	V17	IOSTANDARD LVCMOS33
7	U18	IOSTANDARD LVCMOS33		7	U17	IOSTANDARD LVCMOS33
8	R13	IOSTANDARD LVCMOS33		8	U16	IOSTANDARD LVCMOS33
9	T8	IOSTANDARD LVCMOS18		9	V16	IOSTANDARD LVCMOS33
10	U8	IOSTANDARD LVCMOS18		10	T15	IOSTANDARD LVCMOS33
11	R16	IOSTANDARD LVCMOS33		11	U14	IOSTANDARD LVCMOS33
12	T13	IOSTANDARD LVCMOS33		12	T16	IOSTANDARD LVCMOS33
13	H6	IOSTANDARD LVCMOS33		13	V15	IOSTANDARD LVCMOS33
14	U12	IOSTANDARD LVCMOS33		14	V14	IOSTANDARD LVCMOS33
15	U11	IOSTANDARD LVCMOS33		15	V12	IOSTANDARD LVCMOS33
16	V10	IOSTANDARD LVCMOS33		16	V11	IOSTANDARD LVCMOS33

2. Two-bit wide 4-to-1 multiplexer.

2.1. Listing of VHDL architecture from source file `mux_2bit_4to1.vhd` with syntax highlighting

Excerpt from `mux_2bit_4to1.vhd` :

```
architecture Behavioral of mux_2bit_4to1 is
begin
    f_o <= a_i when (sel_i = "00") else
           b_i when (sel_i = "01") else
           c_i when (sel_i = "10") else
           d_i;

end architecture Behavioral;
```

2.2. Listing of VHDL stimulus process from testbench file `tb_mux_2bit_4to1.vhd` with syntax highlighting,

Excerpt from `tb_mux_2bit_4to1.vhd` :

```
p_stimulus : process
begin
    report "Stimulus process started" severity note;

    s_d <= "00"; s_c <= "00"; s_b <= "00"; s_a <= "00";
    s_sel <= "00"; wait for 100 ns;

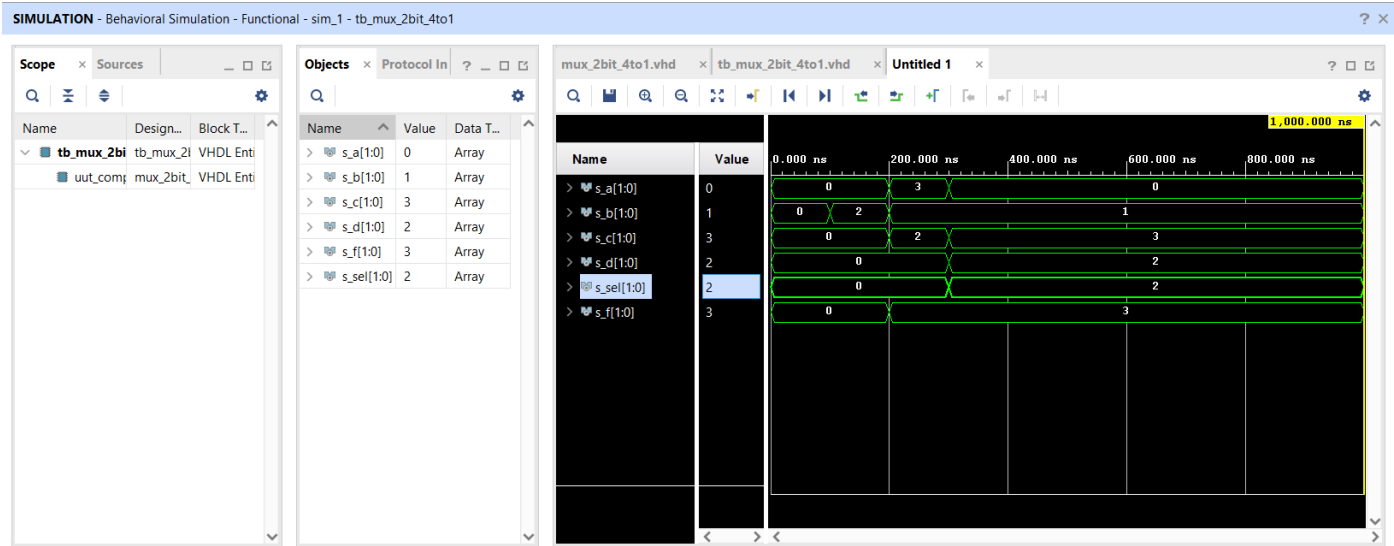
    s_d <= "00"; s_c <= "00"; s_b <= "10"; s_a <= "00";
    s_sel <= "00"; wait for 100 ns;

    s_d <= "00"; s_c <= "10"; s_b <= "01"; s_a <= "11";
    s_sel <= "00"; wait for 100 ns;

    s_d <= "10"; s_c <= "11"; s_b <= "01"; s_a <= "00";
    s_sel <= "10"; wait for 100 ns;

    report "Stimulus process finished" severity note;
    wait;
end process p_stimulus;
```

2.3. Screenshot with simulated time waveforms; always display all inputs and outputs.

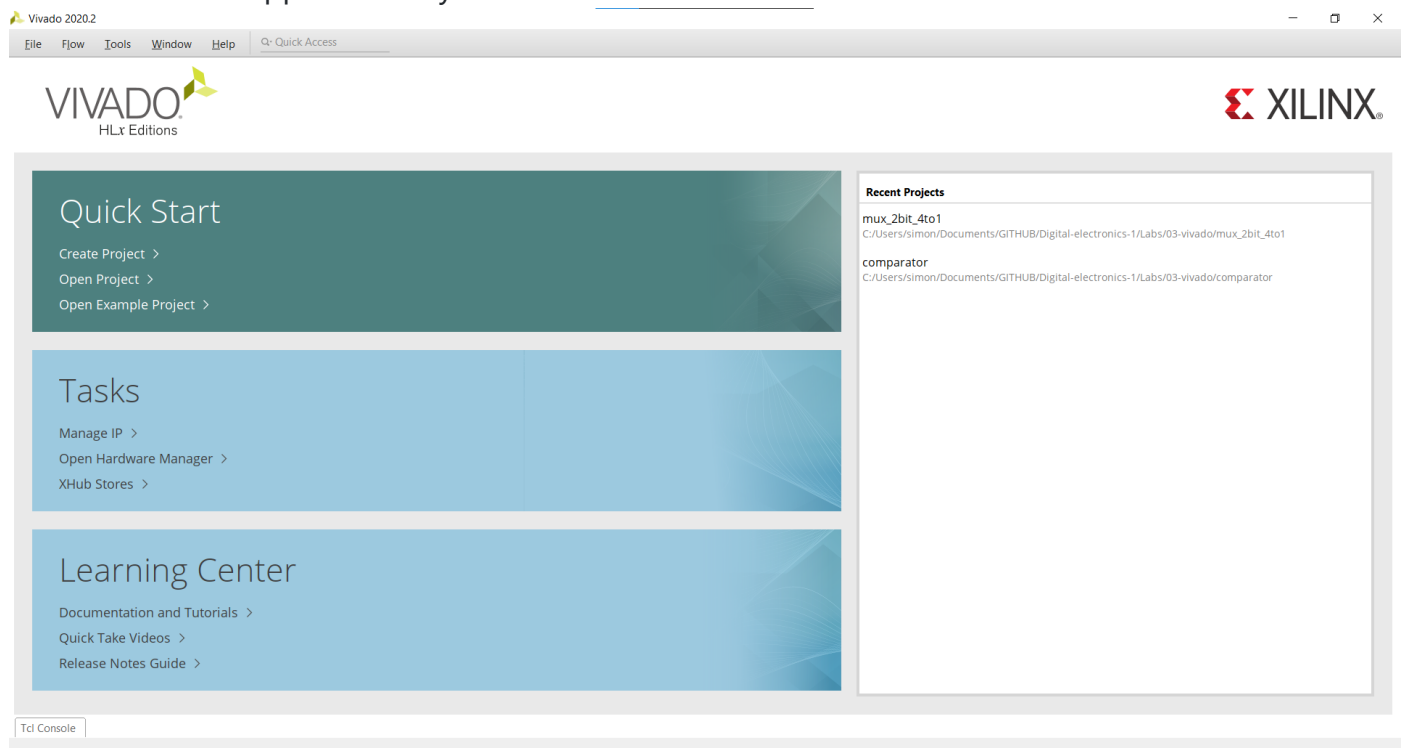


3. A Vivado tutorial.

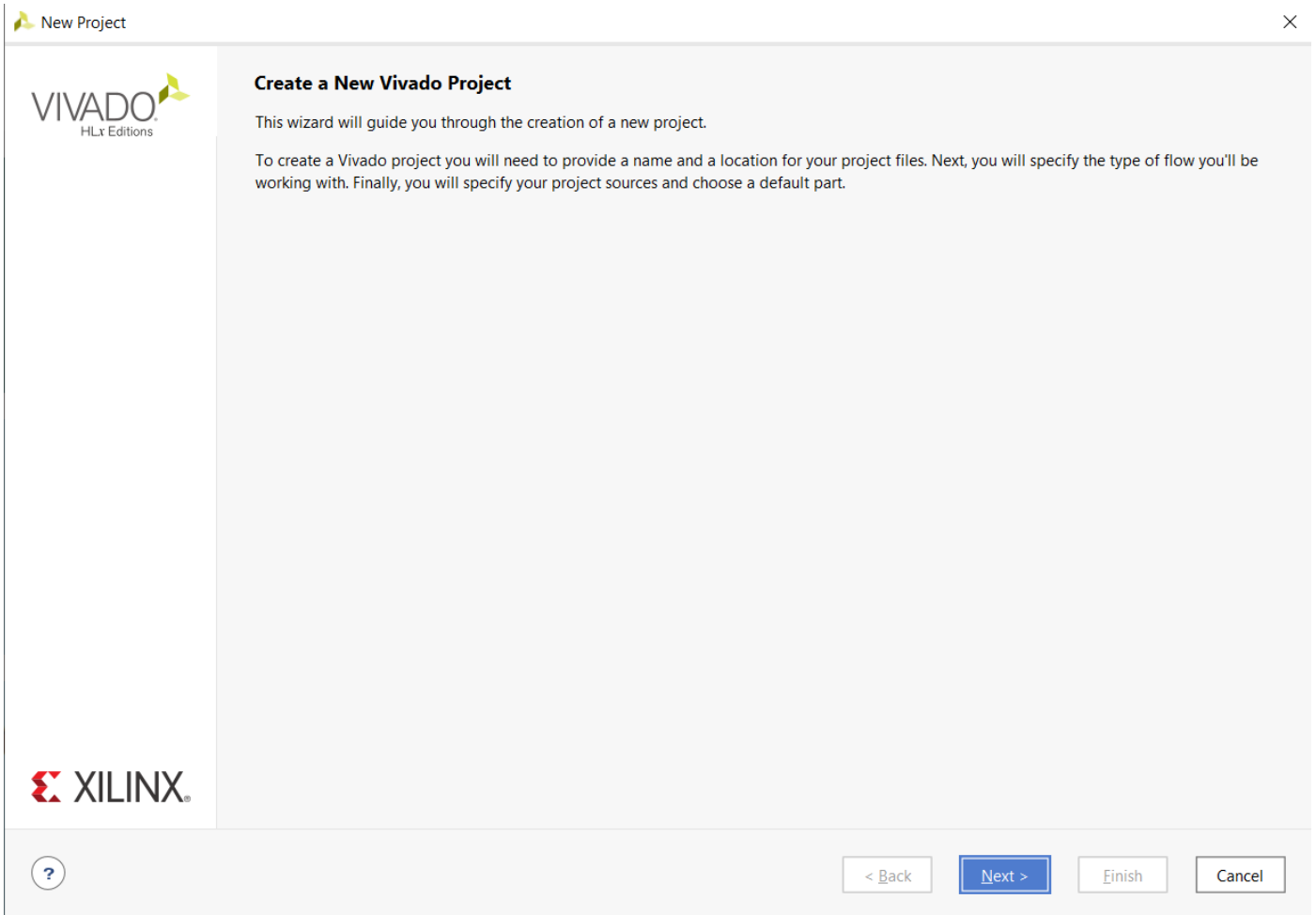
3.1. Your tutorial for Vivado design flow: project creation, adding source file, adding testbench file, running simulation, (adding XDC constraints file).

If you want to create a project in Vivado, you can try the following tutorial

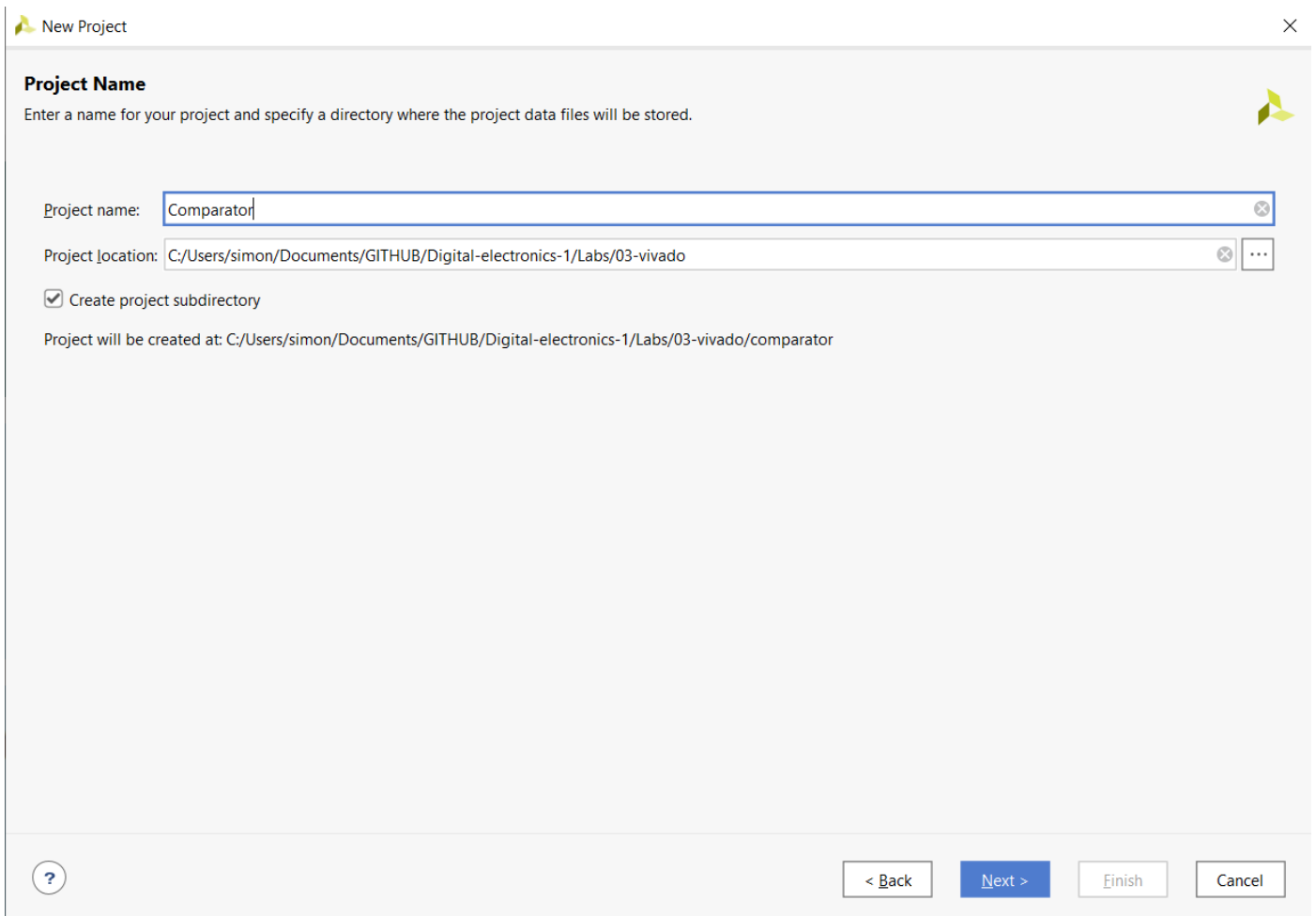
This window will appear when you start Vivado...



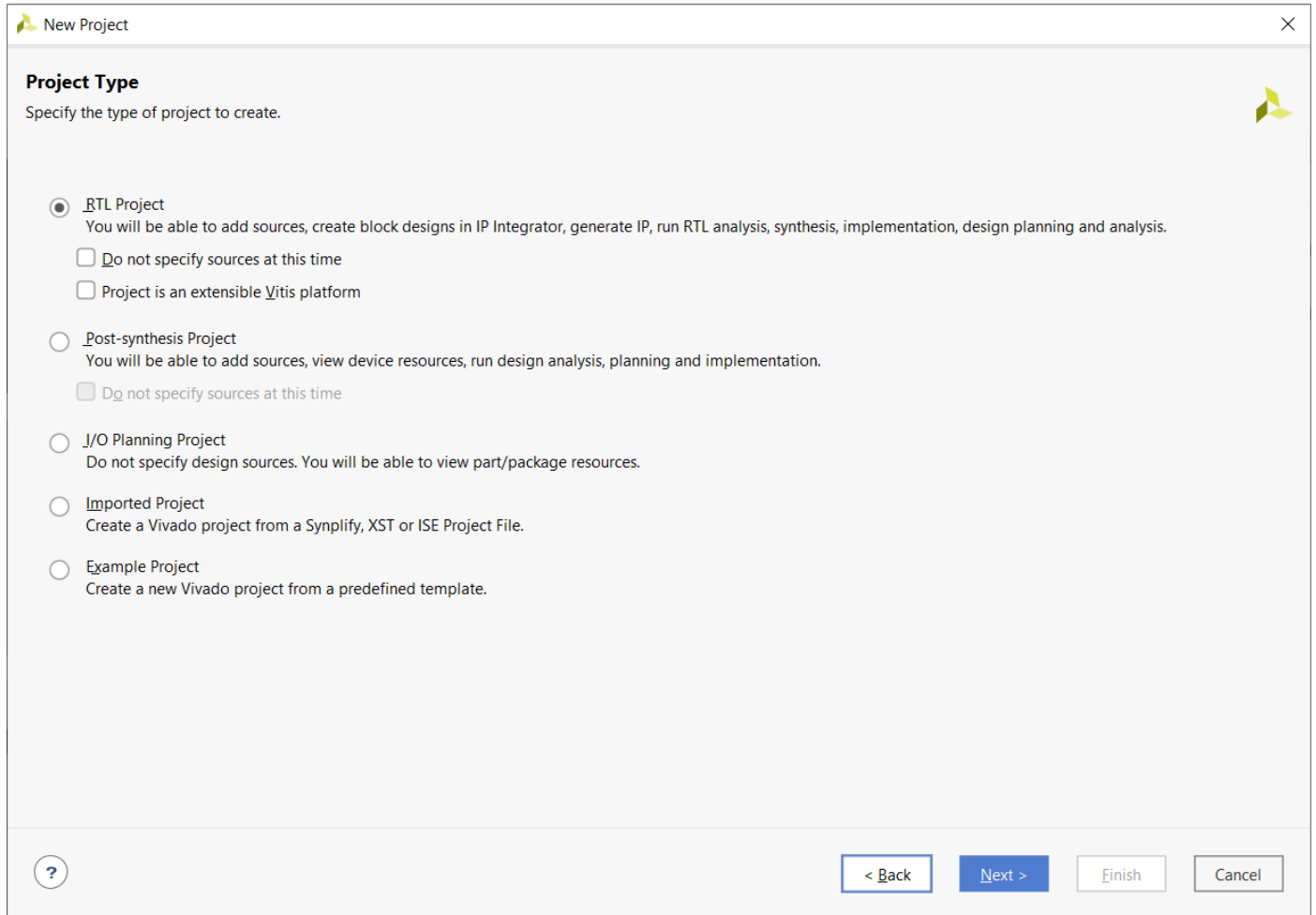
Now you can open an existing project (Open Project) or start a new one (Create Project) We will continue to create a new project (Create Project)...



Click the button **NEXT** . Now we see a window where we can name the project and set the location...



Now click again the button **NEXT** ...



New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

☐ Project is an extensible Yitis platform

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.

☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

Now we see a window called **Add Sources**. Click on **Create File** and after that to the **File name** field write **Design**. Now click **OK** after that **Next** ...

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.



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Create Source File

✕

Create a new source file and add it to your project.

File type:

VHDL

File name:

File location:

<Local to Project>

?

OK

Cancel

Add Files

Add Directories

Create File

- ☐ Scan and add RTL include files into project
- ☐ Copy sources into project
- ☒ Add sources from subdirectories

Target language:

VHDL

 Simulator language:

VHDL



Here select VHDL

< Back

Next >

Finish

Cancel

Now we see a window called **Add Constraints**. Here press **Next**. Here we use parts of old codes, so we skip...

Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.



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Use Add Files or Create File buttons below

Add Files

Create File

- ☐ Copy constraints files into project



< Back

Next >

Finish

Cancel

In the window called **Default Part** The next step is important because we choose the board for which we will create a code. We are using board Nexys A7-50T. So we select the appropriate board and continue to **Next ...**

New Project

Default Part

Choose a default Xilinx part or board for your project.

Select BOARDS

Parts | Boards

Reset All Filters

Vendor: All

Name: All

Board Rev: Latest

Install/Update Boards

Search:

Display Name	Preview	Vendor	File Version	Part	I/O Pin Count	Board Rev	Available IOBs	LUT El
Arty A7-100		digilentinc.com	1.0	xc7a100tcs324-1	324	E.0	210	63400
Arty A7-35		digilentinc.com	1.0	xc7a35tics324-1L	324	E.0	210	20800
Arty S7-25		digilentinc.com	1.0	xc7s25cs324-1	324	E.0	150	14600
Arty S7-50		digilentinc.com	1.0	xc7s50cs324-1	324	B.0	210	32600
Arty		digilentinc.com	1.1	xc7a35tics324-1L	324	C.0	210	20800

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< Back

Next >





Finish

Cancel



VIVADO
HLx Editions


XILINX

New Project Summary

-  A new RTL project named 'Comparator' will be created.
-  1 source file will be added.
-  No constraints files will be added. Use Add Sources to add them later.
-  The default part and product family for the new project:
 - Default Board: Nexys A7-50T
 - Default Part: xc7a50ticsg324-1L
 - Product: Artix-7
 - Family: Artix-7
 - Package: csg324
 - Speed Grade: -1L

To create the project, click Finish



< Back

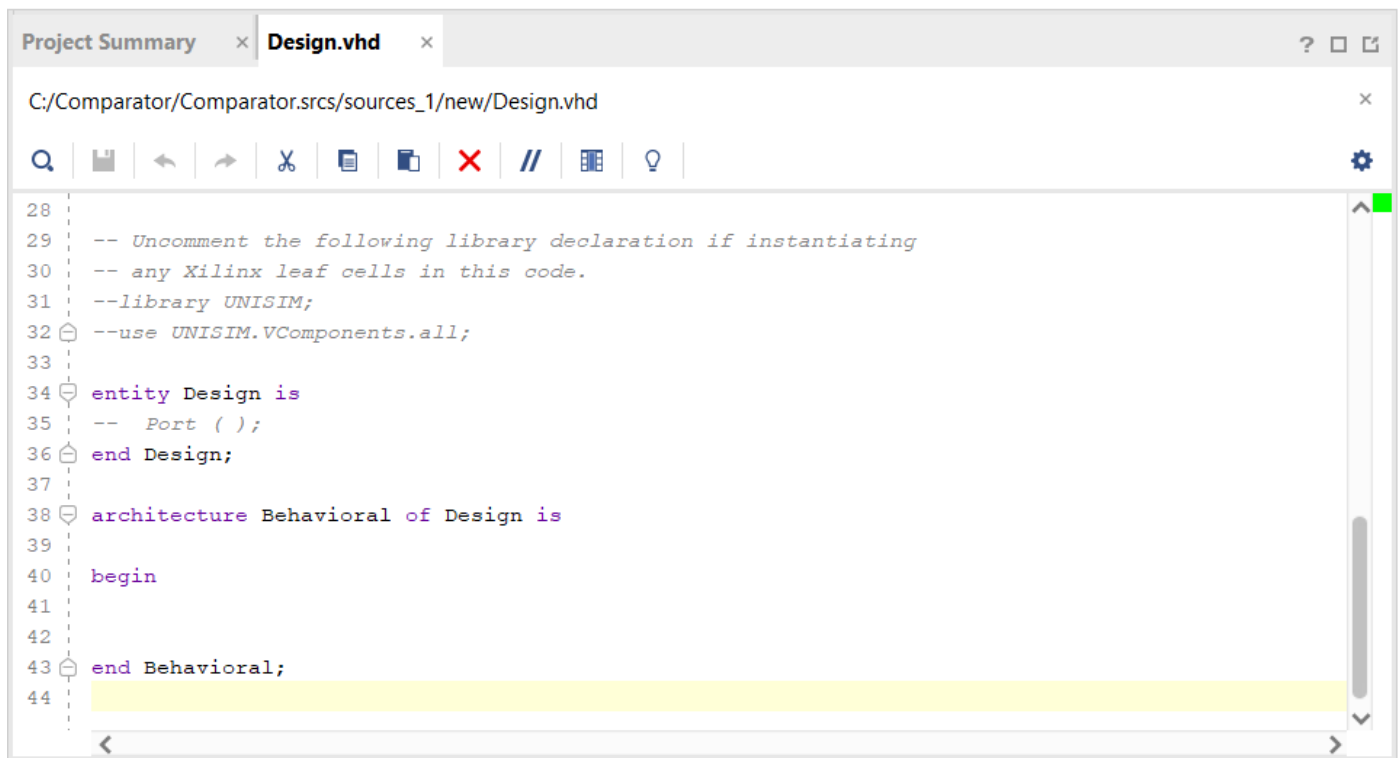
Next >

Finish

Cancel

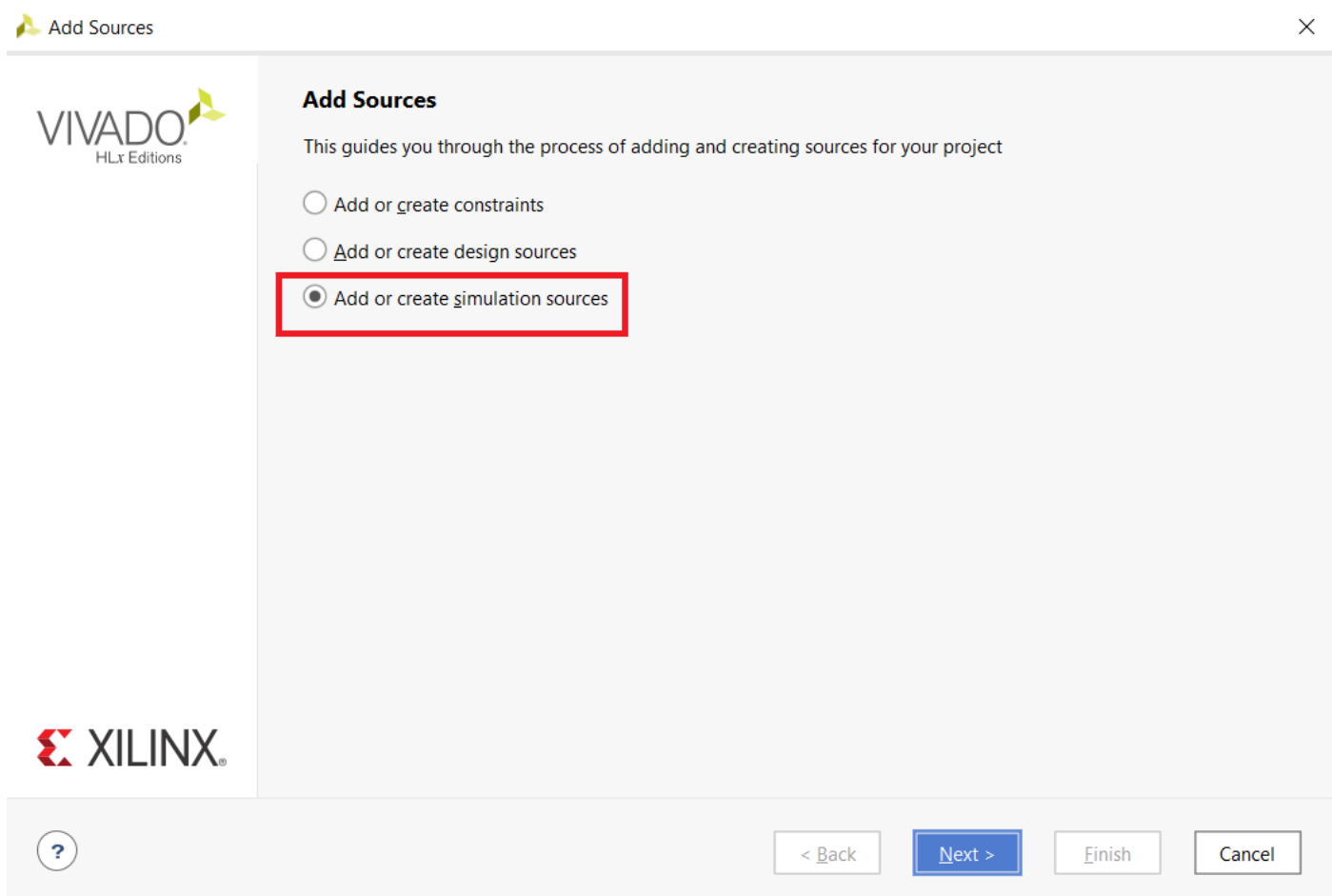
The screenshot displays the Xilinx Vivado 2020.2 IDE. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. The top status bar shows 'Ready' and 'Default Layout'. The left sidebar contains the 'Flow Navigator' with sections for PROJECT MANAGER, IP INTEGRATOR, SIMULATION, RTL ANALYSIS, SYNTHESIS, IMPLEMENTATION, and PROGRAM AND DEBUG. The main workspace is divided into several panels:

- PROJECT MANAGER - Comparator**: Shows a tree view of sources. Under 'Design Sources (1)', 'Design(Behavioral) (Design.vhd)' is selected. Below this is the 'Source File Properties' panel for 'Design.vhd', showing it is 'Enabled' and located at 'C:/Comparator/Comparator.srcs/sources_1/new'. The 'Type' is set to 'VHDL'.
- Sources**: A panel showing the source file 'Design.vhd' and its properties.
- Project Summary**: A panel with tabs for Overview, Settings, and Edit. The 'Settings' tab is active, showing project details:
 - Project name: Comparator
 - Project location: C:/Comparator
 - Product family: Artix-7
 - Project part: Nexys A7-50T (xc7a50ticsg324-1L)
 - Top module name: Design
 - Target language: VHDL
 - Simulator language: VHDL
- Board Part**: A panel showing board details:
 - Display name: Nexys A7-50T
 - Board part name: digilentinc.com:nexys-a7-50t:part0:1.0
 - Board revision: D.0
- Design Runs**: A table showing the status of design runs. The table has columns for Name, Constraints, Status, WNS, TNS, WHS, THS, TPWS, Total Power, Failed Routes, LUT, FF, BRAM, URAM, DSP, Start, Elapsed, and Run Strategy. Two runs are listed: 'synth_1' and 'impl_1', both with 'constraints_1' and 'Not started' status.



```
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity Design is
35 -- Port ( );
36 end Design;
37
38 architecture Behavioral of Design is
39
40 begin
41
42
43 end Behavioral;
44
```

For creating a file named "testbench" choose File/Add Sources . After that choose Add or create simulation sources as you can see in the picture (the process is similar to creating the Design.vhd earlier)...



Add Sources

This guides you through the process of adding and creating sources for your project

☐ Add or create constraints

☐ Add or create design sources

☒ Add or create simulation sources

VIVADO
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? < Back Next > Finish Cancel

We can start the simulation here...

Comparator - [C:/Comparator/Comparator.xpr] - Vivado 2020.2

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access Ready

Flow Navigator PROJECT MANAGER - Comparator

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG

Sources

Design Sources (1)

- Design(Behavioral) (Design.vhd)

Constraints

Simulation Sources (1)

Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

Design.vhd

Enabled

Location: C:/Comparator/Comparator.srsrcs/sources_1/new

Type: VHDL

General Properties

Design.vhd

```
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity Design is
35     port ( );
36 end Design;
37
38 architecture Behavioral of Design is
39
40 begin
41
42
43 end Behavioral;
```

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)

or you can follow this steps Flow/Run Simulation/Run Behavioral Simulation