

Home Assignment 2 Report

Problems Faced:

I encountered several challenges during this lab. I had much difficulty understanding the instructions as I felt like they were extremely vague. As someone who is working with vivado and doing system on chip design for the first time, I was not able to “read between the lines”. This was my first time working with real Verilog code as well. Although the Verilog syntax and portion of the lab were not difficult to overcome. My main issue was experiencing a lot of errors that had to do with the interface for vivado and vitis. Creating a project following all the way to publishing it on the device requires a lot of very particular steps. I had to make multiple projects to solve multiple issues. I also noticed that many of the errors are just learned. When searching online there isn’t much help as often times, issues are specific to the way you set up your design. Some of the errors I had were the black box error, incorrect output pins being mapped in the pin mapping section of my top level project, as well as receiving errors in vitis when trying to create a workspace. As I have not taken microprocessors or reconfigurable design, I was behind on the knowledge needed to understand the implementation on registers and how they can be used when designing your hardware. This made it difficult for me to complete the software portion of the project as I had to refresh and learn how to properly code and access all of the register information. I was able to connect some of the knowledge I learned from the machine intelligence lab to figure out how to make this lab work in the second portion (I worked with systemC and register level programming to program an LED light and output hello world). It was also difficult trying to figure out the resets on the hardware level. I accidentally connected my led_ctrl IP to the active low reset of the processor which led to my rsa cypher always outputting zero. I had difficulty trying to find out how to implement the rsa cypher as well because I did not know that we were supposed to include it in the led control and not implement it top level as it’s separate project. There were little things in the instructions that left gaps on guidance that caused me to take up so much time completing this project. I also ran into a problem with my pong paddle. For some reason the paddle prediction math was not calculating the correct spot due to an improper reading of the ball y position. I had to create my own software fix for this as I felt like it would have taken too much time to adjust the hardware. This taught me a valuable lesson, similar to what Muhammad spoke about in class, creating software fixes for problems are a lot faster, affordable, and easier than changing the hardware. Taking advantage of this helped me avoid little mistakes in reloading the bitstream to use an entirely different hardware setup upload for vitis.

What you learned:

Through this lab, I gained a deeper understanding of Vivado, vitis, hardware level design, the connection between peripherals and processors, as well as multiple debugging techniques. This project was very difficult for me, so it feels really good to come out on the other side and acknowledge my work.

Other:

N/A