001. The 8086 microprocessor addresses _____ bytes of memory. **A**

A 1M B 2M
C 3M D 4M

002. Which of the following instruction is not valid? **B**

A MOV AX, BX B MOV DS, 5000H
C MOV AX, 5000H D PUSH AX

003. How much memory is found in the transient program area? **A**

A 640k B 64k
C 320k D 32k

004. The instruction that is used to transfer the data from source operand to destination operand is **A**

A data copy/transfer instruction B branch instruction
C arithmetic/logical instruction D string instruction

005. Which of the following is not a data copy/transfer instruction? **C**

A MOV B PUSH
C DAS D POP

006. Operation code field is present in : **C**

A programming language instruction B assembly language instruction
C machine language instruction D none of the mentioned

007. A machine language instruction format consists of **C**

A Operand field B Operation code field
C Operation code field & operand field D none of the mentioned

008. The 8086 provides fourteen _____ bit registers. **A**

A 16 bit B 32 bit
C 64 bit D 8 bit

009. The instructions that involve various string manipulation operations are **D**

A branch instructions B flag manipulation instructions
C shift and rotate instructions D string instructions

010. The length of the one-byte instruction is **B**

A 2 bytes B 1 byte
C 3 bytes D 4 bytes

011. In which of the following addressing mode, the offset is obtained by adding displacement and contents of one of the base registers? **C**

A direct mode B register mode
C based mode D indexed mode

012. The representation of 8-bit or 16-bit signed binary operands using 2s complement is a data type of **D**

A Ordinal B ASCII
C Packed BCD D integer

013. In which of these modes, the immediate operand is included in the instruction itself? **B**

A register operand mode B immediate operand mode
C register and immediate operand mode D none of the mentioned

014. The length of the one-byte instruction is **B**

A 2 bytes B 1 byte
C 3 bytes D 4 bytes

015. In a machine instruction format, S-bit is the **C**

A status bit B sign bit
C sign extension bit D none of the mentioned

016. The feature of separated caches is **D**

A supports the superscalar organization B high bandwidth
C low hit ratio D all of the mentioned

017. The instruction or segment that executes the floating point square root instructions is **C**

A floating point square root segment B floating point division and square root

segment

C floating point divider segment D none of the mentioned

018. The stage in which the CPU generates an address for data memory references in this stage is **C**

A prefetch stage B D1 (first decode) stage

C D2 (second decode) stage D execution stage

019. The stage in which the CPU fetches the instructions from the instruction cache in superscalar organization is **A**

A Prefetch stage B D1 (first decode) stage

C D2 (second decode) stage D Final stage

020. In the execution stage the function performed is **D**

A CPU accesses data cache B executes arithmetic/logic computations

C executes floating point operations in execution unit D all of the mentioned

021. The statement that is true for the instruction POP*A is **D**

A flags are unaffected B no operands are required

C exceptions generated are same as that of PUSH*A D all of the mentioned

022. While executing the PUSH*A instruction, the stack pointer is decremented by **B**

A 1 bit B 2 bits

C 4 bits D 16 bits

023. The instruction that represents the rotate source, count is **D**

A RCL B RCR

C ROR D All of the mentioned

024. Which of the following is a floating point exception that is generated in case of integer arithmetic? **D**

A divide by zero B overflow

C denormal operand D all of the mentioned

025. The fifth stage of pipeline is also known as **C**

A read back stage B read forward stage

C write back stage D none of the mentioned

026. The size of a general purpose floating point register of floating point unit is **D**

A 4 bytes B 40 bytes

C 8 bytes D 80 bits

027. The multimedia applications mainly require the architecture of **C**

A single instruction stream single data stream B multiple instruction stream single data stream

C single instruction stream multiple data stream D multiple instruction stream multiple data stream

028. The instruction that is used to exit the procedure is **C**

A QUIT B STOP

C LEAVE D EXIT

029. The instruction that multiplies the content of AL with a signed immediate operand is **C**

A MUL B SMUL

C IMUL D None of the mentioned

030. In which of the following addressing mode, the offset is obtained by adding displacement, with the contents of SI? **D**

A direct mode B register mode

C based mode D indexed mode

031. The micro process or can read/write16bitdatafromor to **A**

A memory B I /O device

C processor D register

032. In 8086 microprocessor, the address bus is bit wide **D**

A 12bit B 10bit
C 16bit D 20bit

033. The purpose of the microprocessor is to control **A**

A memory B switches
C processing D tasks

034. A micro processor is a chip integrating all the functions of a CPU of a computer. **B**

A multiple B single
C double D triple

035. In Rotate source, count instructions, if the CF is equal to MSB of operand (source) then **B**

A TF is cleared B OF is cleared
C TF is set D OF is set

036. TheSFiscalledas **B**

A serviceflag B sign flag
C single flag D condition flag

037. TheOFiscalledas **A**

A overflow flag B overdue flag
C one flag D over flag

038. The instruction that affects the flags is **A**

A IMUL B INSW
C INSB D POP*A

039. The 16 bit flag of 8086 microprocessor is responsible to indicate **A**

A The condition of result of ALU operation B The condition of memory
C The result of addition D The result of subtraction

040. The CFisknownas **A**

A carryflag B condition flag
C common flag D single flag

041. In Harvard machine instruction sand data are present in_____ memory. **B**

A Same RAM B Separate RAM
C Both D None

042. LowLevelLanguagescanbeunderstoodby **C**

A Users B Lay Men
C Machine D None

043. In V on Neumann machine instruction sand data are present in _____memory. **A**

A Same RAM B Separate RAMs
C both D None

044. SystemBusisCollectionof lines. **D**

A Address Bus B Control Bus
C Data Bus D All

045. System software is considered a sinter face between (i)H/W (ii)S/W (iii) User Applications **B**

A (i)(ii) B (i)(iii)
C (ii)(iii) D All

046. If there are 8 address lines then the number of memory locations in the memory are _____ **B**

A 8 B 256
C 128 D 64

047. A 4GB memory with 8bit data lines has _____ address lines **A**

A 32 B 64
C 22 D 12

048. If there are 8 data lines then the size of Data Bus is **A**

A 8 B 16
C 24 D None

049. _____is concerned with the structure and behavior of the computer as seen by **A**

user.

A Computer Architecture B Computer Organization
C Computer Design D None of these

050. In WRITE control signal data transfer is between _____ and_____. **C**
A Memory , CPU B Memory , I/O
C CPU , Memory D I/O , Memory

051. In 1960s Texas institute invented **A**
A Integrated circuits B Microprocessors
C Vacuum tubes D Transistors

052. The intel 8086 Microprocessor is a _____ Processor **B**
A 8-bit B 16 -bit
C 32-bit D 4-bit

053. CPU consists of the following Functional Units: **C**
A CU B ALU
C Both D None

054. During the execution of a program which gets initialized first? **C**
A MDR B IR
C PC D MAR

055. The main advantage of multiple bus organization over single bus is, **A**
A Reduction in the number of cycles for execution B Increase in size of the registers
C Better Connectivity D None of these

056. The BP is indicated by **C**
A binary pointer B bit pointer
C base pointer D digital pointer

057. The index register is used to hold **A**
A Memory register B Offset register
C Segment memory D Offset memory

058. The 16-bit flag of microprocessor is responsible to indicate **B**
A The condition of memory B The condition of result of ALU operation
C The result of subtraction D The result of addition

059. In 8086 Microprocessor, the address bus is _____ bit wide **D**
A 12 B 10
C 16 D 20

060. The work of EU **B**
A Encoding B decoding
C Processing D calculations

061. The _____translates a byte from one code to another code **A**
A XLAT B XCHNG
C POP D PUSH

062. The 8086 fetches instruction one after another from _____ of memory **A**
A codesegment B IP
C ES D SS

063. JS is called as **A**
A Jump the signed bit B Jump single bit
C Jump simple bit D Jump signal it

064. The push source copies a word from source to _____ **A**
A Stack B Memory
C Destination D register

065. LDs copies to consecutive words from memory to register and _____ **B**
A ES B DS
C SS D CS

066. The extension that is essential for every assembly level program is **C**

A ASP B ALP
C ASM D PGM

067. The extension file that is must for a file to be accepted by the LINK as a valid object file is **A**

A OBJ file B EXE file
C MASM file D DEBUG file

068. The result of MOV AL, 65 is to store **B**

A Store 0100 0010 in AL B Store 0100 0001 in AL
C Store 40 H in AL D Store 44 H in AL

069. isusedtowriteinto memory **B**

A RD B WR
C RD/WR D CLK

070. Address line for TRAP is **B**

A 0023H B 0024 H
C 0033H D 0044 H

071. In case of string instructions, the NMI interrupt will be served only after **C**

A initialisation of string B execution of some part of the string
C complete string is manipulated D the occurrence of the interrupt

072. The INTR signal can be masked by resetting the **B**

A TRAP flag B INTERRUPT flag
C MASK flag D DIRECTION flag

073. The process of storing the data in the stack is called the stack. **C**

A pulling into B pulling out
C pushing into D popping into

074. As the storing of data words onto the stack is increased, the stack pointer is **D**

A incremented by 1 B decremented by 1
C incremented by 2 D decremented by 2

075. While retrieving data from the stack, the stack pointer is **B**

A incremented by 1 B incremented by 2
C decremented by 1 D decremented by 2

076. Which of the following instruction is not valid **B**

A MOV AX, BX B MOV DS, 5000H
C MOV AX, 5000H D PUSH AX

077. The instruction that puses the contents of the specified register/memory location on to the stack is **C**

A PUSH F B POP F
C PUSH D POP

078. Assembly language programs are written using **B**

A Hex code B Mnenonics
C ASCII Code D None of the above

079. If the pin LOCK (active low based) is low at the trailing edge of the first ALE pulse, then till the start of the next machine cycle, the pin LOCK (active low) is **A**

A Low B High
C low or high D none of the mentioned

080. To estimate the size of an executable program before it is assembled and linked, the programming methodology concerned is by writing **D**

A programs with more than one segment for data and code
B programs with FAR subroutines each of size up to 64KB
C programs with more than one segment for stack
D all of the mentioned

081. Among the five interrupts generated by 8051, the lowest priority is given to the interrupt **D**

A IE0 B TF1
C TF0 D RI

082. The instruction, MOV AX, 1234H is an example of **C**

A register addressing mode B direct addressing mode
C immediate addressing mode D based indexed addressing mode

083. The timer generates an interrupt, if the count value reaches to **D**
A 00FFH B FF00H
C 0FFFH D FFFFH

084. Which of the following is not an addressing mode of 8051? **D**
A register instructions B register specific instructions
C indexed addressing D none

085. The instruction, RLA performs **B**
A rotation of address register to left B rotation of accumulator to left
C rotation of address register to right D rotation of accumulator to right

086. Both the CISC and RISC architectures have been developed to reduce the _____ **C**
A Cost B Time delay
C Semantic gap D All of the mentioned

087. The _____ directive is used to allocate 4 bytes of memory. **A**
A DD B ALLOC
C RESERVE D SPACE

088. The computer architecture aimed at reducing the time of execution of instructions is _____ **B**
A CISC B RISC
C ISA D ANNA

089. In8086theoverflowflagissetwhen . **B**
A thesumismorethan16bits. B signednumbersgooutoftheirrangeafter anarithmeticoperation.
C carryandsign flagsareset. D subtraction

090. The Sun micro systems processors usually follow _____ architecture. **D**
A CISC B ISA
C ULTRA SPARC D RISC

091. 8086 microprocessor is interfaced to 8253 a programmable interval timer.Themaximum number by which the clock frequency on one of the timers is dividedby **A**
A 2^{16} B 2^{8}
C 2^{10} D 2^{20}

092. ForthemostStaticRAMthemaximumaccesstimeisabout **C**
A 1ns B 10ns
C 100ns D 1s

093. 8086 is interfaced to two 8259s (Programmable interrupt controllers). If 8259sare in master slave configuration the number of interrupts available to the 8086microprocessoris **D**
A 8 B 16
C 15 D 64

094. Which of the following statements regarding Stacks is/are True? i) The stack always grows towards higher addresses ii) The stack always grows towards lower addresses iii) The stack has a fixed size iv) The width of the stack is 32 bits **C**
A i and iii B i and iv
C ii and iv D iii and iv

095. The MMX (Multimedia Extension) operands are stored in _____ **C**
A General purpose registers B Banked registers
C Float point registers D Graphic registers

096. Which of the following sequence that a microprocessor follows? **A**
A Fetch, decode, execute B Fetch, execute, decode
C Decode, fetch, execute D Execute, Decode,etch,

097. How many months does it take for a microprocessor to build? **B**
A 1 B 2
C 3 D 4

098. Which of the following statement is related to the register array? **C**

A It consists of an accumulator
B It consist of registers like B, C, D, E, H, L
C Both a and b
D None of the above

099. What is the purpose of zero flags in the 8086 processor? **D**

A Checks the arithmetic operation
B Checks the logical operation
C Includes bitwise logical instructions
D Both a and c

100. The directive that directs the assembler to start the memory allotment for a particular segment/block/code from the declared address is **C**

A OFFSET
B LABEL
C ORG
D GROUP