Binary to Gray Code Converter by using QCA

Submitted By

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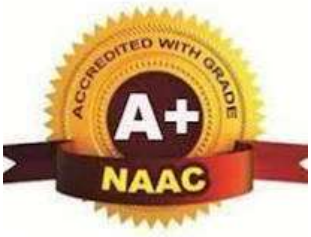

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DECLARATION

This is to certify that the work reported in the present project entitled

"Implementation of Binary to Gray Code Converter in Quantum Dot Cellular Automata"

is a record of work done by us in the Department of **ELECTRONICS AND COMMUNICATION ENGINEERING ECE (A SEC)**, CMR Institute of Technology , Hyderabad. We submit our project for further development by any interested students who share similar interests to improve the project in the future.

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Implementation of Binary to Gray Code Converter in Quantum Dot Cellular Automata

Abstract Quantum dot cellular automaton (QCA) are dominant nanotechnology which has been used extensively in digital circuits and systems. It is a promising alternative to complementary metal–oxide–semiconductor (CMOS) technology with many enticing features such as high-speed, low power consumption and higher switching frequency than transistor based technology. The code converters are the basic unit for transformation of data to execute arithmetic processes. In this paper, QCA based 2-bit binary-togray; 3-bit binary-to-gray and 4-bit binary-to-gray code converter have been proposed. The proposed design reduces the number of cells, area and raises switching speed. The simulations are completed using QCADesigner and Microwindlite tool which is widely used for simulation and verification.

Keywords: Binary to Gray Converter; Quantum Dot Cellular Automata; Gray Code; QCA cell.

1. **INTRODUCTION QCA** is an advanced access towards the modern era of nanotechnology and an alternative of CMOS technology [1] and offers a new designing procedure which is relevant for logic gates. Physical limits of CMOS such as quantum effects and technological limits like power dissipation; momentum of microelectronics using regular circuit scaling [2]. QCA is an emerging technology which allows operating frequencies in range of THz [3] that is not achievable in current CMOS technologies. Conversion circuit embedded between two structures if each uses different codes for the same information. A code converter is a combinational circuit which generates two structures consistent even each uses distinct binary code.
   In this paper we have designed and implemented a 2-bit binary-to-gray, 3-bit binary-to-gray and 4-bit binary-to-gray code converter in QCA technology. We implement the binary to gray converter in an efficient way using less number of cell and area.

2. **FUNDAMENTAL** OF QCA The principal unit of QCA structure is QCA cell and it consists of two electrons with four quantum dots positioned at the vertices of a squared cell [4-6]. Electrons can shift to different quantum dots by means of electron tunneling. The electrons are forced to the corner area to expand their separation due to Coulomb repulsion. The state of a cell is called its polarization. The identical energetically nominal arrangements of the two electrons in the QCA cell, as shown in Figure 1. These two stable arrangements of electrons are denoted as cell polarization P= + 1.00 and P = –1.00. By using cell polarization P = + 1.00 to represent logic “1” and P = –1.00 to represent logic “0”, binary data is encoded in the charge composition of the QCA cell [7, 8]

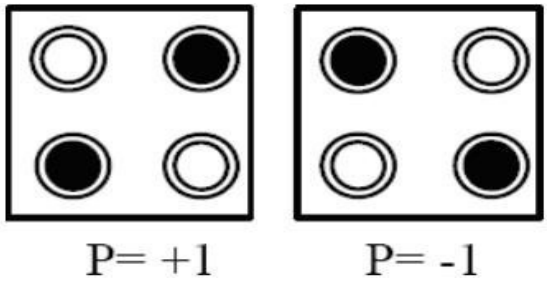


Figure 1: Structure of a basic QCA cell. A number of QCA combinational [1, 5, 9-22], sequential [23-32] and reversible logic [33-40] circuit have been proposed in recent years based on two cell inverters and three input majority voter elements [10, 17, 41, 42]. Elemental structures for QCA are the inverter and the majority gate. The elemental blocks of QCA logic involve a QCA wire, QCA inverter and QCA majority gate.

2.1 QCA wire QCA wire is a bundle of interconnecting cells that are used to transfer polarization state. QCA wire can be made up of 45o cells or 90o cells shown in figure 2 respectively. The formal arrangement of QCA cells patterns a binary wire. For the electrostatic communications between the cells the signal propagates from one end to another. For a 45o QCA wire the propagation of the signal must be alternates between the two polarizations [43].

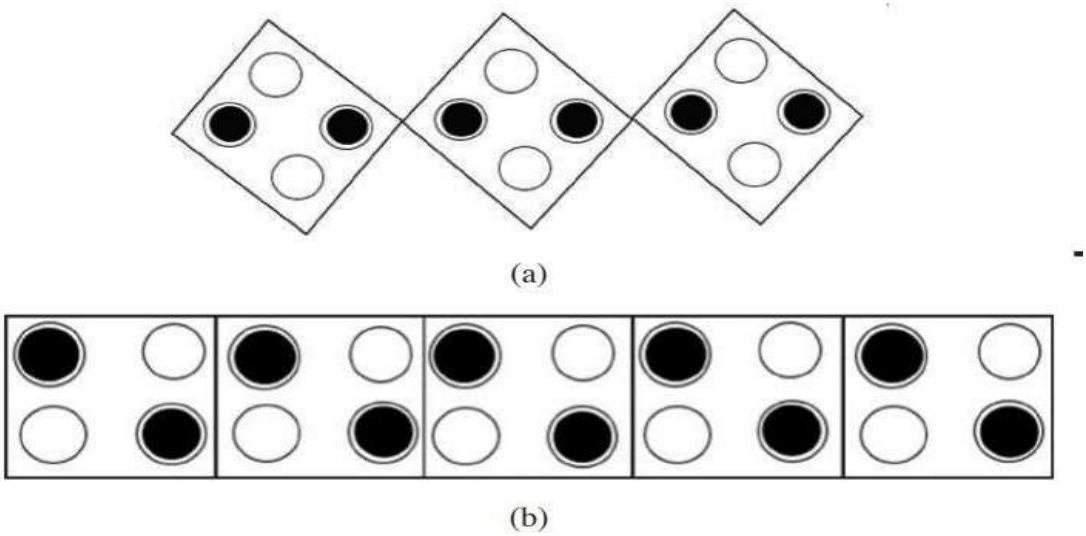


Figure 2: QCA (a) 45° wire (b) 90° wire.

2.2. QCA inverter QCA inverter is generally composed by placing the cells with only their edges contacts. This aspect is employed to forge an inverter as shown in Figure 3. QCA inverter returns the reversed value of the input value.

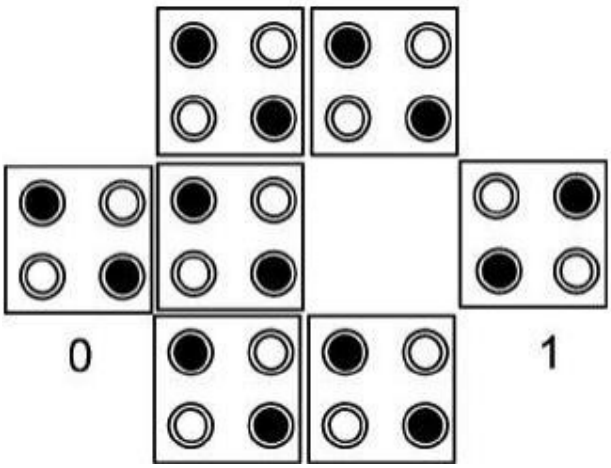


Figure 3: QCA inverter.

2.3 Majority voter (MV) The MV has four terminal cells. Among these terminals three are defining as input terminal cells and resting one defining as output cell. Majority Gate [44] is expressed as logic function MV (A, B, C) = AB + BC + AC.

To produce well-organized QCA design, the digital circuits are implemented with the help of majority gate-based design techniques are needed [45]. Logical AND gate and OR gate can be realized from the majority gate as shown in Figure 4.

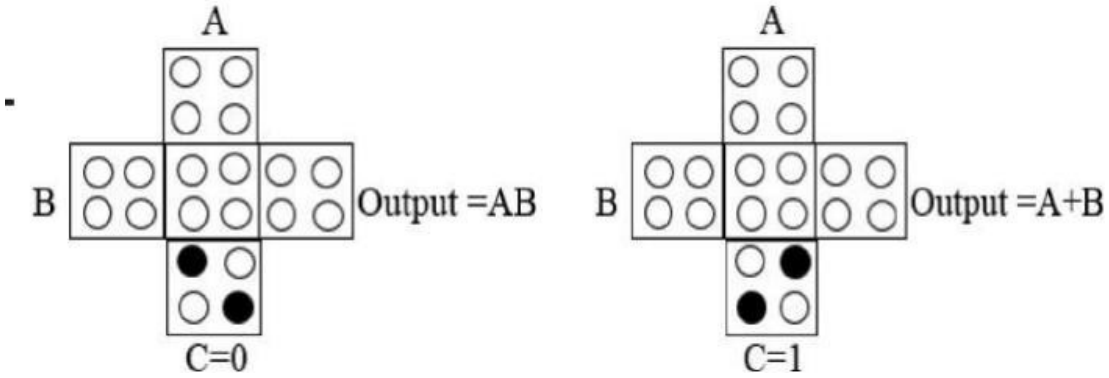


Figure 4: 2-input AND gate and 2-input OR gate using Majority voter.

3. METHODOLOGY QCA computation proceeds by direction of cells based on polarization of adjoining cells. An analysis is executed to find out the appropriate tools and verify the proposed circuit. Several approximate simulators as nonlinear approximation processes and bistable simulation engine are used to demonstrate. These procedures do not generate the genuine portion. Then QCA Designer 2.0.3 is preferred and this simulation engine is described [46]. QCA Designer is a tool used for model and simulation of QCA based circuit evolved at the ATIPS Laboratory. The functionality of the circuit is tested by QCA Designer 2.0.3 [47] which encompasses default values such as cell size, number of samples, radius of effect, convergence tolerance, relative permittivity, clock amplitude factor, Relaxation time etc. For implement the code converter in CMOS we used MICROWIND [48] which is a integrated tool for simulation.

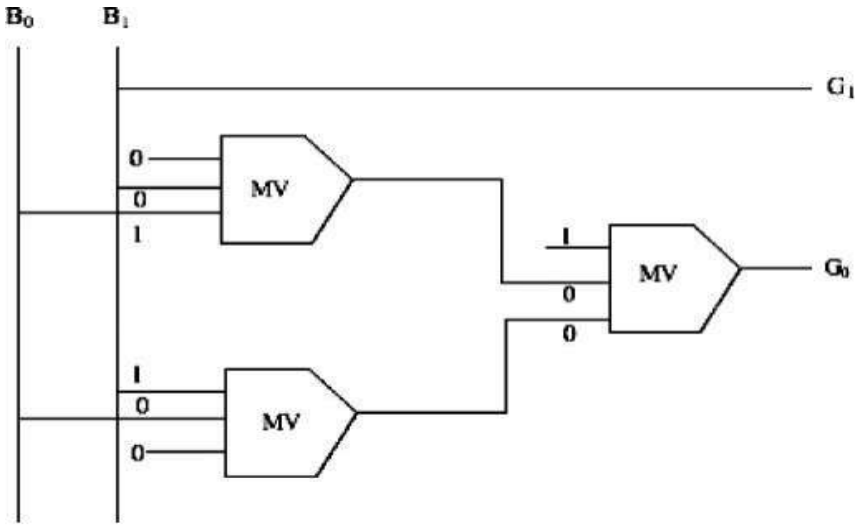
4. PROPOSED CIRCUIT AND PRESENTATION The immense availability of codes for corresponding different elements of information outcomes in the use of distinct codes by distinct schemes and it is required sometimes to use the result of the one system as employed to the input to another system. Code converters are circuits that convert a code into another which is programmed in logic arrays and used in many

fields such as protecting information from third parties and increase data. flexibility. It is also efficient in security department for devising and cracking codes.

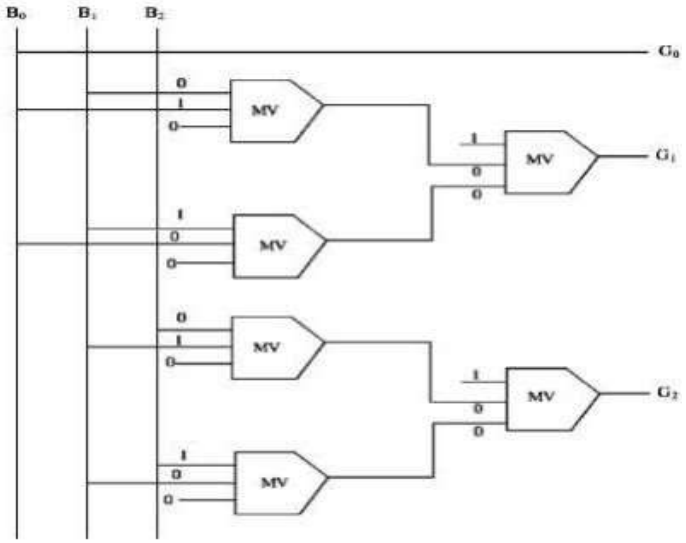
4.1 Binary code : A code is a symbolic presentation of data and performs text information using the number system. For instance a binary sequence of six bits 110100 is identical to decimal number 52.

4.2 Gray code : Reflected binary code, also known as Gray code is a numeral structure where each value differs only a sole bit from the previous bit. Gray code is not convenient for arithmetic operations. Gray code has many constructive applications including simplify fault correction, terrestrial television, some cable television system, analog-to-digital converter and peripheral apparatus.

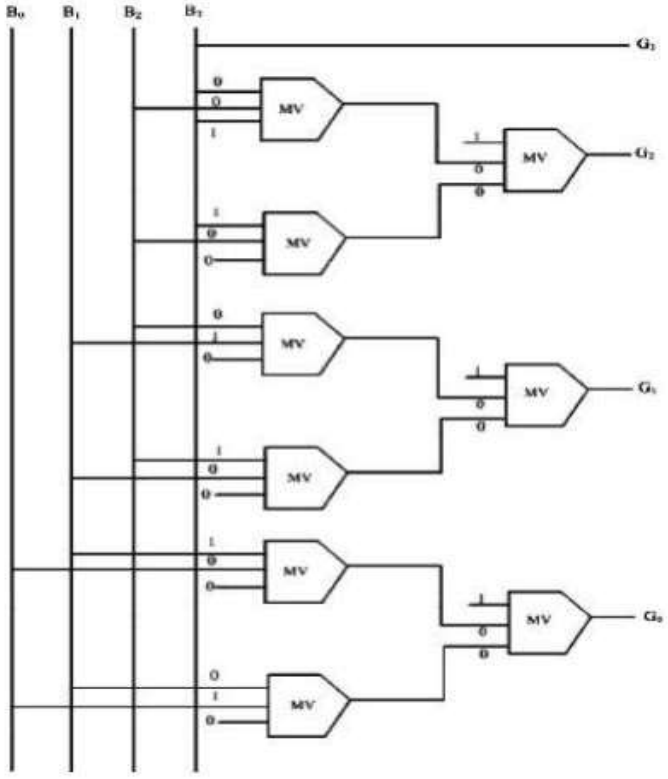
5. QCA IMPLEMENTATION OF CODE CONVERTERS Figure 5 shows the simplified block diagram of 2-bit binary-to-gray, 3-bit binary-to-gray and 4-bit binary-to-gray code converter using majority voter.



(a)

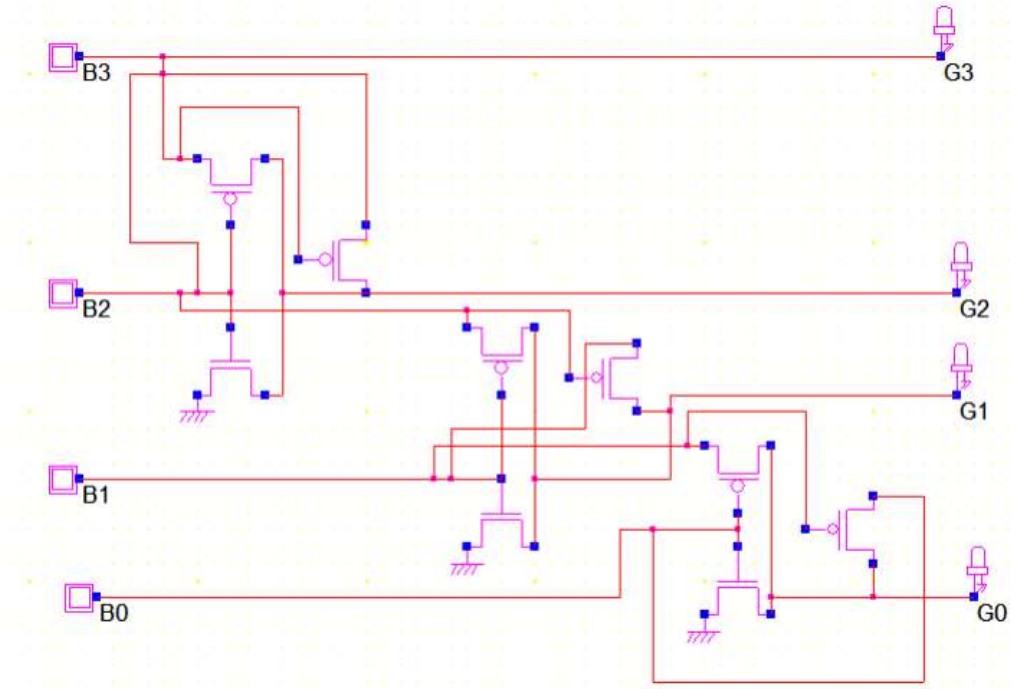


(b)

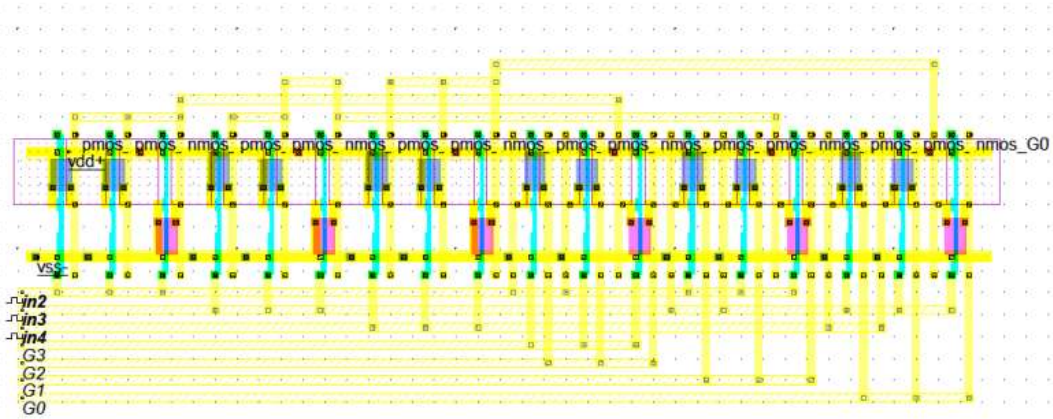


(c)

Figure 5: Block diagram of (a) 2-bit binary-to-gray (b) 3-bit binary-to-gray (c) 4-bit binary-to-gray code converter.



CMOS Implementation of Binary to Gray Code



Layout of Binary to grey Converter

A two bit binary-to-gray code converter composed of two binary inputs B1 and B0 and the corresponding gray outputs are G1 and G0 . Three bit binary-to-gray code converter composed of 3-inputs B0 , B1 and B2 and the corresponding gray outputs are G0 , G1 and G2 . Four bit binary-to-gray code converter composed of 4-inputs B3 , B2 , B1 and B0 and the corresponding gray outputs are G3 , G2 , G1 and G0 .Tables 1 to 3 shows the truth table of binary-to-gray code converter.

Table 1: Truth table Representations of two bit Binary to Gray Code Converter.

Binary Inputs		Gray Outputs	
B_1	B_0	G_1	G_0
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 2: Truth table Representations of three bit Binary to Gray Code Converter.

Binary Inputs			Gray Outputs		
B_0	B_1	B_2	G_0	G_1	G_2
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table 3: Truth table Representations of four bit Binary to Gray Code Converter.

Binary Inputs				Gray Outputs			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0

0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

6. SIMULATION AND RESULT The code converter circuits are designed using QCADesigner 2.0.3. The simulated circuit layout of 2-bit binary to gray, 3-bit binary to gray and 4-bit binary to gray code converter are shown in figure 6 to 8 respectively. The object parameters: cell width × cell height is 18 × 18 and dot diameter is 5.00. The logical equation of two bit binary to gray code converter is G1 = B1 and G0 = B1 ⊕B0 . For three bit binary to gray code converter the logical equation is G0 = B0 , G1 = B1 ⊕B0 and G2 = B2 ⊕B1 .The logical equation of four bit binary to gray code converter is G3 = B3 , G2 = B3 ⊕B2 , G1 = B2 ⊕B1 and G0 = B1 ⊕B0 .

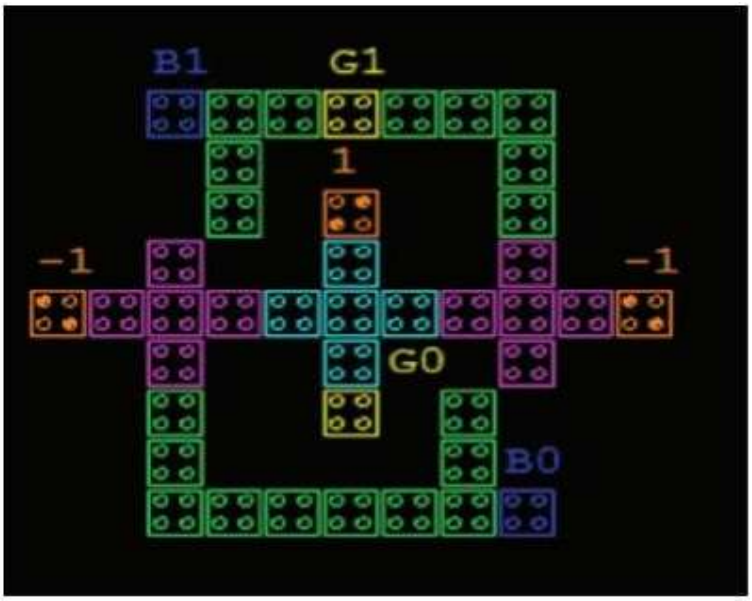


Figure 6: QCA implementation of two bit binary to gray code converter.

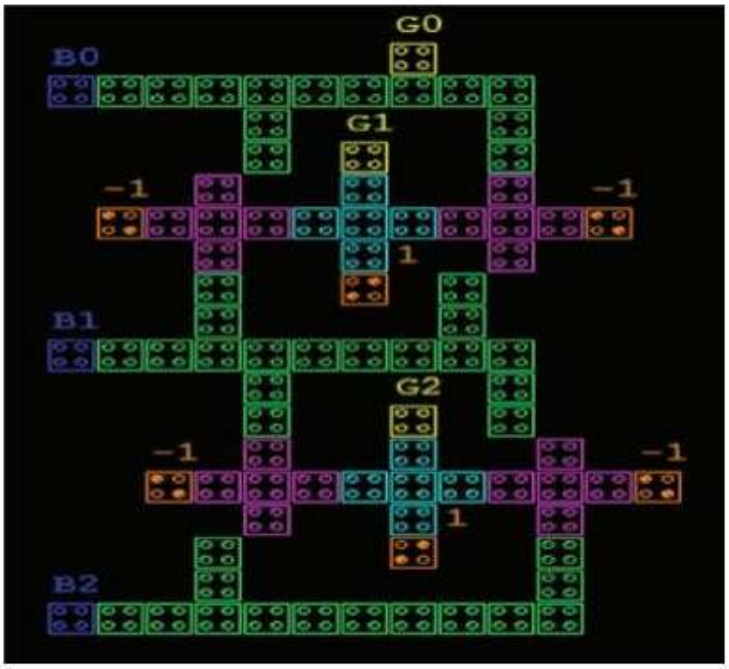


Figure 7: QCA implementation of three bit binary to gray code converter

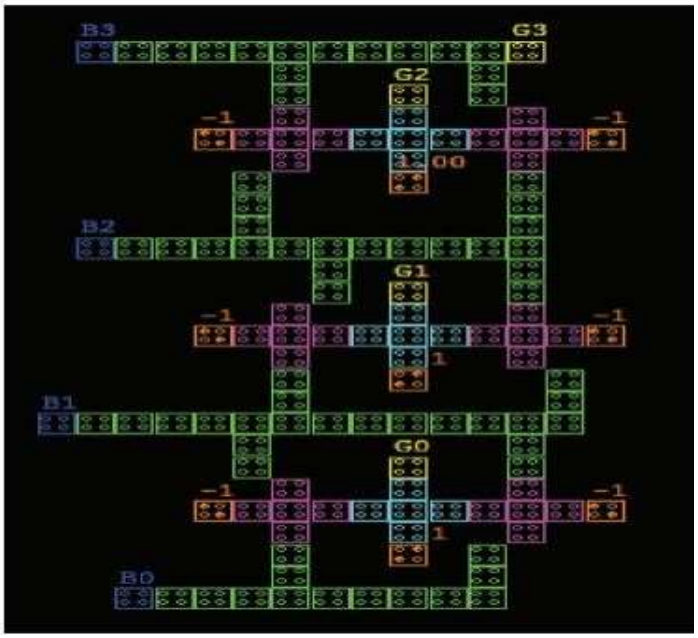
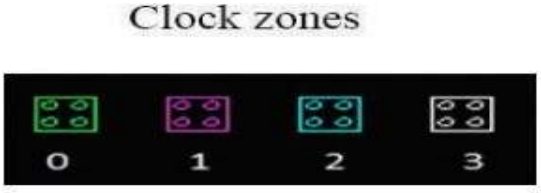


Figure 8: QCA implementation of four bit binary to gray code converter



The functionality of the proposed structure is approved from the simulated waveform. The following parameters are used for Bistable Approximation: Number of samples = 12800, convergence tolerance = 0.001000, radius of effect = 65.000000nm, relative permittivity = 12.900000, clock low = 3.800000e–023J, clock high = 9.800000e–022J, clock shift = 0, clock amplitude factor = 2.000000, layer separation = 11.500000 and maximum iterations per sample = 100. The above mentioned parameters are mostly default values in QCA Designer. Figure 9 to 11 shows the simulated waveforms of the code converters.

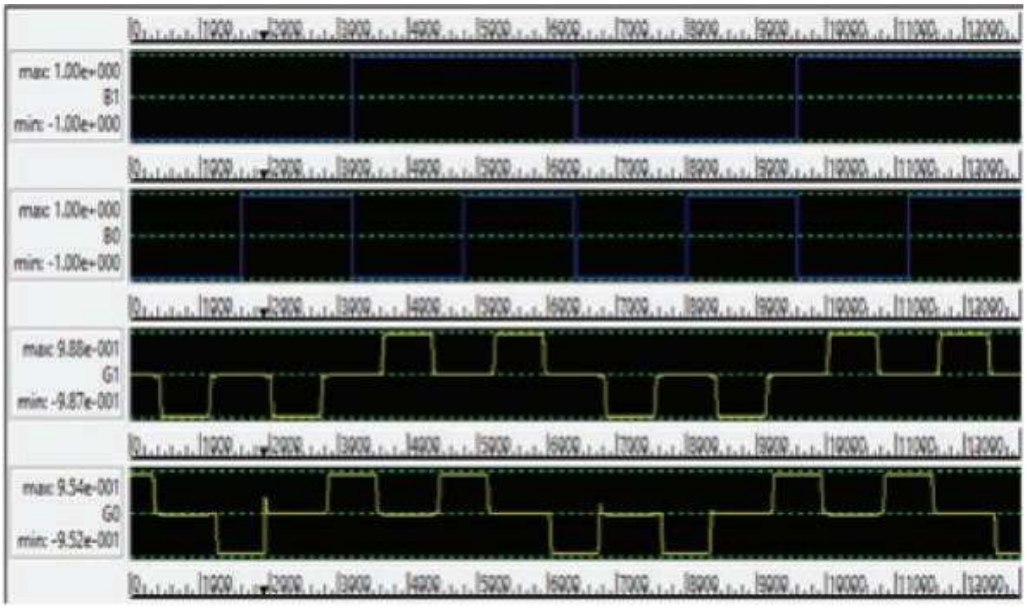


Figure 9: Simulated output of two bit binary to gray code converter.

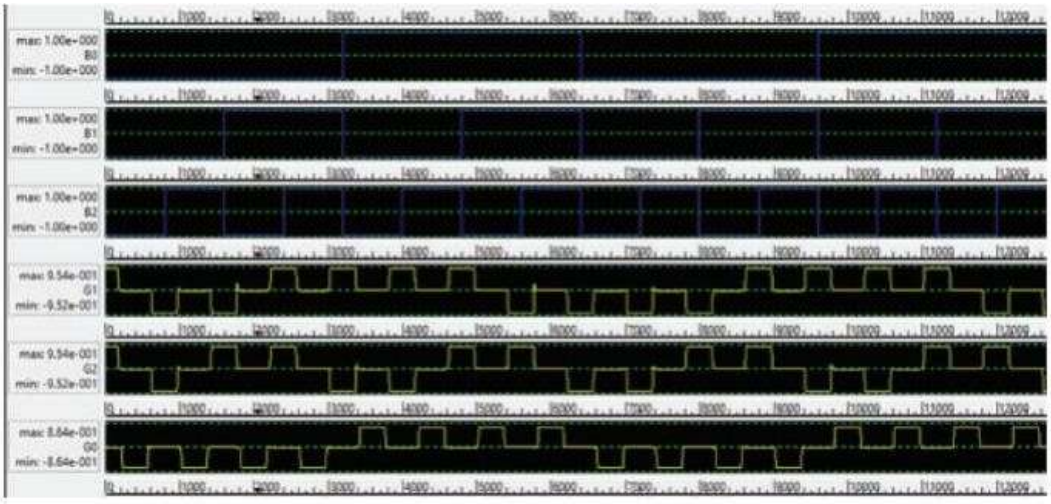


Figure 10: Simulated output of three bit binary to gray code converter.

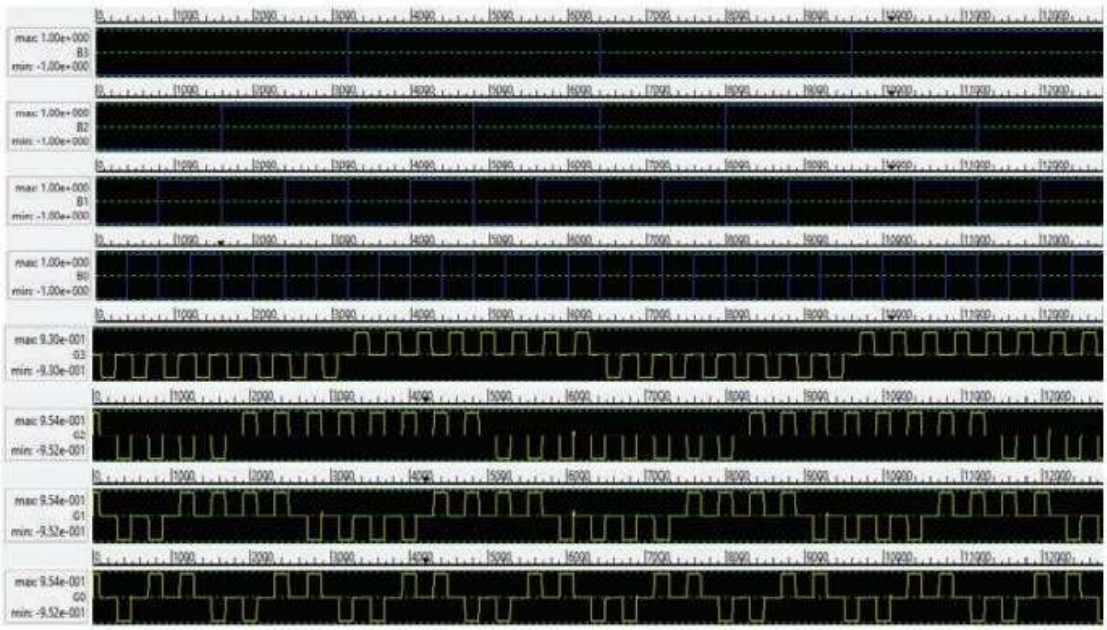


Figure 11: Simulated output of four bit binary to gray code converter.

For design and simulation the code converter in CMOS we employed MICROWIND. This is a very user-friendly engine to design and find out the covered area of logic gate.

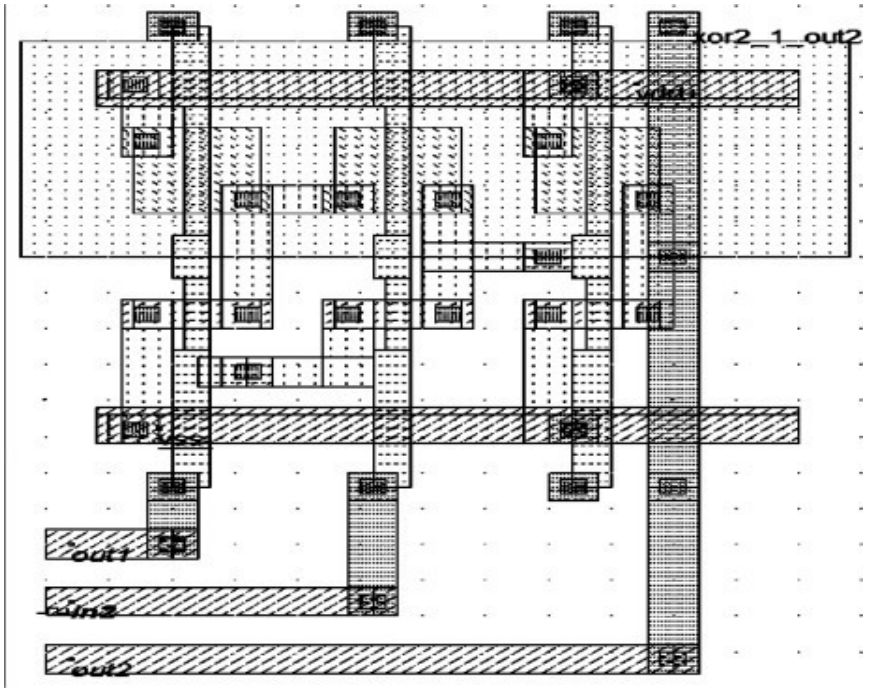


Figure 12: Simulated layout of two bit binary to gray code converter in CMOS.

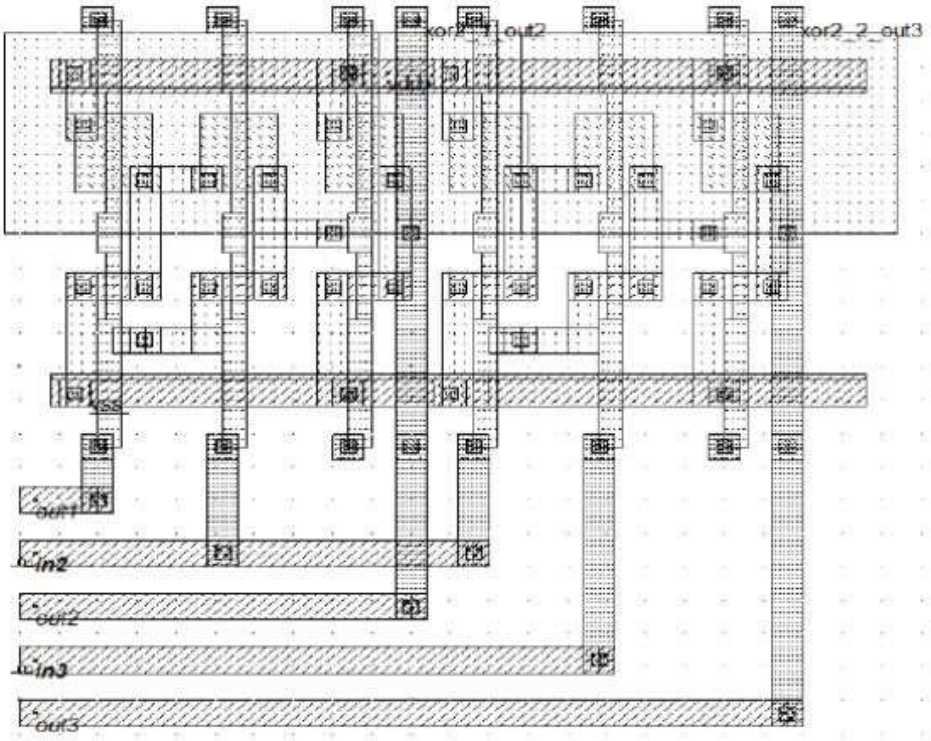


Figure 13: Simulated layout of three bit binary to gray code converter in CMOS.

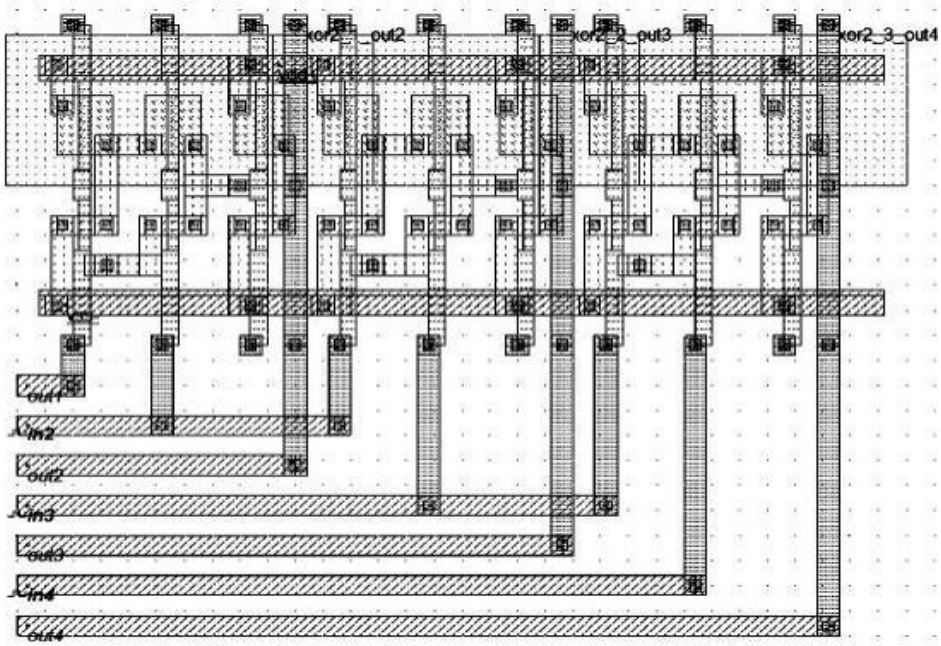


Figure 14: Simulated layout of four bit binary to gray code converter in CMOS

Table 4: Performance Factors of Binary to Gray Code Converter

Parameter	2 bit B2G	3 bit B2G	4 bit B2G
Total Number of Cells	41	86	131
Number of Clock	3	3	3
Clock delay	0.75	0.75	0.75
Area in QCA (μm^2)	0.05	0.12	0.18
Area in CMOS (μm^2)	22	44.2	71.78
Improvement (in times)	440	369	399

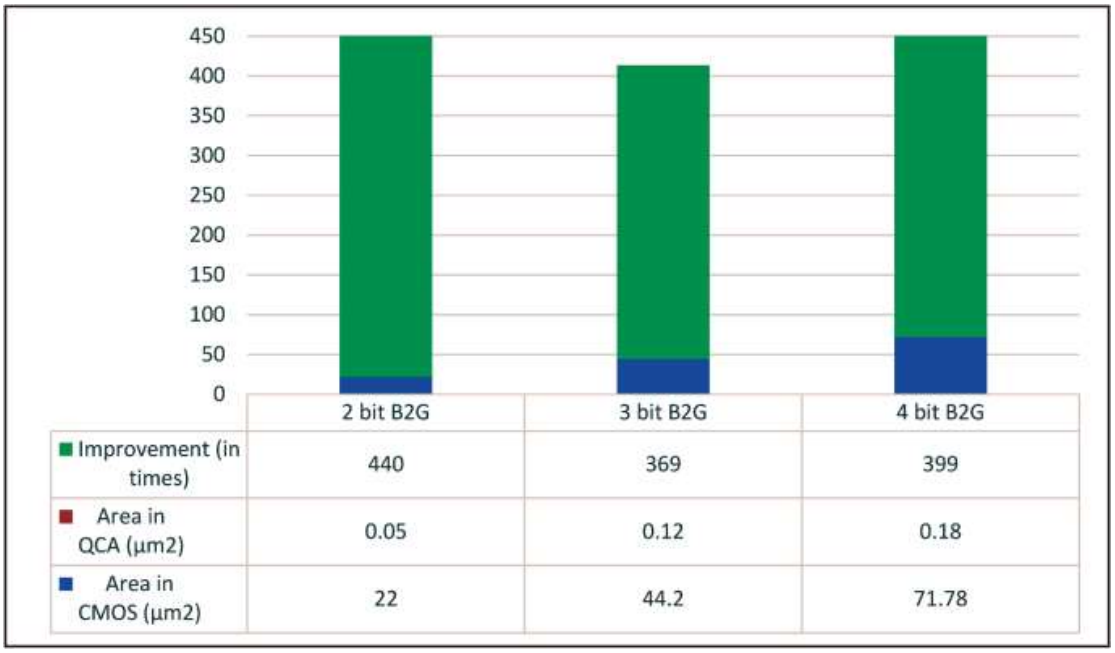
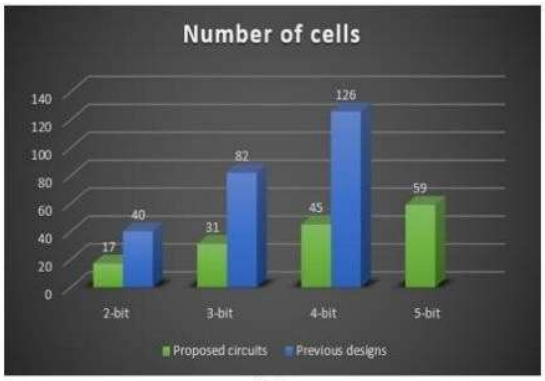
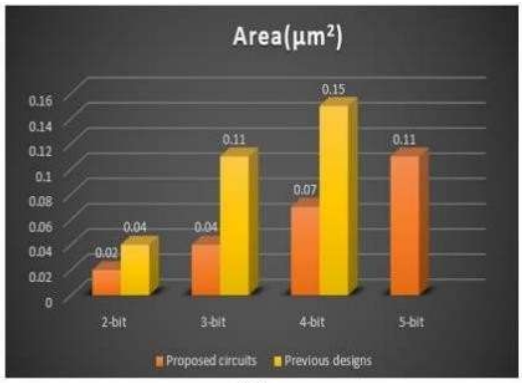


Figure 15: Comparative Figures for area (size) of QCA and CMOS with improvement.



(a)



(b)

Fig.16 **Fig.17**

Fig. 16 (a) Comparison of required cells between proposed designs and previous existing designs

(b) Represent the area (μm2) of basic gates and circuits.

Fig. 17 shows an analysis of the area between proposed designs and existing designs. The proposed designs of 2-bit, 3-bit, 4-bit, and 5-bit gray code converters take 0.02 μm2 , 0.04 μm2 , 0.07 μm2 and 0.11 μm2 , respectively and previous existing designs of 2-bit, 3-bit, and 4-bit gray code converters take 0.04 μm2 , 0.11 μm2 and 0.15 μm2 , respectively.

Fig. 18 shows the Area Utilization Factor (AUF) of 2-bit, 3-bit, 4-bit, and 5-bit binary to gray code converter which are 3.38, 4.05, 4.86 and 5.70, respectively.

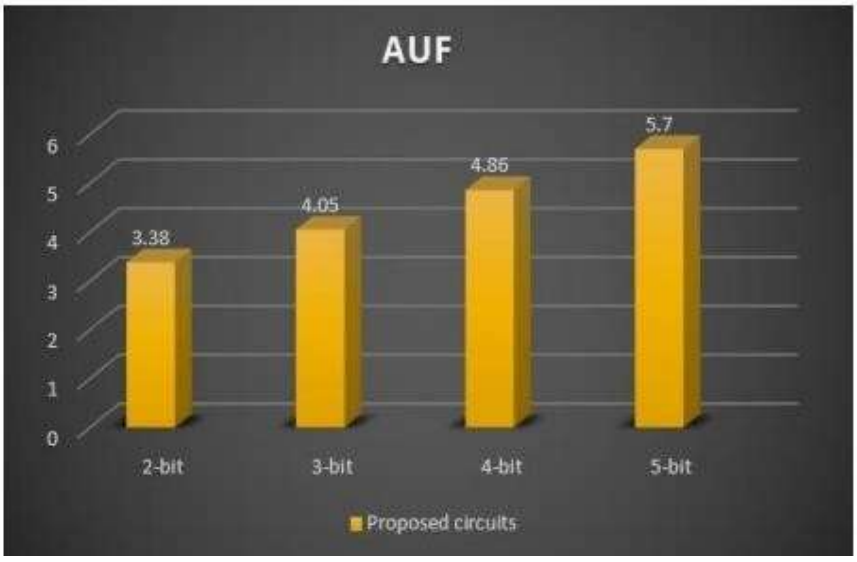


Fig. 18. Area utilization factor (AUF)

Chart 1

Comparative Study of proposed design for the 2-bit binary to gray code Converter.

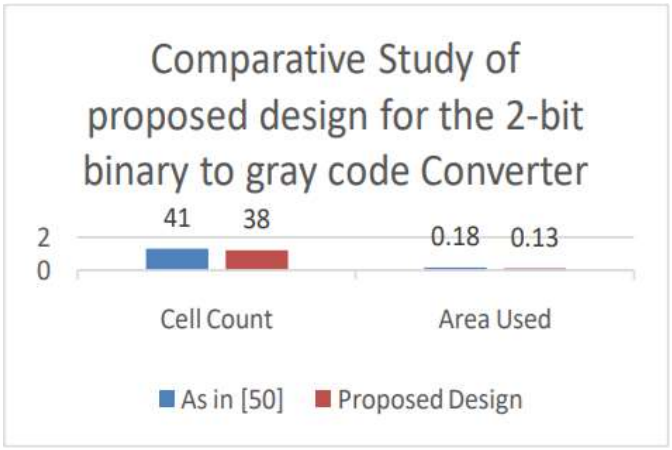


Chart 2

Comparative Study of proposed design for the 3-bit binary to gray code Converter.

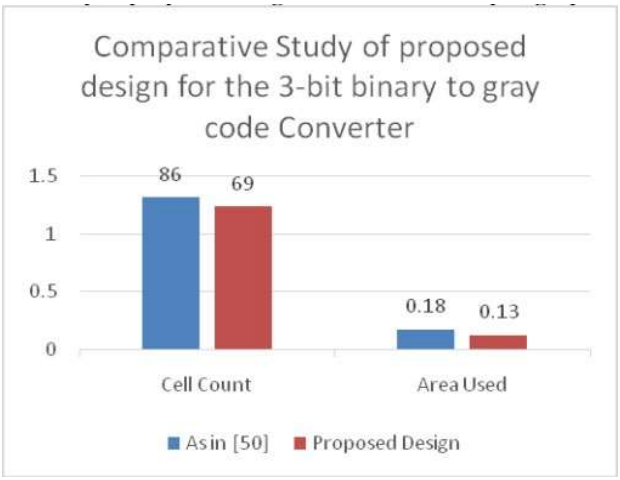
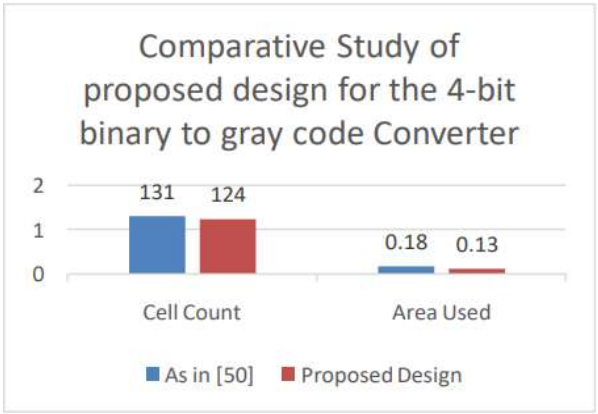


Chart 3 Comparative Study of proposed design for the 4-bit binary to gray code Converter.



CONCLUSION

In this paper, an effective approach for designing QCA based binary to gray converter has been presented in detail. The proposed designs are fit in the manner that they enclose less number of cells, clock phases and area. QCA technology can be best suited alternative of CMOS based technology. The simulation outcomes present that the proposed circuits execute well. These methods are conducive in quantum computing, digital signal processing (DSP), and nanotechnology. The proposed designs could be a promising step to build ALU's, model complicated circuits in smaller dimensions and low power architecture in nanotechnology.

This paper proposes a QCA based binary to gray code converter circuit. These converters' operations are explored using bistable vector simulation using QCA designer. The proposed designs are well organized with fewer cells and area, when compared to the existing circuits proposed in literature. The AUF of each design is also calculated.

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