Aditya Engineering College

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PROJECT TITLE: **Design of memristor based low power encoder using PGL technique**

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ABSTRACT	PO'S MAPPING	PSO'S MAPPING
Combinational logic circuits are the fundamental building blocks for almost all digital electronic systems. Here, a Memristor-based Encoder using Power Gating Logic (PGL) is designed. The design of digital logic gates using a memristor gives an alternative to the present IC design because of its lower power consumption as compared to CMOS logic. Memristive devices are novel structures, developed primarily as memory. Another interesting application for memristive devices is logic circuits. Here, A memristor-based encoder using power gating logic (PGL) is proposed. The encoder is also designed using various logic styles such as CMOS logic, Pseudo NMOS logic, and Memristor (MRL) logic for comparative analysis. From this Analysis Average Power is reduced to 80.7mW from 61.4mW and power-delay product (PDP) is reduced to 10666 x 10^-12 from 10816 x 10^-12.	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO8, PO9, PO10, PO11, PO12	PSO1

RELEVANCE TO PO'S & PSO'S

PO1	This project helped students to gain in depth knowledge upon the VLSI CAD Tools i.e., Cadence
PO2	This project helped students to understands the impacts of high-power usage of different combinational circuits.
PO3	This project of low power encoder design is achieved by the design of PGL technique on MRL based encoder.
PO4	This project helped students to understand the nature of memristor through various research papers and helped to implement the PGL Technique.
PO5	Through this project students can understand it is possible to retrieve circuit design through Verilog A code in Cadence.
PO6	This project can help us to build more complex designs that uses less power. And the need for less power consumption in electronics.
PO7 & PO8	This project helped us understand the basics ethics to be followed during the research stage of our project. We collaborated with professional researchers and used their ideas to develop ours.
PO9	This project can be tested individually and on team, students worked as team to bring this project into implementation
PO10	This project helped students to improve their communication in all means which bring up them as a leader
PO11 &PO12	In this project implementation students used resources and money efficiently and the need for managing a project effectively. An extension of this project could involve broadest the learning.

PO1	**Engineering Knowledge**	**PO7**	**Environment and Sustainability**	**PSO1**	**Provide sustainable solutions in the field of Communication and Signal Processing**
PO2	**Problem Analysis**	**PO8**	**Ethics**		
PO3	**Design & Development solution**	**PO9**	**Individual and Teamwork**	**PSO2**	**Apply current technologies in the field of VLSI and embedded systems for professional growth.**
PO4	**Investigations**	**PO10**	**Communication**		
PO5	**Modern tools**	**PO11**	**Project management and finance**		
PO6	**The Engineer & society**	**PO12**	**Life log learning**		

CONCLUSION

When compared to pseudo NMOS and regular CMOS logic, memristor-based encoders in Power Gating logic are significantly more efficient in terms of both power and area. A circuit's power, area, and speed are always being traded off. It is therefore possible to draw the conclusion that this design method requires fewer transistors overall thereby reducing the power consumption and delay of the overall combinational circuit. The memristor based encoder with power gating logic (PGL) uses 91.4% less power than CMOS encoder circuit and 41.3% less power than pseudo NMOS encoder circuit and 23.9% less than the memristor based encoder. So, therefore 23.9% of power saving achieved by implementing PGL technique in the memristor based encoder. By employing the PGL Technique, the encoder's total power consumption is lowered by 23.9% to 61.4mW from 80.7mW. This benefit makes the process of constructing a digital circuit more effective.