The maximum clock frequency in MHz of a 4-stage ripple counter, utilizing flip-flops, with each flip-flop having a propag
The digital circuit shown _____

[label=()]is a divide-by-5 counter is a divide-by-7 counter is a divide-by-8 counter does not function as a counter due to

The propogation delay of the exclusive-OR(XOR) gate in the circuit in the figure is 3ns.The propogation delay of all the
logic ports=ieee, logic ports/scale=0.5 (-1.3,-0.56)node[xor port,anchor=out](x) ; (-1.3,-1.3) rectangle (0,0); (-1,-0.6) no
Starting from the initial value of the flip-flop outputs $Q2Q1Q0 = 111$ with $D2 = 1$,the minimum number of triggering cl
For the 3-bit binary counter shown in the figure, the output increments at every positive transition in the clock (CLK).
Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops. [H
The number of states in the state transition diagram of this circuit that have a transition back to the same state on som

(0.35,-0.3)node; (2.35,-0.35)node; (4.6,-0.35)node$Output$; (-2,-0.6)node$Input$;
$1000, 3$
$333.33, 1$
$2000, 3$
$333.33, 3$

In a given sequential circuit, initial states are $Q1 = 1$ and $Q2 = 0$. For a clock frequency of $1MHz$, the frequency of sig

(10.9,3.5)–(10.9,5.4); (10.9,5.4)–(-1.0,5.4); (-1.0,5.4)–(-1.0,3.5); (0,3.5)–(-1.0,3.5);
Neglecting the delays due to the logic gates in the circuit shown in figure, the decimal equivalent of the binary sequence

[H] [width=]ide/7474/figs/Gate$_q$uestion.png$Neglecting the delays$
Consider a sequential digital circuit consisting of T flip-flops and D flip-flops as shown in the figure. CLKIN is is the clo
[ht] (1.6,2.5) node T Flip Flop; (0,0)–(3,0)–(3,5)–(0,5)–(0,0); (0.3,4.5) node$T$; (2.8,3.5) node$Q$; (0.7,2.0) nodeCLK; (6.6
$(0, 0, 1)$
$(1, 0, 0)$
$(1, 0, 1)$
$(1, 1, 1)$
The output of a 2-input multiplexer is connected back to one of its inputs as shown in the figure.

Match the functional equivalence of this circuit to one of the following option.

[label = Alph*]D Flip-Flop D Latch Half-adder Demultiplexer