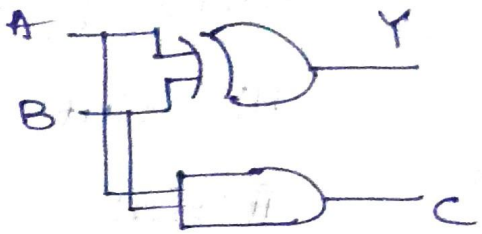
* HALF ADDER :—

→ Design code :

A	B	Y	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1




```
module HF(
 input A, B,
 output Y, C
 );
 xor (Y, A, B);
 and (C, A, B);
endmodule
```

[or]

```
module HF(
 input A, B;
  output Y, C.
 );
 assign Y = A ^ B;
 assign C = A & B;
endmodule
```

Testbench :—

```
module HF ( );
reg A, B;
wire Y, C;
HF dut (A, B, Y, C);
initial
    begin
A = 0 ; B = 0;
#10
A = 0 ; B = 1;
#10
A = 1 ; B = 0;
#10
A = 1 ; B = 1;
#10
end
$finish ( );
endmodule
```