HALF SUBTRACTOR

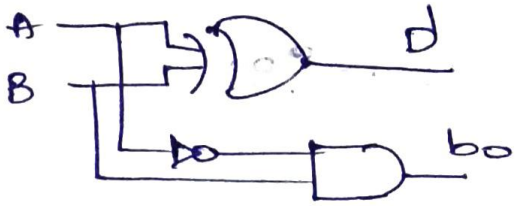
```
module HS(a,b,d,bo);
input a,b;
output d,bo; wire n1;
xor(d,a,b);
not(n1,a);
and(bo,n1,b);
endmodule
```

[00]

```
module HS(a,b,d,bo);
input a,b;
output d,bo;
assign diff = a^b;
assign bo = ~a&b;
endmodule
```

[00]

```
module HS(a,b,d,bo);
input a,b;
output reg d,bo;
always@(*)
  begin
    d = a^b;
    bo = ~a&b;
  end
endmodule
```



A	B	d	bo
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Testbench :—

```
module HS_tb();
reg a,b;
wire d, bo;
HS uut (a,b,d, bo);
initial
    begin
a=0 ; b=0;
#10
a=0 ; b=1;
#10
a=1 ; b=0;
#10
a=1; b=1;
#10
end
endmodule
```