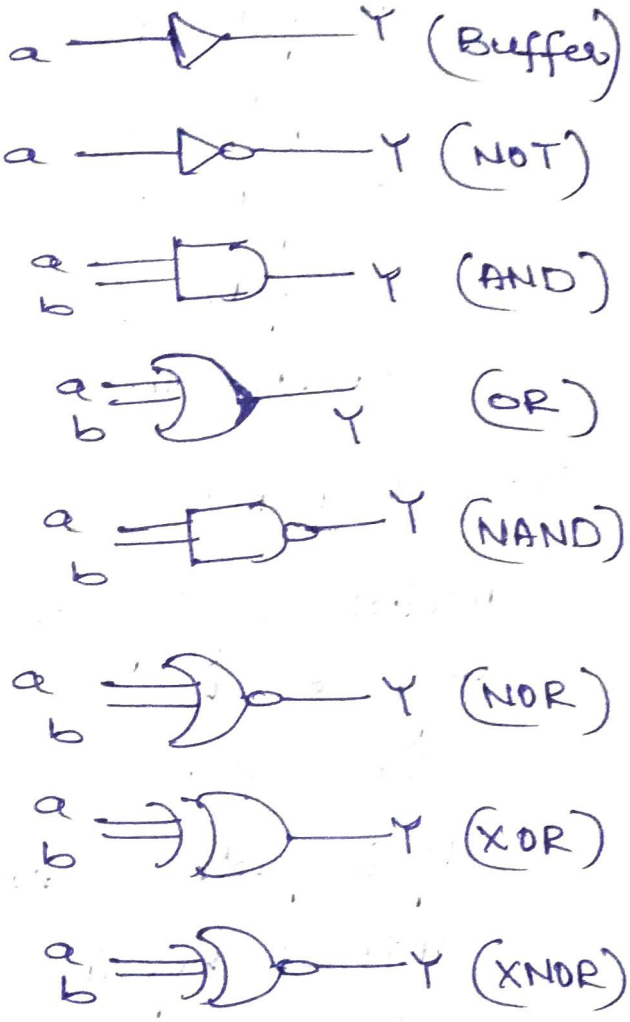
Verilog codes

* logic Gates :-

① Design code : [Gate level modelling]

```
module logicgates(
input a, b,
output Y
);
not(Y, a);
not(Y, b);
and (Y, a, b);
or (Y, a, b);
nand (Y, a, b);
nor (Y, a, b);
xor (Y, a, b);
xnor (Y, a, b);
buf (Y, a);
end module
```



(or)

② Design code : [Data flow modelling]

```
module logic gates(
input a, b,
```

```
    output Y
    );
    assign Y = a;
    assign Y = ~a;
    assign Y = a ^ b;
    assign Y = a | b;
    assign Y = ~(a ^ b);
    assign Y = ~(a | b);
    assign Y = a & b;
    assign Y = ~(a & b);
    endmodule
```

Test bench :—

```
module logicgates_tb( );
reg a, b;
wire Y;
logic gates dut (a, b, Y);
initial begin
a=1 ; b=1;
#10
a= 1; b=0;
#10
a=0; b=1;
#10
a=0 ; b=0;
#10
end
$finish( );
endmodule.
```