Verilog codes

* 10 gic Gates:

Design code: [Gate level modelling]
module logicales:

input a, b, output y
);

not(Y,a);
not(Y,b);
and (Y,a,b);

nond (Y, a, b); nond (Y, a, b); nost (Y, a, b);

XOL (Y, a, b); XOL (Y, a, b);

buf (Y, a);

end module

a Y (Buffer)

a - DO Y (NOT)

a Dy (AND)

a=Dy (OR)

a TOTY (NAND)

a JOY (NOR)

b T (XOR)

2 -> Y (XNOR)

(go)

1 Design code: [Douta flow modelling]

module 10 gic getes (

input asb,

output Y 1 assign Y = a; assign Y = was assign Y = a + b; assign Y = a | b; assign ix = n(a fb); assign Y = n(a16); assign Y = a 1 b; assign Y = N(a 16); end module. Test bench :module logicogates-tb(); rega, b; wine Y; logic gates dut (a,b, Y); initial begin #10 a= 1; b=0; #10 a=0; b=1; # 10 a=0; b=0; #10 \$finish c