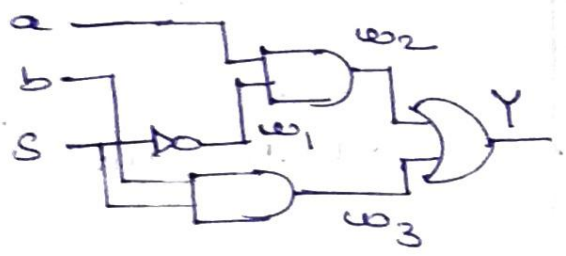
MUX

Design code :-




```
module mux21(
    input a, b, s,
    output Y );
wire w1, w2, w3;
not (w1, s);
and (w2, a, w1);
and (w3, b, s);
or (Y, w2, w3);
endmodule
```

[ ]

```
module mux21(
    input a, b, s,
    output Y );
assign Y = (a & ~s) | (b & s);
endmodule
```

[ ]

```
module mux21(
    input a, b, s,
    output Y );
always @(a | b | s)
  begin
   if (s == 1)
```

```
    Y = a;
  else
    Y = b;
 end
 endmodule
```

Testbench :—

```
module mux21_tb();
reg a, b, s;
wire Y;
mux21 uut (a, b, s, Y);
initial
    begin
a=0; b=0; s==0;
#10
a=1; b=1; s==0;
#10
a=0; b=1; s==1;
#10
a=1; b=0; s==1;
#10
end
$finish();
endmodule
```