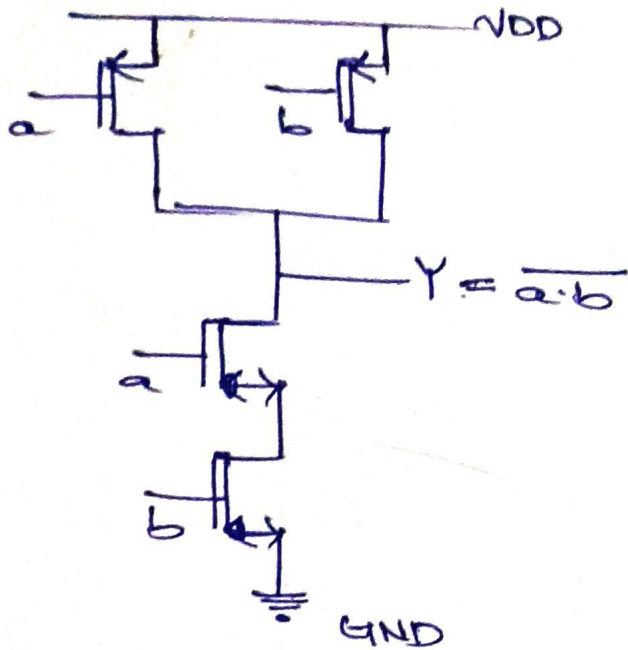
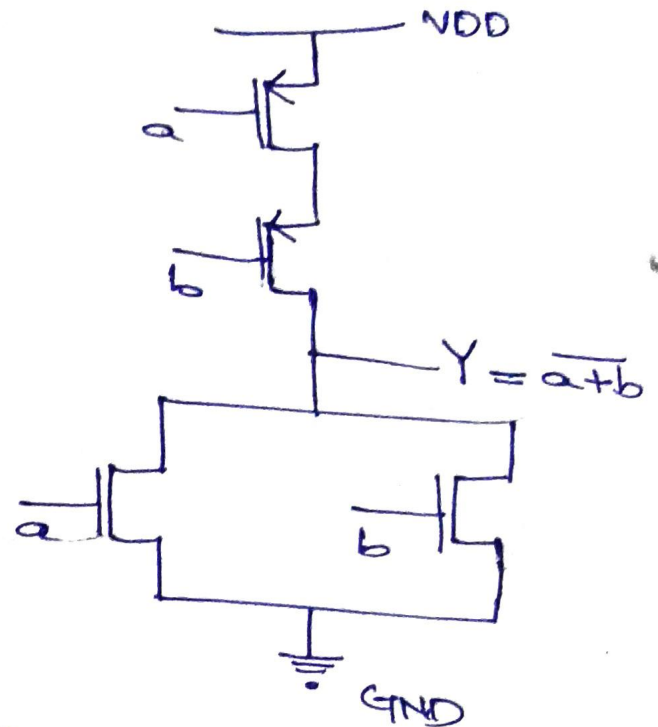


Transistor level Designs for logic gates:-

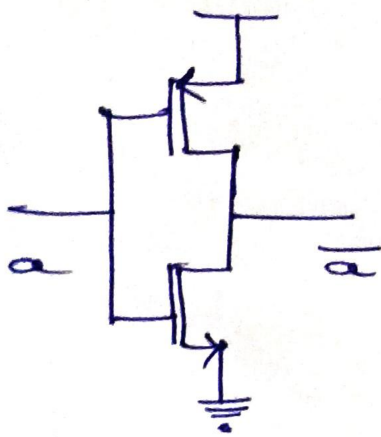
NAND:-



NOR :-



NOT :-



XOR :-

