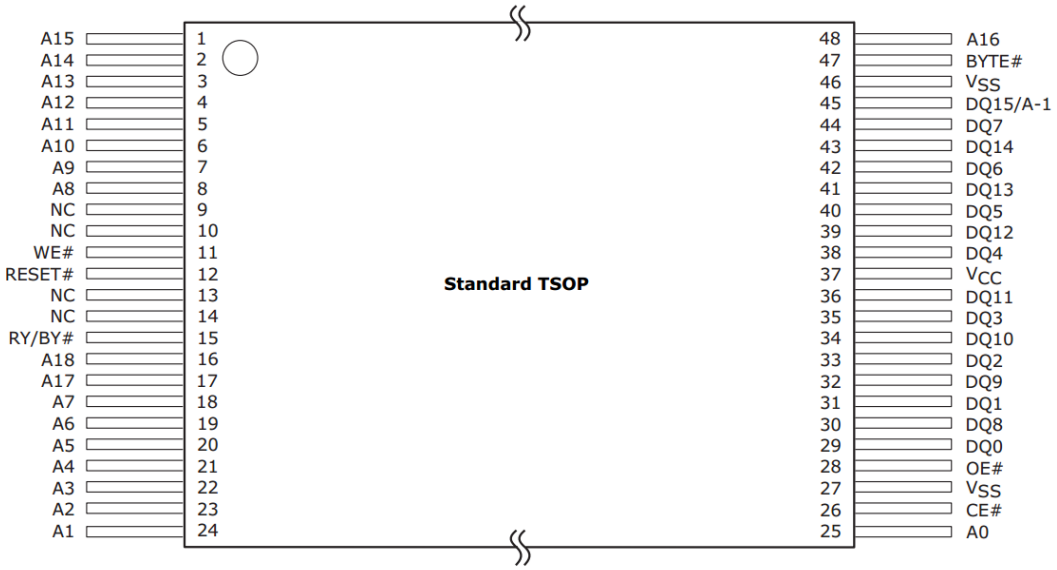
Am29LV800BB-90EC

基本参数

容量：8M 电源 2.7-3.6V 响应时间：90ms 引脚数：48

引脚图

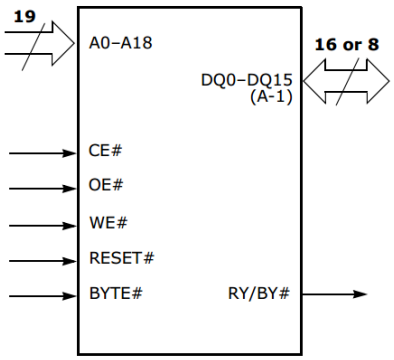


PIN CONFIGURATION

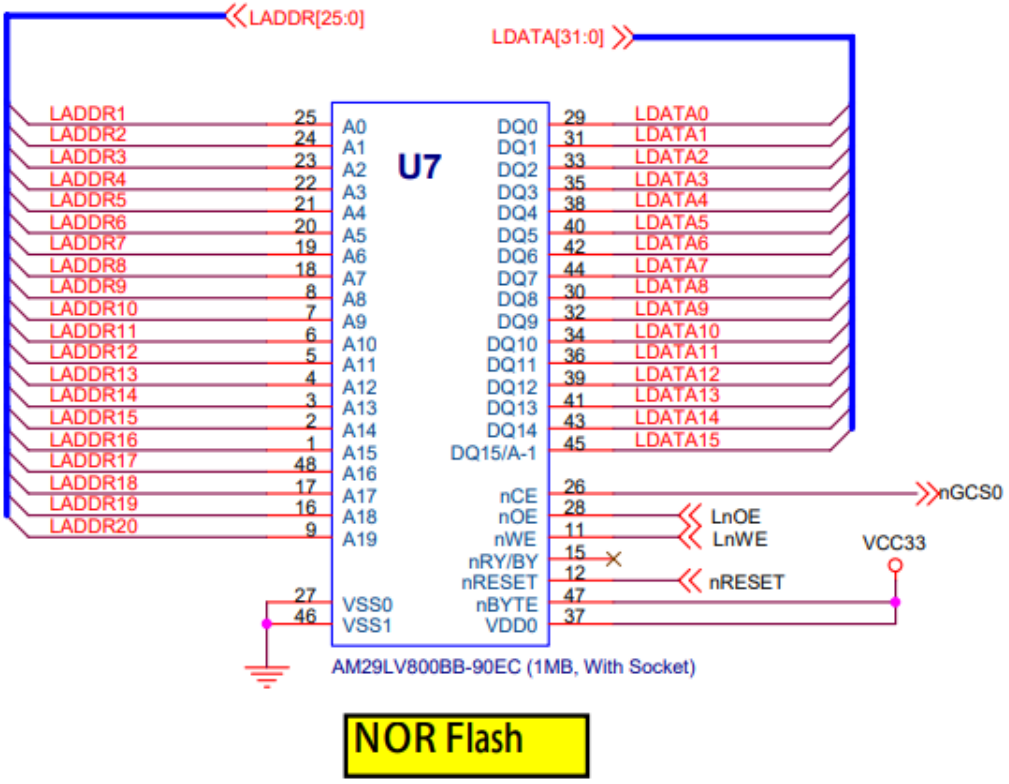
A0–A18	=	19 addresses
DQ0–DQ14	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin, active low
RY/BY#	=	Ready/Busy# output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

字节模式比字模式多需要一位地址，由此输入

LOGIC SYMBOL



与 S3C2440 接线



根据连线可知，BYTE#键设置模式为字配置状态。

设备总线操作

Table 1. Am29LV800B Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
							BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:
1. *Addresses are A18:A0 in word mode (BYTE# = V_{IH}), A18:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection/Unprotection" section.*

扇区划分

Table 3. Am29LV800BB Bottom Boot Block Sector Addresses

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
									(x8) Address Range	(x16) Address Range
SA0	0	0	0	0	0	0	X	16/8	00000h–03FFFh	00000h–01FFFh
SA1	0	0	0	0	0	1	0	8/4	04000h–05FFFh	02000h–02FFFh
SA2	0	0	0	0	0	1	1	8/4	06000h–07FFFh	03000h–03FFFh
SA3	0	0	0	0	1	X	X	32/16	08000h–0FFFFh	04000h–07FFFh
SA4	0	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA5	0	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA6	0	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA7	0	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA8	0	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA9	0	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA10	0	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh
SA11	1	0	0	0	X	X	X	64/32	80000h–8FFFFh	40000h–47FFFh
SA12	1	0	0	1	X	X	X	64/32	90000h–9FFFFh	48000h–4FFFFh
SA13	1	0	1	0	X	X	X	64/32	A0000h–AFFFFh	50000h–57FFFh
SA14	1	0	1	1	X	X	X	64/32	B0000h–BFFFFh	58000h–5FFFFh
SA15	1	1	0	0	X	X	X	64/32	C0000h–CFFFFh	60000h–67FFFh
SA16	1	1	0	1	X	X	X	64/32	D0000h–DFFFFh	68000h–6FFFFh
SA17	1	1	1	0	X	X	X	64/32	E0000h–EFFFFh	70000h–77FFFh
SA18	1	1	1	1	X	X	X	64/32	F0000h–FFFFFh	78000h–7FFFFh

Note for Tables 2 and 3: *Address range is A18:A-1 in byte mode and A18:A0 in word mode. See "Word/Byte Configuration" section.*

命令时钟周期

Table 1. Am29LV800B Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2-5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	01				
		Byte		AAA		555		AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	90	X01	22DA				
		Byte		AAA		555		AAA		X02	DA				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	555	90	X01	225B				
		Byte		AAA		555		AAA		X02	5B				
	Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
											XX01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 10)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 12)			1	XXX	B0										
Erase Resume (Note 13)			1	XXX	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A18–A12 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except when reading array or autoselect data, all bus cycles are write operations.*
4. *Data bits DQ15–DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A18–A11 are don't cares for unlock and command cycles, unless PA or SA required.*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth cycle of the autoselect command sequence is a read cycle.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.*
10. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
11. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
12. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
13. *The Erase Resume command is valid only during the Erase Suspend mode.*

写操作状态表

Table 2. Write Operation Status

Operation		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes:

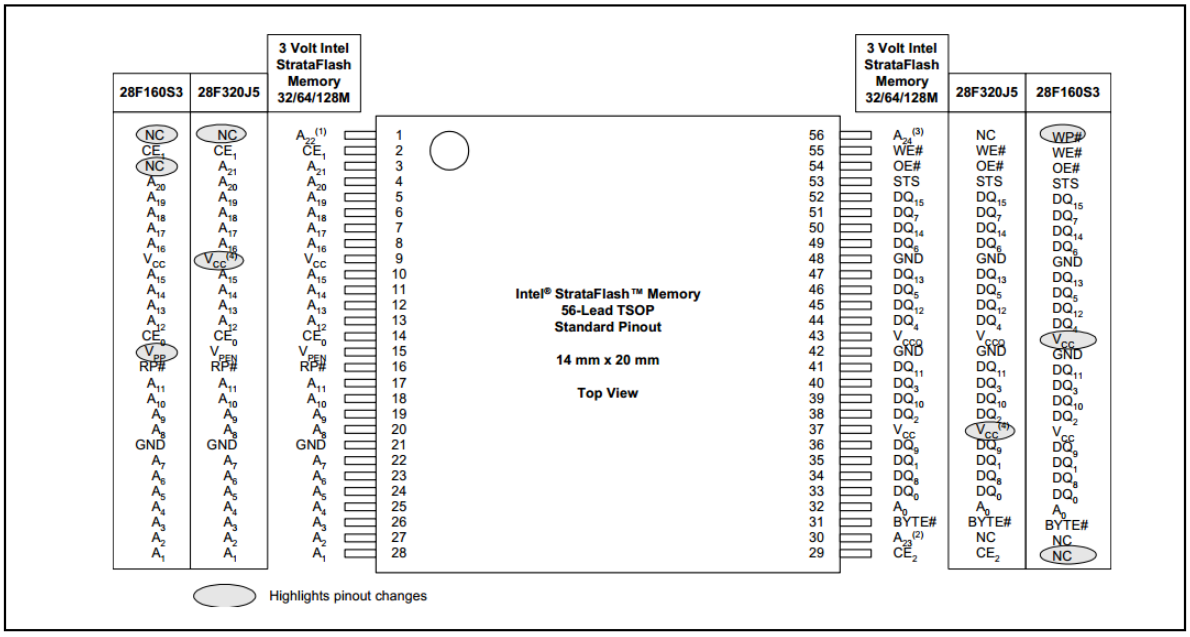
1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

E28F128J3A150

基本参数

容量：16M 电源 2.7-3.6V 引脚数：56

引脚图

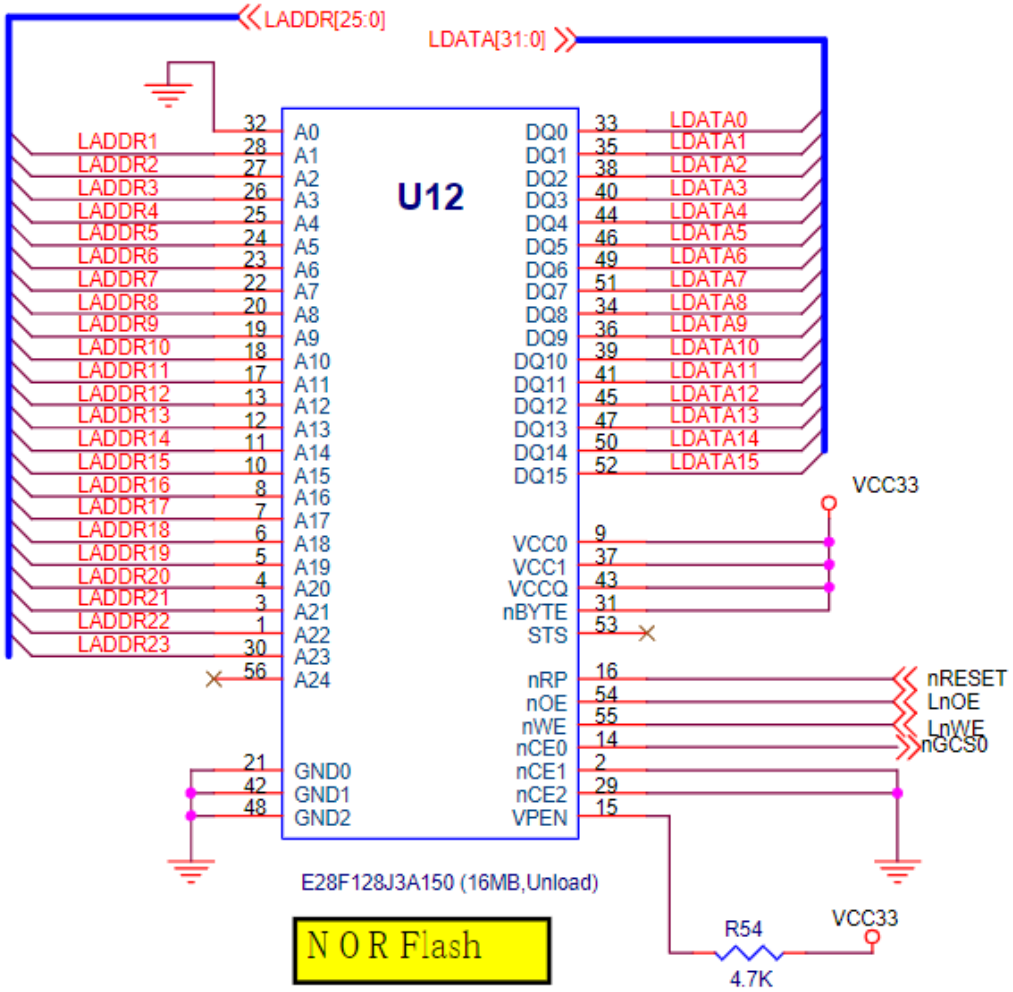


NOTES:

1. A_{22} exists on 64-, 128- and 256-Mbit densities. On 32-Mbit densities this pin is a no-connect (NC).
2. A_{23} exists on 128-Mbit densities. On 32- and 64-Mbit densities this pin is a no-connect (NC).
3. A_{24} exists on 256-Mbit densities. On 32-, 64- and 128-Mbit densities this pin is a no-connect (NC).
4. V_{CC} = 5 V ± 10% for the 28F640J5/28F320J5.

Symbol	Type	Name and Function
A_0	INPUT	**BYTE-SELECT ADDRESS:** Selects between high and low byte when the device is in x8 mode. This address is latched during a x8 program cycle. Not used in x16 mode (i.e., the A_0 input buffer is turned off when BYTE# is high).
A_1–A_{23}	INPUT	**ADDRESS INPUTS:** Inputs for addresses during read and program operations. Addresses are internally latched during a program cycle. 32-Mbit: A_0–A_{21} 64-Mbit: A_0–A_{22} 128-Mbit: A_0–A_{23}
DQ_0–DQ_7	INPUT/ OUTPUT	**LOW-BYTE DATA BUS:** Inputs data during buffer writes and programming, and inputs commands during Command User Interface (CUI) writes. Outputs array, query, identifier, or status data in the appropriate read mode. Floated when the chip is de-selected or the outputs are disabled. Outputs DQ_6–DQ_0 are also floated when the Write State Machine (WSM) is busy. Check SR.7 (status register bit 7) to determine WSM status.
DQ_8– DQ_{15}	INPUT/ OUTPUT	**HIGH-BYTE DATA BUS:** Inputs data during x16 buffer writes and programming operations. Outputs array, query, or identifier data in the appropriate read mode; not used for status register reads. Floated when the chip is de-selected, the outputs are disabled, or the WSM is busy.
CE_0, CE_1, CE_2	INPUT	**CHIP ENABLES:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. When the device is de-selected (see Table 2 on page 7), power reduces to standby levels. All timing specifications are the same for these three signals. Device selection occurs with the first edge of CE_0, CE_1, or CE_2 that enables the device. Device deselection occurs with the first edge of CE_0, CE_1, or CE_2 that disables the device (see Table 2 on page 7).
RP#	INPUT	**RESET/ POWER-DOWN:** Resets internal automation and puts the device in power-down mode. RP#-high enables normal operation. Exit from reset sets the device to read array mode. When driven low, RP# inhibits write operations which provides data protection during power transitions.
OE#	INPUT	**OUTPUT ENABLE:** Activates the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the Command User Interface, the Write Buffer, and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
STS	OPEN DRAIN OUTPUT	**STATUS:** Indicates the status of the internal state machine. When configured in level mode (default mode), it acts as a RY/BY# pin. When configured in one of its pulse modes, it can pulse to indicate program and/or erase completion. For alternate configurations of the STATUS pin, see the Configurations command. Tie STS to V_{CCQ} with a pull-up resistor.
BYTE#	INPUT	**BYTE ENABLE:** BYTE# low places the device in x8 mode. All data is then input or output on DQ_0–DQ_7, while DQ_8–DQ_{15} float. Address A_0 selects between the high and low byte. BYTE# high places the device in x16 mode, and turns off the A_0 input buffer. Address A_1 then becomes the lowest order address.
V_{PEN}	INPUT	**ERASE / PROGRAM / BLOCK LOCK ENABLE:** For erasing array blocks, programming data, or configuring lock-bits. With $V_{PEN} \le V_{PENLK}$, memory contents cannot be altered.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY:** With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited.
V_{CCQ}	OUTPUT BUFFER SUPPLY	**OUTPUT BUFFER POWER SUPPLY:** This voltage controls the device's output voltages. To obtain output voltages compatible with system data bus voltages, connect V_{CCQ} to the system supply voltage.
GND	SUPPLY	**GROUND:** Do not float any ground pins.
NC		**NO CONNECT:** Lead is not internally connected; it may be driven or floated.
DU		DON'T USE: **Do not drive ball to V_{IH} or V_{IL}, leave disconnected**

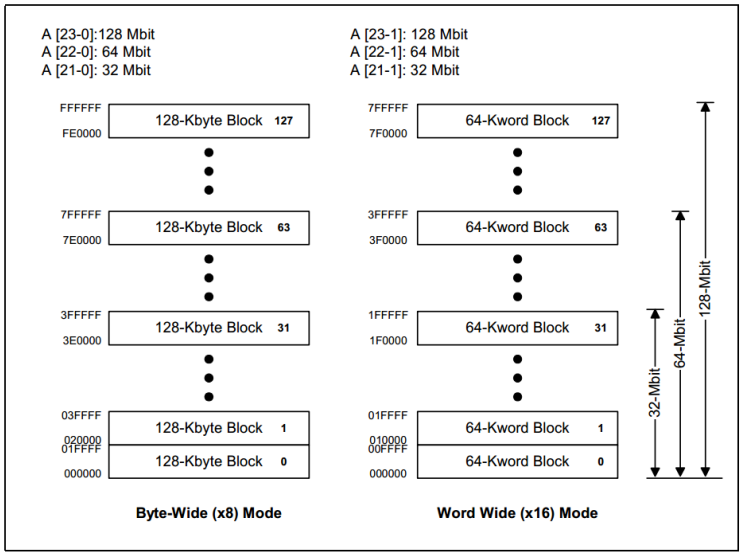
与 S3C2440 连线



根据连线可知，BYTE#键设置模式为字配置状态。

分区

Figure 4. Memory Map



设备总线操作

Table 3. Bus Operations

Mode	Notes	RP#	$CE_{0,1,2}$[1]	OE#[2]	WE#[2]	Address	V_{PEN}	DQ[3]	STS (default mode)
Read Array	4,5,6	V_{IH}	Enabled	V_{IL}	V_{IH}	X	X	D_{OUT}	High Z[7]
Output Disable		V_{IH}	Enabled	V_{IH}	V_{IH}	X	X	High Z	X
Standby		V_{IH}	Disabled	X	X	X	X	High Z	X
Reset/Power-Down Mode		V_{IL}	X	X	X	X	X	High Z	High Z[7]
Read Identifier Codes		V_{IH}	Enabled	V_{IL}	V_{IH}	See Figure 5	X	Note 8	High Z[7]
Read Query		V_{IH}	Enabled	V_{IL}	V_{IH}	See Table 7	X	Note 9	High Z[7]
Read Status (WSM off)		V_{IH}	Enabled	V_{IL}	V_{IH}	X	X	D_{OUT}	
Read Status (WSM on)		V_{IH}	Enabled	V_{IL}	V_{IH}	X	X	$DQ_7 = D_{OUT}$ $DQ_{15–8}$ = High Z $DQ_{6–0}$ = High Z	
Write	6,10,11	V_{IH}	Enabled	V_{IH}	V_{IL}	X	V_{PENH}	D_{IN}	X

NOTES:
1. See Table 2 for valid CE configurations.
2. OE# and WE# should never be enabled simultaneously.
3. DQ refers to DQ_0–DQ_7 if BYTE# is low and DQ_0–DQ_{15} if BYTE# is high.
4. Refer to *DC Characteristics*. When $V_{PEN} \le V_{PENLK}$, memory contents can be read, but not altered.
5. X can be V_{IL} or V_{IH} for control and address pins, and V_{PENLK} or V_{PENH} for V_{PEN}. See *DC Characteristics* for V_{PENLK} and V_{PENH} voltages.
6. In default mode, STS is V_{OL} when the WSM is executing internal block erase, program, or lock-bit configuration algorithms. It is V_{OH} when the WSM is not busy, in block erase suspend mode (with programming inactive), program suspend mode, or reset/power-down mode.
7. High Z will be V_{OH} with an external pull-up resistor.
8. See Section 3.6 for read identifier code data.
9. See Section 4.2 for read query data.
10. Command writes involving block erase, program, or lock-bit configuration are reliably executed when $V_{PEN} = V_{PENH}$ and V_{CC} is within specification.
11. Refer to Table 4 for valid D_{IN} during a write operation.

命令时钟周期

Table 4. Intel® StrataFlash™ Memory Command Set Definitions[1]

Command	Scalable or Basic Command Set[2]	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
				Oper[3]	Addr[4]	Data[5,6]	Oper[3]	Addr[4]	Data[5,6]
Read Array	SCS/BCS	1		Write	X	FFH			
Read Identifier Codes	SCS/BCS	≥ 2	7	Write	X	90H	Read	IA	ID
Read Query	SCS	≥ 2		Write	X	98H	Read	QA	QD
Read Status Register	SCS/BCS	2	8	Write	X	70H	Read	X	SRD
Clear Status Register	SCS/BCS	1		Write	X	50H			
Write to Buffer	SCS/BCS	> 2	9, 10, 11	Write	BA	E8H	Write	BA	N
Word/Byte Program	SCS/BCS	2	12,13	Write	X	40H or 10H	Write	PA	PD
Block Erase	SCS/BCS	2	11,12	Write	BA	20H	Write	BA	D0H
Block Erase, Program Suspend	SCS/BCS	1	12,14	Write	X	B0H			
Block Erase, Program Resume	SCS/BCS	1	12	Write	X	D0H			
Configuration	SCS	2		Write	X	B8H	Write	X	CC
Set Block Lock-Bit	SCS	2		Write	X	60H	Write	BA	01H
Clear Block Lock-Bits	SCS	2	15	Write	X	60H	Write	X	D0H
Protection Program		2		Write	X	C0H	Write	PA	PD

控制寄存器定义

Table 16. Status Register Definitions

WSMS	ESS	ECLBS	PSLBS	VPENS	PSS	DPS	R
bit 7	bit 6	bit 5	bit 4	bit 3	bit2	bit 1	bit 0
High Z When Busy?	Status Register Bits				Notes		
No	SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy				Check STS or SR.7 to determine block erase, program, or lock-bit configuration completion. SR.6–SR.0 are not driven while SR.7 = “0.”		
Yes	SR.6 = ERASE SUSPEND STATUS 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed						
Yes	SR.5 = ERASE AND CLEAR LOCK-BITSSTATUS 1 = Error in Block Erasure or Clear Lock-Bits 0 = Successful Block Erase or Clear Lock-Bits				If both SR.5 and SR.4 are “1”s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.		
Yes	SR.4 = PROGRAM AND SET LOCK-BIT STATUS 1 = Error in Setting Lock-Bit 0 = Successful Set Block Lock Bit						
Yes	SR.3 = PROGRAMMING VOLTAGE STATUS 1 = Low Programming Voltage Detected, Operation Aborted 0 = Programming Voltage OK				SR.3 does not provide a continuous programming voltage level indication. The WSM interrogates and indicates the programming voltage level only after Block Erase, Program, Set Block Lock-Bit, or Clear Block Lock-Bits command sequences.		
Yes	SR.2 = PROGRAM SUSPEND STATUS 1 = Program suspended 0 = Program in progress/completed						
Yes	SR.1 = DEVICE PROTECT STATUS 1 = Block Lock-Bit Detected, Operation Abort 0 = Unlock				SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates the block lock-bits only after Block Erase, Program, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set. Read the block lock configuration codes using the Read Identifier Codes command to determine block lock-bit status.		
Yes	SR.0 = RESERVED FOR FUTURE ENHANCEMENTS				SR.0 is reserved for future use and should be masked when polling the status register.		