

1. Describe the three key concepts of the von Neumann architecture.

Sol. (1) Central Processing Unit (CPU):

→ The brain of the computer, responsible for executing instructions.

→ Comprises of several key components:

- Control Unit (CU): Manages processor control signals, directing I/O flow etc.

- Arithmetic & Logic Unit (ALU): Handles calculations and logical operations.

- Registers: High speed storage areas within the CPU.

(2) Main Memory Unit:

→ stores data as well as instructions

→ Programs and data share same memory space.

→ stored program concept enables easier programming.

(3) Input/Output (I/O) Devices:

→ facilitate comm' b/w the computer and external world

→ Ex: Keyboards, displays, printers etc.

2. Discuss the two approaches for handling multiple interrupts.

Soln: (1) Disable Interrupts:

→ In this method, whenever an interrupt occurs, the processor temporarily disables all further interrupts.

→ This ensures the current interrupt is handled without being interrupted by another.

→ Once the first interrupt's Service Routine (ISR) finishes, the processor re-enables interrupts.

→ Advantage: Simple to implement, avoids complex interrupt nesting scenarios.

→ Disadvantage: Can lead to latency issues.

(1) Interrupt Priority:

- This approach assigns priorities to different interrupts.
- A higher-priority interrupt can interrupt a lower priority interrupt that is currently being serviced.
- The processor stores the state of the lower-priority ISR and jumps to the higher priority one.
- **Advantages:** Ensures timely handling of critical interrupts.
- **Disadvantages:** More complex to implement compared to disabled interrupts.

3. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a. What is the maximum directly addressable memory capacity (in bytes)?

Soln: One byte = reserved for opcode

remaining 3 bytes ($32\text{ bits} - 8\text{ bits}\right) = 24\text{ bits}$

so, maximum addressable memory capacity

$$= 2^{(\text{no. of addressable bits})} = 2^{24} \text{ bytes} \approx 16 \text{ MB.}$$

b. Discuss the impact on the system speed if the microprocessor bus has:

1. 32-bit local address bus and a 16-bit local data bus

2. ^{or} 16-bit local address bus and a 32-bit local data bus.

Soln. (1) 32-bit address bus & 16-bit data bus:

Advantage: Wider address bus allows accessing the full 16 MB memory.

Disadvantage: Narrower data bus means it takes two transversals to fetch a complete 32-bit instruction. This can slow down instruction fetching compared to wider data bus.

(ii) 16-bit address bus and 16-bit data bus:

Advantage: Single transfer can fetch a complete instruction due to matching data bus width.

Disadvantage: significantly limited address space.

(2^{16} bytes = 64 KB). Most programs would exceed their memory limit.

c. How many bits are needed for the program counter and the instruction register?

Solⁿ: Both the program counter (PC) and instruction register (IR) need to hold a complete 32-bit instruction. Therefore, they both require 32 bits.

4. Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32-bits long, 40% are 16 bits long, and 40% are 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor.

Solⁿ: The improvement achieved when fetching instructions and operands using a 32-bit microprocessor as compared to a 16-bit microprocessor

Given : 20% Instructions 32 bits long
40% Instructions 16 bits long
40% Instructions 8 bits long

<u>16-bit (no. of bus cycle)</u>	<u>Instruction length</u>	<u>32-bit (no. of bus cycle)</u>
2 bus cycles	32-bit	1 bus cycle
1 cycle	16-bit	0.5 cycle
0.5 cycle	8-bit	0.25 cycle

Avg: $20\% \times 2 + 40\% \times 0.5 + 40\% \times 0.5 = 1.2$ bus cycles

Avg: $20\% \times 1 + 40\% \times 0.5 + 40\% \times 0.25 = 0.7$ bus cycles

So, improvement is $1.02 - 0.7 = 0.5$ bus cycles/instruction
 In percentage terms, the improvement is $\frac{0.5}{1.02} \times 100 = 41.67\%$.

5. What are the advantage and disadvantage of the logical cache over the physical cache?

Logical Cache (Virtual)

Advantages:

- Faster access due to avoiding MMU translation
- Simple cache design

Disadvantages

- More complex MMU with translation cache
- Cache coherence challenges in multiprocessor systems.

Physical Cache

Advantages:

- Simpler cache coherence
- Reduced MMU overhead

Disadvantages:

- Slower access due to MMU translation
- More complex cache design with internal translation

6. A cache memory unit with capacity of N words and block size of B words is to be designed. If it is designed as direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a 16-way set-associative cache, the length of the TAG field is _____ bits.

Solⁿ: Cache size = N words

No. of bits to address cache size = $\log_2 N$

Block size = B words | No. of blocks in Cache = N/B

Block offset = $\log_2 B$ | No. of bits to represent block = $\log_2(N/B)$

No. of sets in cache = $(N/B)/16$ | Length (direct) = 10 bits

Bits to represent sets = $\log_2((N/B)/16)$ | Length (set-associative) = x

Here direct mapped cache is compared with set associative cache, but in both block offset is same.

$$\text{so, } 10 + \log_2(\frac{N}{B}) = x + \log_2(\frac{N}{B}/16)$$

$$10 + \log_2(\frac{N}{B}) = x + \log_2(\frac{N}{B}) - \log_2 16$$

$$10 = x - 4 \Rightarrow x = 14. \text{ Length of bits} = 14 \text{ for set-associative}$$

7. On 8-way set associative cache of size 64 KB ($1 \text{ KB} = 1024 \text{ bytes}$) & used in a system with 32-bit address. The address is sub-divided into TAG, INDEX and BLOCK OFFSET. The number of bits in the TAG is _____.

Soln: System is 32-bit address

$$\begin{aligned}\text{Cache size} &= 64 \text{ KB} = 64 \times 1024 \text{ Bytes} \\ &= 2^6 \times 2^{10} = 2^{16}\end{aligned}$$

$$\text{So Cache bits} = 16$$

$$\text{So, Tag bits} = 32 - 16 = 16 \text{ bit}$$

As, cache is 8-way set associative. So, we have to transfer 3 bits to tag side.

$$\text{So, final Tag bits} = 16 + 3 = 19.$$

$$\text{No. of bits in Tag field} = 19.$$

8. For the hexadecimal main memory addresses 111111, 666666, BBBB BBB, show the following information, in hexadecimal format :

a. Tag, Line, and Word values for a direct mapped cache, using the format of fig 4.10.

Soln: Acc to figure 4.10, the field lengths are:
tag - 8 bits, line - 14 bits, word - 2 bits

	Tag	Line	Word
111111	11	444	1
666666	66	1999	2
BBBB BBB	BB	2EEE	3

b. Tag and word values for an associative cache, using the format of figure 4.12.

Soln: According to fig 4.12, the field lengths of associative cache are

Tag = 22 bits, word - 2 bits

	Tag	word
111111	444444	1
666666	1999999	2
B BBBB B	2 EEEEEE	3

c. Tag, set, and Word values for a two-way set associative cache using the format of fig 4.15

Soln: Acc. to fig 4.15, the field lengths of set-associative cache are

Tag - 9 bits, set - 13 bits, word - 2 bits

	Tag	set	Word
111111	22	444	1
666666	CC	1999	2
B BBBB B	177	EEE	3