SI.No.	Lessame/Tonics to be sovered	Book Reference
31.NO.	Lessons/Topics to be covered	(sections)
1	Organization and Architecture.	WS 1.1 (pg.26-
2	Structure and Function.	WS 1.2 (pg.27-
		WS 1.5 &
3	Embedded Systems and Cloud Computing.	WS 1.7 (pg.53-
		57 & pg. 63-66)
	Lab#0: Introduction to 8086 microprocessor - Architecture	
4	(Execution unit, Bus interface unit, Register organization) and Evolution	
	of x86 processor.	
5	Designing for Performance Multicore, MICs, and GPG-PUs.	WS 2.1-2.2
		(pg.69-77)
6	Two Laws that Provide Insight: Amdahl's Law and Lit-tle's Law.	WS 2.3 (pg.77-
7	Basic Measures of Computer Performance.	WS 2.4 (pg.80-
8	Lab#1: Analyze the Arithmetic and logical operations using different	
	Addressing Modes of the 8086 Micropro-cessor	
9	Calculating the Mean.	WS 2.5 (pg.83-
10	Calculating the Mean.	WS 2.5 (pg.83-
11	Computer components & Computer Function (Instruc-tion fetch and	WS 3.1-3.2
	Execute).	(pg.105-113)
12	Lab#2: Analyze and Evaluate the Branching operation in the 8086	
12	Microprocessor.	
13	Computer Function (Interrupts) and I/O function.	WS 3.2 (pg.113-
13	Computer Function (interrupts) and i/O function.	123)
14	Interconnection Structures Due Interconnection	WS 3.3-3.4
14	Interconnection Structures. Bus Interconnection.	(pg.123-126)
15	Computer Memory System Overview.	WS 4.1 (pg.145-
15	Computer internory system overview.	151)
16	Lab#3: Analyze and Evaluate the Array Operations using 8086	
10	microprocessors.	
17	Cache Memory Principles.	WS 4.2 (pg.152-
	Cache Memory Filliciples.	155)
18	Elements of Cache Design (Direct mapping).	WS 4.3 (pg.155-
16	Liements of Cache Design (Direct mapping).	162)
19	Elements of Cache Design (Associative and set-associative	LU 4.3 (pg.162-
	mapping).	168)
20	Lab#4: Evaluate Different Arithmetic Operations and Logical	
	operations on two 32-bit data using ARM pro-cessor	
21	Semiconductor Main Memory (DRAM,SRAM and Types of ROM)	WS 5.1 (pg.190-
		194)
22	Error Correction.	WS 5.2 (pg.198-
	2.10. correction.	204)
23	Error Correction.	WS 5.2 (pg.198-
		204)
24	Lab#5: Analyze and evaluate different Array operations using ARM	
25	RAID	WS 6.2 (pg.228-
		236)
26	RAID	WS 6.2 (pg.228-
		236)
27	External devices (Classification) and I/O modules (Mod- ule function, I/O	WS 7.1-7.2
	module structure).	(pg.254- 259)
28	Lab#6: Interfacing Seven Segment Display with 8086 processor.	

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