Assignment-4

1) DRAM

→ DRAM is made with cells that store data as charge on capacitors.

→ The absence or presence of charge in a capacitor is interpreted as a binary 0 or 1.

→ It is requires periodic charge refreshing to maintain the data.

→ This refresh process can slow down the overall speed of computer

SRAM

→ SRAM is a digital device that uses the same logic element used in processor.

→ Store binary data using traditional flip-flop logic gate configuration.

→ SRAM is much faster than dynamic ram. and hold its data as long as power is supplied.

2) Types of ROM

Memory Type	Category	Erasure	Write mechanism	Volatility
MROM	Read only memory	Not possible	Masks	Non volatile
PROM (Programmable ROM)	Read only memory	not possible	Electrically	Non volatile
Erasable PROM (EPROM)	Read mostly memory	UV light chip level	Electrically	non volatile
Electrically Erasable PROM (EEPROM)	Read mostly memory	Electrically byte-level	Electrically	non volatile
Flash memory	Read mostly memory	Electrically block-level	Electrically	non volatile

(3) In hamming code

→ If the syndrome contains all zeros, no error is detected.

→ If the syndrome contains one and only one bit set to 1, then the error has occured in one of the check bits. No error correction is needed.

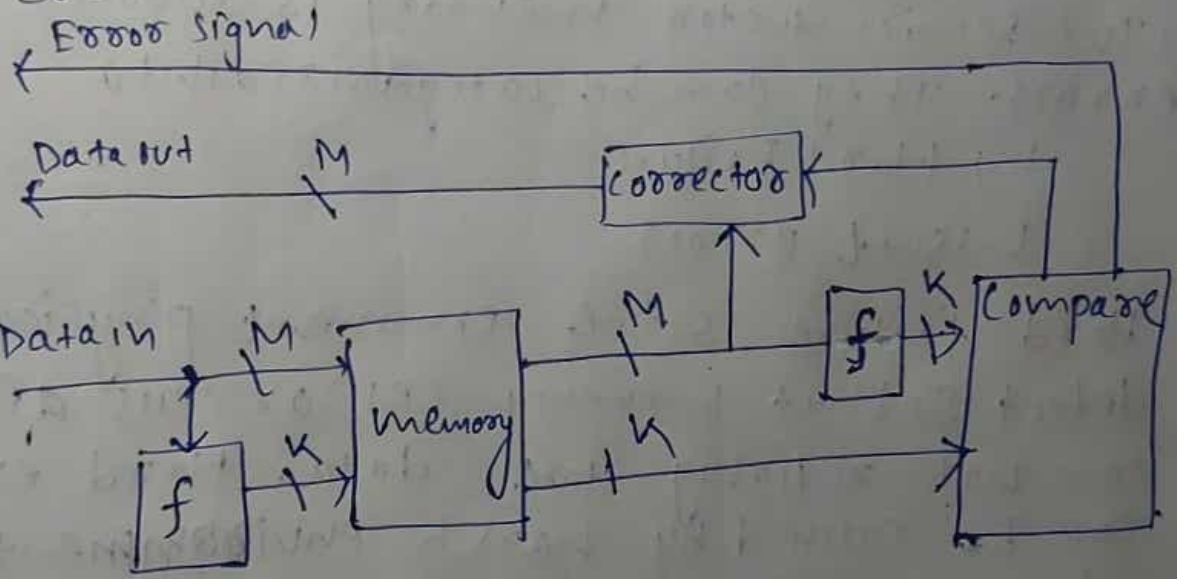
→ If the syndrome contains more than one bit set to 1, then the numerical value of the syndrome indicates the position of the data bit in error. This data bit is inverted for correction.

vi) → When data are to be written into memory, a calculation is performed on the data to produce a code.

→ Code is stored along with the word in memory.

→ Code is used to identify and correct errors.

→ When the word is fetched a new code is generated and compared to the stored code.



Name:

Regd. Number:

(5) Soln

A decoder with k input lines has 2^k output line

So if memory is 1KB

$\hookrightarrow 2^{10}$ B

no of input lines (m) = 10

Number of output lines (n) = $2^m = 1024$

m+n = 10 + 1024 = 1034.

Ans

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Q6)

M = 1 1 0 0 0 0 1 0
D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1

M = 8 so
k = 4 (using $2^{k-1} \geq M+k$)
Total = 8 + 4 = 12

$C_1 = D_1 \oplus D_2 \oplus D_4 \oplus D_5 \oplus D_7$
$= 0 \oplus 1 \oplus 0 \oplus 0 \oplus 1$
$= 0$

$C_2 = D_1 \oplus D_3 \oplus D_4 \oplus D_6 \oplus D_7$
$= 0 \oplus 0 \oplus 0 \oplus 0 \oplus 1 = 1$

$C_4 = D_2 \oplus D_3 \oplus D_4 \oplus D_8$
$= 1 \oplus 0 \oplus 0 \oplus 1 = 0$

$C_8 = D_5 \oplus D_6 \oplus D_7 \oplus D_8$
$= 1 \oplus 0 \oplus 1 \oplus 1 = 0$

Check bit stored

C_8	C_4	C_2	C_1
0	0	1	0

Q7)

M = 0 0 1 1 1 0 0 1

original check bit = 0 1 1 1

New that calculated check bit = 1 1 0 1

XOR OPR = 1 0 1 0

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$(1\,0\,1\,0)_2 = (10)_{10}$, 10th

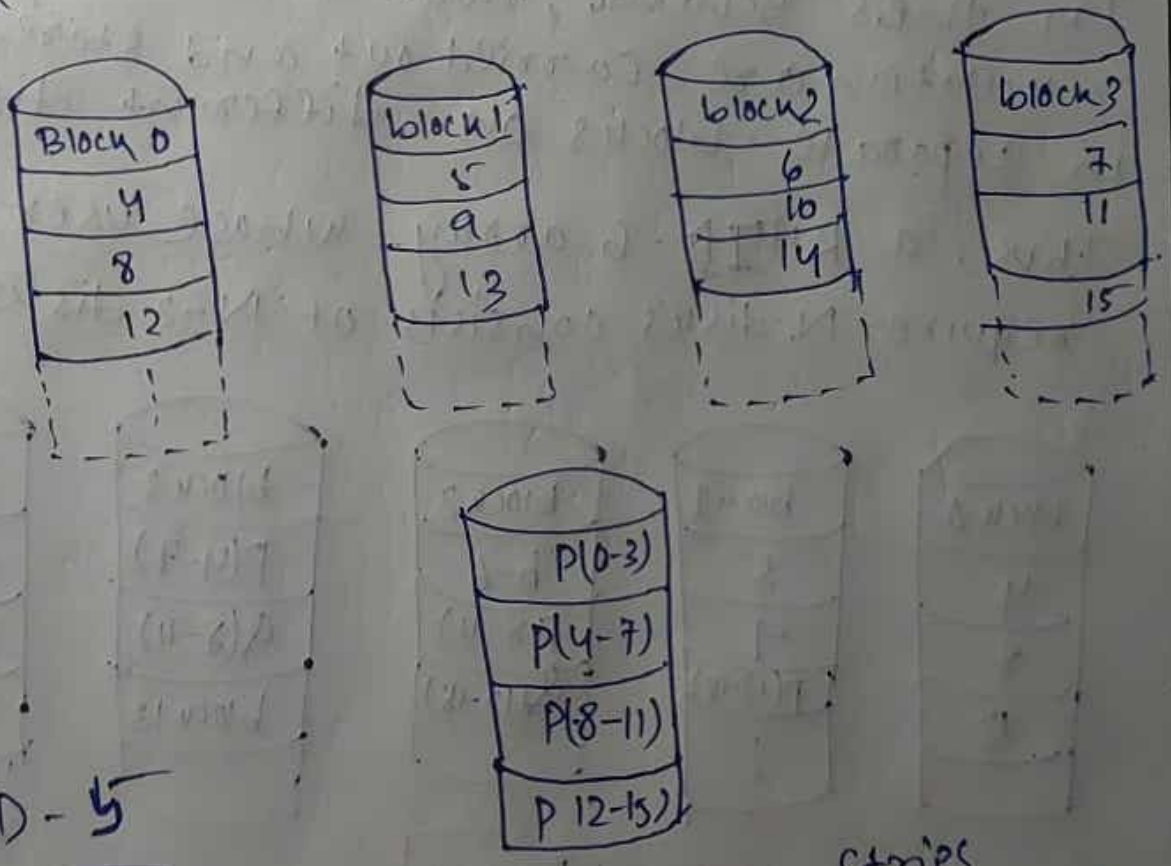
the error will be in the D_6 bit.

Data read from memory = 0 0 0 1 1 0 0 1
D_6 in error

Q8) RAID-4

→ In RAID-4 Disk required = N + 1

1 disk is for parity bit store



RAID-5

→ In RAID-5 the parity bit is distributed among all the disk

strips

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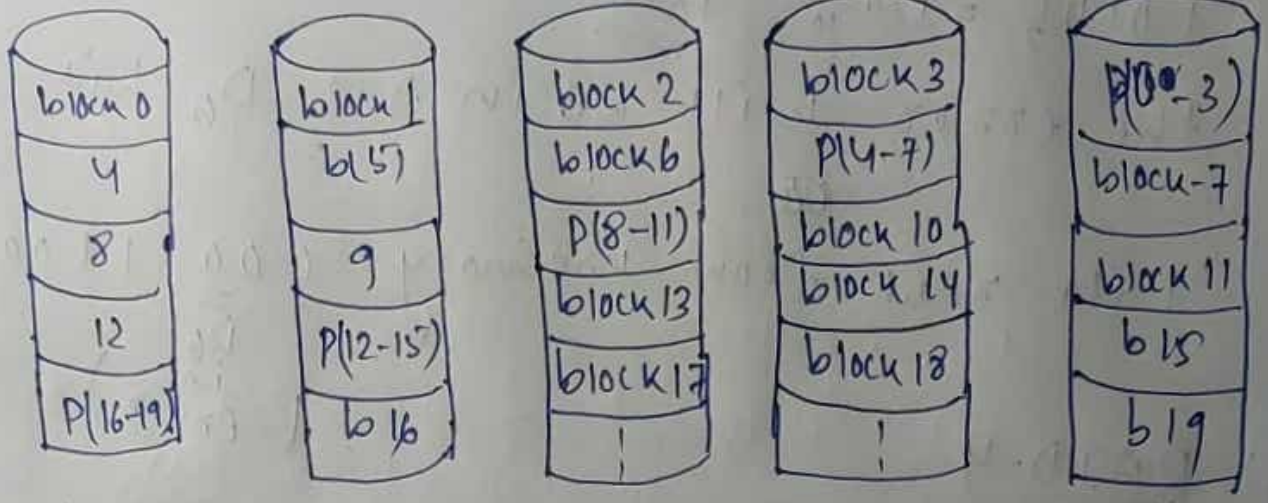
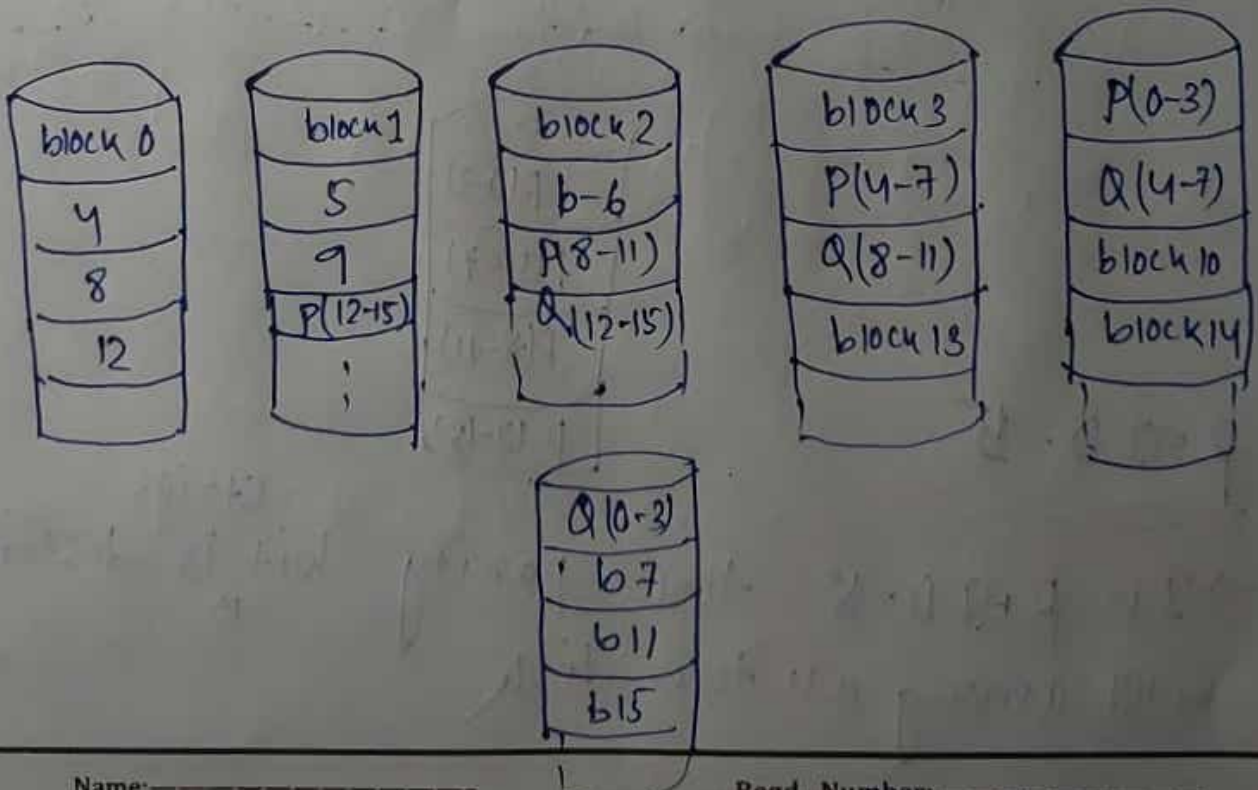


RAID-6

In this scheme, two different parity calculation are carried out and stored in separate blocks on different disks.

Thus, a RAID-6 array whose user data require N disks consists of N-2 disks.



Name:_____ Regd. Number:_____

Q9) 200 GB per drive. 4 drive available

In RAID 0 → 4 * 200 = 800 GB

In RAID 1 → for every strip there is parity strip in different disk

So

(4/2) * 200 = 400 GB

In RAID 3, 4, 5 → there is one disk for parity strips

(4-1) * 200 = 600 GB

In RAID 6 → there is N+2 disk required that means 2 disk for parity bit strip even if they are with data bits

data storage available

(4-2) * 200 = 400 GB

Q10) Major functions of I/O function.

→ Interface to the processor and memory via the system bus or central switch.

→ Interface to one or more peripheral device by tailored data links.

Q11) classification of external devices

↳ Human readable:
Suitable for communicating with the computer user.
eg → Video display terminals (VDTs) and printers.

↳ Machine readable:-
Suitable for communicating with equipment:
Eg → Magnetic disk, sensors and actuators.

↳ communication:
Suitable for communicating with remote devices.
eg → Human readable device such as terminal a machine readable device even another computer.

Q12) [redacted]
Three different mode of operation of 8255A

Mode 0:

This is the basic I/O mode. The three groups of eight external lines function as three 8-bit I/O ports. Each port can be

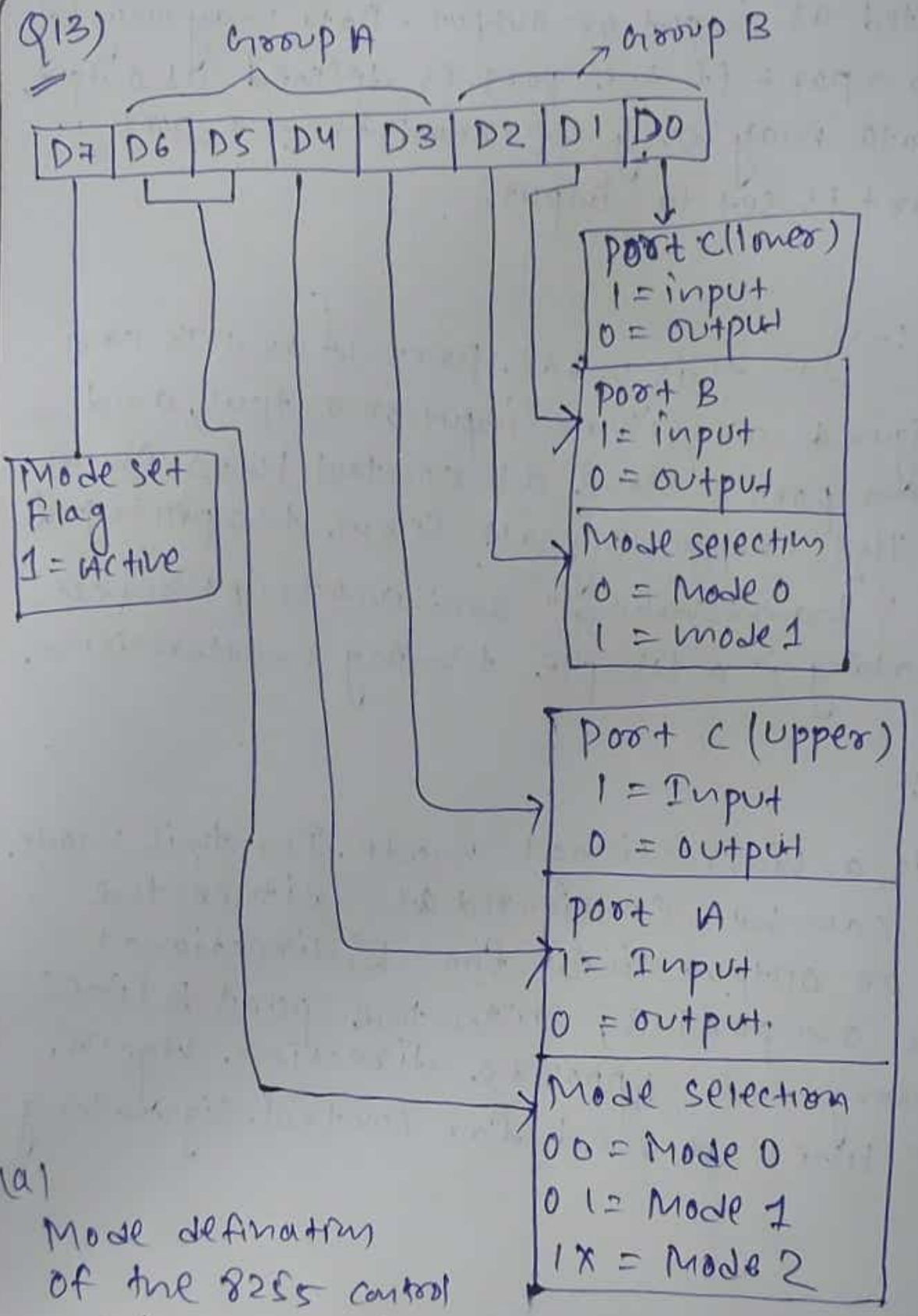
designated as input or output. Data may only be sent to a port if the port is defined as output, and data may only be read from a port if the port is set to input.

Mode 1:→ In this mode, port A and B can be configured as either input or output, and lines from port C serve as control lines for A and B. The control signals serve two principal purpose: "handshaking" and interrupt request. Handshaking is a simple timing mechanism.

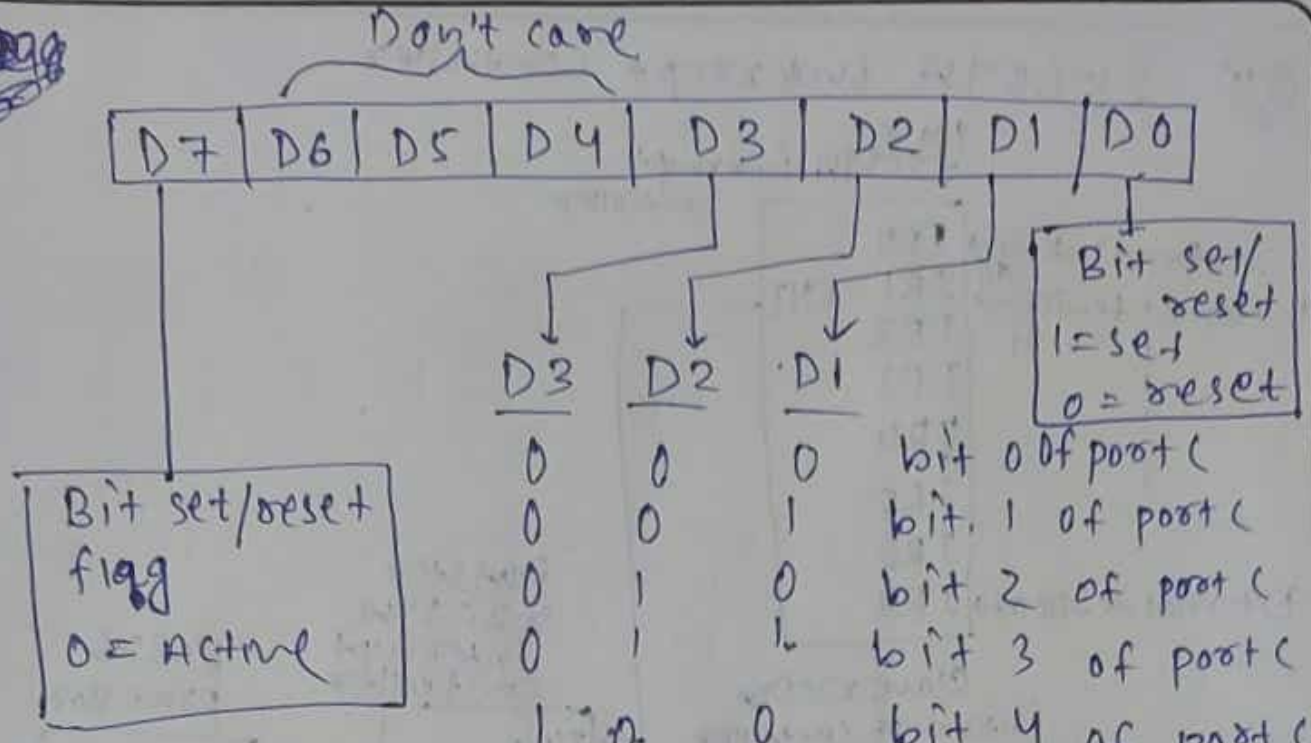
Mode 2:

This is a bidirectional mode. In this mode port A can be configured as either the input or output lines for bidirectional traffic on port B, with the port B lines providing the opposite direction. Again, port C lines are used for control signaling.

Q13)



(a) Mode definations of the 8255 control register to configure the 8255



D3	D2	D1	
0	0	0	bit 0 of port C
0	0	1	bit 1 of port C
0	1	0	bit 2 of port C
0	1	1	bit 3 of port C
1	0	0	bit 4 of port C
1	0	1	bit 5 of port C
1	1	0	bit 6 of port C
1	1	1	bit 7 of port C

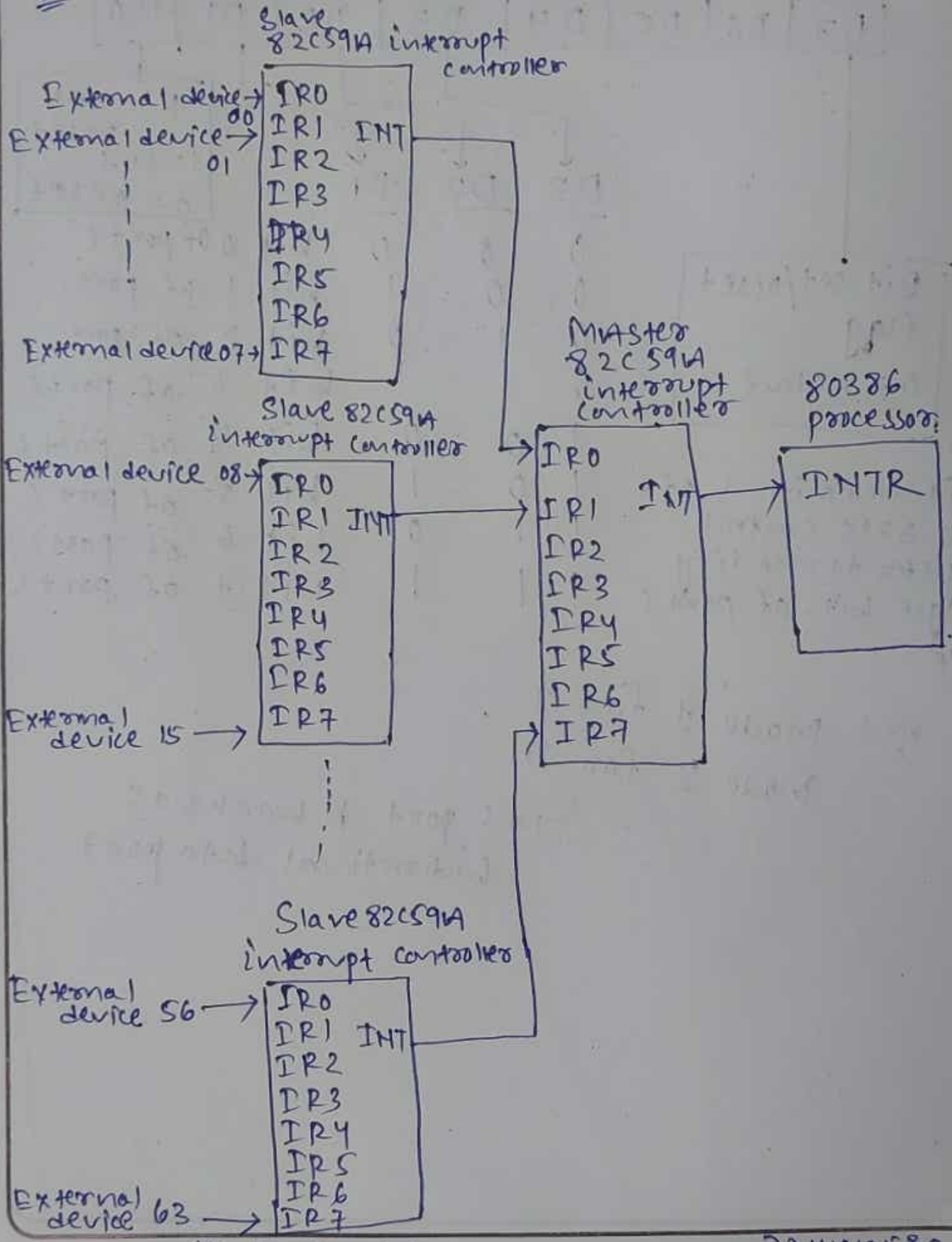
Bit definitions of the 8255 control register to modify single bits of port C

Q14

Ans Mode 1 for I.
Mode 2 for II
↳ as port A works as bidirectional data port

Name:---------- Regd. Number:----------

Q15 85C59A Interrupt Controller



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