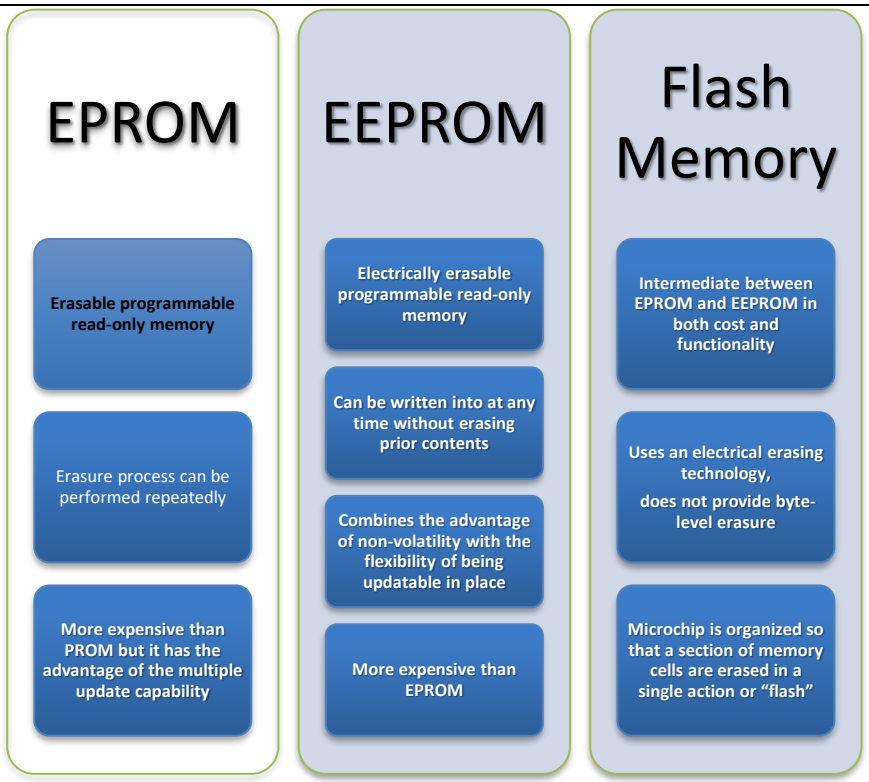
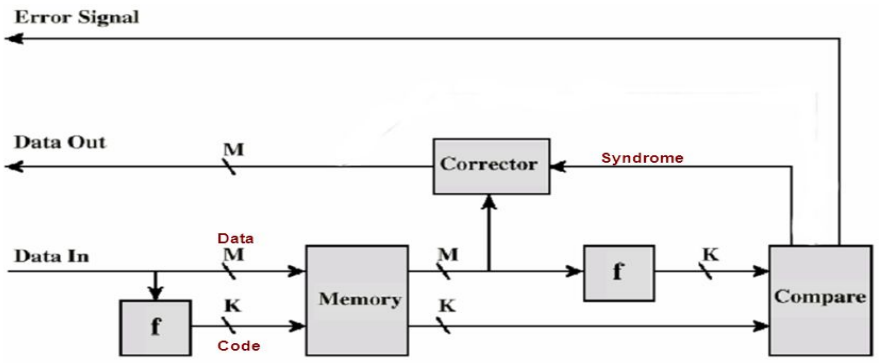
	ITER, SIKSHA 'O' ANUSANDHAN (Deemed to be University)		**Assignment**
Branch	**Computer Science and Engineering**	Programme	**B.Tech**
Course Name	**Computer Organization and Architecture**	Semester	**IV**
Course Code	**EET 2211**	Academic Year	**2023/Even**
Solution of Assignment-4	**Topic-Cache memory, Internal memory, External memory and Input/Output**	**GP-1**	

Learning Level (LL)	**L1**: Remembering	**L3:** Applying	**L5**: Evaluating
	L2: Understanding	**L4**: Analyzing	**L6**: Creating

Q's	Questions	COs	LL
1	What is the difference between DRAM and SRAM in terms of application? Solution:	**CO4**	**L1**

DRAM	**SRAM**
The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0	Traditional flipflop logic gates are used to store binary 1 or 0
Essentially an analog device	Basically, digital devices
Cells are smaller and simpler	Cells are not simpler
More dense	Less Dense
Less expensive	More expensive
Used for main memory	Used for cache memory (both on and off-chip)
Requires the supporting refresh circuitry which Tend to be favoured for large memory	Refresh circuitry is not required

2	Explain different types of ROM. Solution:	**CO4**	**L1**

			
3.	How is the syndrome for the Hamming code interpreted? **Solution:** **The syndrome for the Hamming code is interpreted as follows** • **If the syndrome contains all zeros, no error is detected.** • **If the syndrome contains one and only one bit set to 1(i.e. if parity is corrupted), then the error has occurred in one of the check bits. No error correction is needed.** • **If the syndrome contains more than one bit set to 1,then the numerical value of the syndrome indicates the position of the data bit in error. This data bit is inverted for correction.**	**CO4**	**L2**
4.	Explain the error correction process in the memory system using a suitable diagram. **Solution:** 	**CO4**	**L1**

	• **Prior to storing data, a code is generated from the bits in the word.**
	• **Code is stored along with the data word in memory.**
	• **Code used to identify and correct errors.**
	• **When the word is fetched a new code is generated and compared to the stored code.**
	  • **No errors detected.**
	  • **An error is detected and it is possible to correct the error.**
	  • **An error is detected, but it is not possible to correct it.**		

5.	If there are m input lines n output lines for a decoder that is used to uniquely address a byte addressable 1 KB RAM, then the minimum value of m+n is _____. **(A)** 18 **(B)** 1034 **(C)** 10 **(D)** 1024 **[GATE 2020]** **Solution:** **A Decoder is represented as m x n(2^m) used to identify a byte address of 1KB RAM.** **1KB memory is represented as,** **1 KB = 1K x B = 2^{10} x 8 = 2^m x 8.** **So m = 10** **n= 2^m = 2^{10} = 1024** **so minimum value of m+n = 10+ 1024 = 1034 , option (B)**	**CO4**	**L2**
6.	Suppose an 8-bit data word stored in memory is 11000010. Using the Hamming algorithm, determine what check bits would be stored in memory with the data word. Show how you got your answer. Ans: **1. Length of data word =m=8-bits** **According to inequality condition 2^k -1 ≥ m+k, no of check bits required is 4** **So, k=4-bit (C8, C4, C2, C1)** **Length of codeword=m+k=12-bit** **2. Arrange the data bits and check bits in the cord word** Cord word Position: 12 11 10 9 8 7 6 5 4 3 2 1 Check bits: **C8** **C4** **C2** **C1** Data bits: **D8** **D7** **D6** **D5** **D4** **D3** **D2** **D1** **1 1 0 0 C8 0 0 1 C4 0 C2 C1** **3. Check bits can be determined** **C1= XOR (3,5,7,9,11) = 0** **C2 = XOR (3,6,7,10,11) =1** **C4 = XOR(5,6,7,12) = 0** **C8 = XOR (9,10,11,12) = 0**	**CO4**	**L3**
7	For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read from memory, the check bits are calculated to be 1101. What is the data word that was read from memory?	**CO4**	**L3**

Solution:

Cord word Position	12	11	10	9	8	7	6	5	4	3	2	1
Check bits					**C 8**				**C4**		**C 2**	**C 1**
Data bits	**D8**	**D7**	**D6**	**D5**		**D4**	**D3**	**D2**		**D1**		
	0	**0**	**1**	**1**	**C 8**	**1**	**0**	**0**	**C4**	**1**	**C 2**	**C 1**

Syndrome = K_{old} xor K_{new}
K_{old} = 0111
K_{new} = 1101

So, Syndrome = 0111 (+) 1101 = 1010
Since, Syndrome $\neq 0$, so error has been detected. The position of error is the decimal equivalent of the syndrome i.e. 10. The 10^{th} position of the codeword is in error.

Correct data word is **00011001**

8. Define and compare the RAID 4,5, and 6 levels with suitable diagrams **CO4** **L1**

Solution:

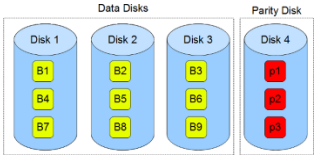
RAID 0: Non-redundant

RAID1: Mirrored; every disk has a mirror disk containing the same data.

RAID 2: Redundant via Hamming code; an error-correcting code is calculated across corresponding bits on each data disk, and the bits of the code are stored in the corresponding bit positions on multiple parity disks.

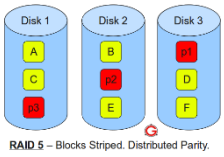
RAID **3:** Bit-interleaved parity; similar to level 2 but instead of an error-correcting code, a simple parity bit is computed for the set of individual bits in the same position on all of the data disks.

RAID **4:** Block-interleaved parity; a bit-by-bit parity strip is calculated across corresponding strips on each data disk, and the parity bits are stored in the corresponding strip on the parity disk.



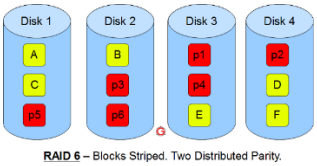
RAID-4: Block-Level Stripping with Dedicated Parity

RAID **5:** Block-interleaved distributed parity; similar to level 4 but distributes the parity strips across all disks.



RAID-5: Block-Level Stripping with Distributive Parity

RAID **6:** Block- interleaved dual distributed parity; two different parity calculations are carried outand stored in separate blocks on different disks.



RAID-6: Block-Level Stripping with Two Distributive Parity

9.	**Consider a 4-drive, 200 GB-per-drive RAID array. What is the available data storage capacity for each of the RAID levels 0, 1, 3, 4, 5, and 6?** **Solution:** **No of disks available =N=4** **Capacity of each disk =200GB** **For RAID level 0, all the disks are used to store data.** **So no of data disk=N= 4** **Data storage capacity = no of data disks * capacity of each disk** **=4*200GB** **= 800GB** **For RAID level 1, no of data disk=N/2= 2** **Data storage capacity = no of data disks * capacity of each disk** **=2*200GB** **= 400GB** **For RAID level 3, no of data disk=N-1= 3** **Data storage capacity = no of data disks * capacity of each disk** **=3*200GB** **= 600GB** **For RAID level 4, no of data disk=N-1= 3** **Data storage capacity = no of data disks * capacity of each disk** **=3*200GB** **= 600GB** **For RAID level 5, no of data disk=N-1= 3** **Data storage capacity = no of data disks * capacity of each disk** **=3*200GB** **= 600GB** **For RAID level 4, no of data disk=N-2= 2** **Data storage capacity = no of data disks * capacity of each disk** **=2*200GB** **= 400GB**	**CO4**	**L2**
10..	What are the major functions of an I/O module? **Solution:** **The major functions of an I/O module are** • **Control and timing** ○ **Coordinates the flow of traffic between internal resources and external devices** • **Processor communication** ○ **Involves command decoding, data, status reporting, address recognition** • **Device communication** ○ **Involves commands, status information, and data** • **Data buffering** ○ **Performs the needed buffering operation to balance device and memory speeds** • **Error detection** ○ **Detects and reports transmission errors**	**CO1**	**L1**

11.	List three broad classifications of external, or peripheral, devices Solution: External device categories • **Human readable:** communicate with the computer user – CRT • **Machine-readable:** communicate with equipment – disk drive or tape drive • **Communication:** communicate with remote devices – may be human readable or machine-readable	**CO1**	**L1**
12.	Explain the different modes of operation of 8255A. Solution: Mode 0: This is the basic I/O mode. Each port (Port A, Port B and Port C) can be designated as input or output port. Data may only be sent to a port if the port is defined as output, and data may only be read from a port if the port is set to input. ■ Mode 1: In this mode, ports A and B can be configured as either input or output, and lines from **port C serve as control lines for A and B.** The control signals serve two principal purposes: "handshaking" and interrupt request. **Handshaking** is a simple timing mechanism. The control lines used are **DATA READY** line, to indicate when the data are present on the I/O data lines, **ACKNOWLEDGE**, indicating that the data have been read and the data lines may be cleared and **INTERRUPT REQUEST** line to send request to the processor for data transfer. ■ Mode 2: This is a bidirectional mode. In this mode**, port A can be configured as either the input or output lines**. Again, port C lines are used for control signaling for Port A only.	**CO1**	**L1**
13.	Suppose that the 8255A is configured as follows: port A as input, port B as output, and all the bits of port C as output. Show the bits of the control register to define this configuration. Solution: **Control word Format of 8255A** **D7 D6 D5 D4 D3 D2 D1 D0** **1 0 0 1 0 0 0 0**	**CO1**	**L2**
14.	The 8255 Programmable Peripheral Interface is used as described below. (i) An A/D converter is interface to a microprocessor through an 8255. The conversion is initiated by a signal from the 8255 on Port C. A signal on Port C causes data to be strobe into Port A. (ii) Two computers exchange data using a pair of 8255s. Port A works as a bidirectional data port supported by appropriate handshaking signals. The appropriate modes of operation of the 8255 for (i) and (ii) would be **(A)** Mode 0 for (i) and Mode 1 for (ii) **(B)** Mode 1 for (i) and Mode 2 for (ii) **(C)** Mode for (i) and Mode 0 for (ii) **(D)** Mode 2 for (i) and Mode 1 for (ii) **[GATE 2004]** **Solution:** **Option (B)**	**CO1**	**L2**

15.	Explain the use of 82C59A interrupt handler to handle up to 64- I/O request using a suitable diagram. Solution: Figure 7.8 of text book.	**CO1**	**L1**