MID-SEMESTER EXAMINATION, MAY-2022
Computer Organization and Architecture (EET 2211)

Programme: B.Tech

Full Marks: 30

Semester: 4th

Time: 2 Hours

Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
Able to explain the concepts that underline the modern computers evolution, function and organization.	L1,L2	Q.1 Q. 4(a), 4(c)	10
Able to identify the appropriate organization of a computer for achieving the best performance when asked to make a selection from the current market.	L2, L3	Q.2, Q. 3	12
Able to demonstrate the flow of an instruction cycle.	L1, L3,L4	Q. 4(b), Q.5	8

*Bloom's taxonomy levels: Knowledge (L1), Comprehension (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries equal mark.

1. (a) List and briefly explain the basic function of a computer. — 2

   (b) Distinguish between microprocessor and microcontroller. — 2

   (c) Briefly explain the services provided by the cloud computing. — 2

2. (a) Describe the pipeline architecture. Also discuss the advantages of pipeline architecture. 2

(b) Briefly explain the factors affecting the processor speed. 2

(c) Examine the speed of the processor with respect to system clock. Define the term clock rate and clock cycle time. 2

3. (a) Explain the limitation of high clock speed and high logic density. 2

(b) Explain Amdahl's law with suitable diagram. 2

(c) A benchmark program is run on a 200 MHz. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count: 2

Instruction Type	Instruction Mix (%)	CPI
Arithmetic & Logic	50	2
Data transfer	15	2
Control transfer	15	1
others	20	3

Determine the effective CPI, MIPS rate and execution time.

4. (a) Describe the three key concepts of Von Neumann Architecture. 2

(b) Explain different states of instruction cycle with a suitable diagram. 2

(c) With proper diagram, compare the two approaches used for handling multiple interrupts. 2

5. (a) Describe five addressing mode of 8086 microprocessor with suitable example. 2

(b) Using the instruction set of 8086 microprocessor, write an assembly program to add two 16-bit data which are 2

available in the memory location 400h and 500h and store the result in 600h using register indirect addressing mode.

(c) i) Analyze the content of registers and memory location   2
    of the given sequence of code.
    MOV BX, 1004H
    MOV AX,23F4H
    MOV [BX], AX
    ADD AX,BX
    HLT

ii) State the physical address calculation of the operand in 8086 Microprocessor.

End of Questions