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E344 Assignment 1

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Report submitted in partial fulfilment of the requirements of the module
Design (E) 344 for the degree Baccalaureus in Engineering in the Department of Electrical
and Electronic Engineering at Stellenbosch University.

August 15, 2021

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MC van der Berg Voorletters en van / *Initials and surname*	August 15, 2021 Datum / *Date*

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Nomenclature

Variables and functions

V	Voltage over the module
V_{oc}	Open source voltage
V_{STC}	Standard test condition voltage
$V_{T-coeff}$	Temperature Coefficient of V_{oc}
I	Current flowing threw the module
I_{sc}	Short circuit current
P	power output of the module
P_{max}	Maximum power
P_{STC}	Standard test condition power
T_{cell}	Temperature of the cell

Acronyms and abbreviations

PV	Photovoltaic
STC	Standard Test Conditions
MPPT	Maximum power point tracking

Chapter 1

Solar photovoltaic cells and solar modules

1.1. The photovoltaic effect

A PV cell is an energy harvesting technology, that converts solar energy into electricity through the photovoltaic effect (PV). The photovoltaic cell is a specially treated semi-conductor layer [1]. This layer consists of two other layers: the p-type and n-type layer, forming a pn-junction. The pn-junction converts the sun's energy into useful electricity through a process called the photovoltaic effect. Electrons move to the positive p-type side, and holes move to the negative n-type side. This creates a depletion region. When sunlight hits the depletion region; photons energise the atoms and separate holes and electrons. These holes and electrons are then pulled away from each other by the existing electric field. If the pn-junction is connected into a circuit, the electrons will flow from the n-type side through the circuit to the p-type side. Therefore, a current will be present [4].

A photovoltaic cell is however not ideal. In practise it can only convert a percentage of the solar energy it receives into electrical energy. The average efficiency of a solar panel is between 17 to 19 percent. This could be due to the material of the panel component, the reflective efficiency, and Thermodynamic efficiency [5] .

1.2. The I-V-curve

A photovoltaic cell has a I-V curve that indicates the relationship between the voltage and the current of the cell under certain conditions. This relationship is almost parallel with the Voltage axis. The knee of this curve drops drastically until the curve is in an open-circuit state and the voltage is equal to the open-circuit voltage. This drop represents the current that is produce if more voltage is introduced [2].
The open-circuit voltage VOC is the maximum voltage attainable by a photovoltaic cell. This voltage will be reached when the circuit is in an open circuit configuration, therefore the current will be zero illustrated in Figure 1.2. The value however is not fixed for a cell, as many factors may change this value like discussed in section 1.3. The open circuit voltage of a single cell is typically 0.6V [?]. Our specific solar module has a VOC = 21.6V [3]. The photovoltaic cell has a short circuit configuration where the voltage over the cell is Zero, but maximum current is flowing through the circuit. This maximum current is denoted as Isc in Figure 2.1. The short-circuit current is a result of light-generated carrier that are gathered

by the cell. For ideal solar cells, the short-circuit current is identical to the light-generated current. There are many factors that influence the short-circuit value such as, the area of the cell, the number of photons, the spectrum of the incident light, the optical properties and the collection probability. Our specific solar module has a Isc = 0.34A [3]. This is not very large, but these cells are connected in series with one another to produce a larger voltage value. These are called solar modules. Our specific module has 36 cells in series with one another [?]

Illustrated in Figure 1.2, the equation P = IV can be used to calculate a power curve. The maximum power will be produced when the voltage is regulated to be at the knee of the IV-curve, however the IV-curve is not static and may change due to many factors as mentioned above. As a result, the maximum power point is not static and has to be tracked to optimise the power efficiency of the solar cell. This is known as maximum power point tracking or MPPT [6].. Our specific solar module has a Pmax = 5W [3].

1.3. Standard Test Conditions

All PV module manufacturers must test the modules they produce. These manufacturers do this by implementing the standard test conditions (STC). The three main elements that are tested are temperature, irradiance, and air mass [7].

Temperature: the efficiency of the cell decreases as the cell temperature increases. The STC for cell temperature is 25 $°C$. The change in temperature and the effect thereof can be calculated by doing the following calculations:

$$V = V_{STC} + V_{T-coeff} * (T_{cell} - 25)$$

$$P = P_{STC} + P_{T-coeff} * (T_{cell} - 25)$$

Irradiance represents the power output of the sun per unit area. The STC value for irradiance is 1000W/m2. This value may range from 0W/m2 to 1250W/m2. Higher irradiance leads to higher current values flowing through the module.

Air mass:represents the amount of atmosphere the sunlight must pass through before reaching the earth. The STC value of Air mass is 1.5 AM. This value may range allot depending on location, time of year and time of day.

Chapter 2

Lead acid batteries

Chapter 3

High-side switching circuit

3.1. Intro

A High-side switch will be designed that must switch between 0V and 25V. The transistor will be placed between the source voltage (25V) and the load. The arduino that will be used for this report has a GPIO output of 5V. This value is not high enough to force the single PMOS into saturation. Therefore the design will consist of a high-side PMOS transistor as well as a NMOS driver transistor [8].

The voltage over the load will be 25V when the PMOS transistor is in cut off mode. For this to occur the NMOS transistor is in saturation mode. This will only happen when the arduino output GPIO is high. A schottky diode is placed between the PMOS and the supply voltage. This will allow the load voltage to remain a constant 25V after Vloadon and the supply voltage is turned off. A pull-up resistor Rc will also be addedJames:2018.

3.2. Design

When designing the most important information is to how much voltage is required to drive the transistor into saturation (the transistor is on) or in other words when will I_D become significant and for what voltage will the transistor be in cut off (the off state). Because the arduino outputs a 5V the I_D is 250mA) roughly. Using this value we calculate the minimum value of Rc_min to be 30 . We use Rc = 100 . A 50 resistor is placed in front of the NMOS transistor for protection. The schottky diode is placed as mentioned above.

3.3. Results

Vsupply indicates the source voltage of 25V.It is turned off at t = 1.5 seconds.Vloadon is the arduino 5V output.This voltage is turned on for the time period between t = 0.5 seconds and t = 1 seconds.Vload is the voltage over the load. THe load receives 25V as soon as the Vloadon goes high at t = 0.5s. The voltage over the load stays 25V no matter if Vloadon is turned off or Vsupply is turned off. Thus this design meets all the design requirements.

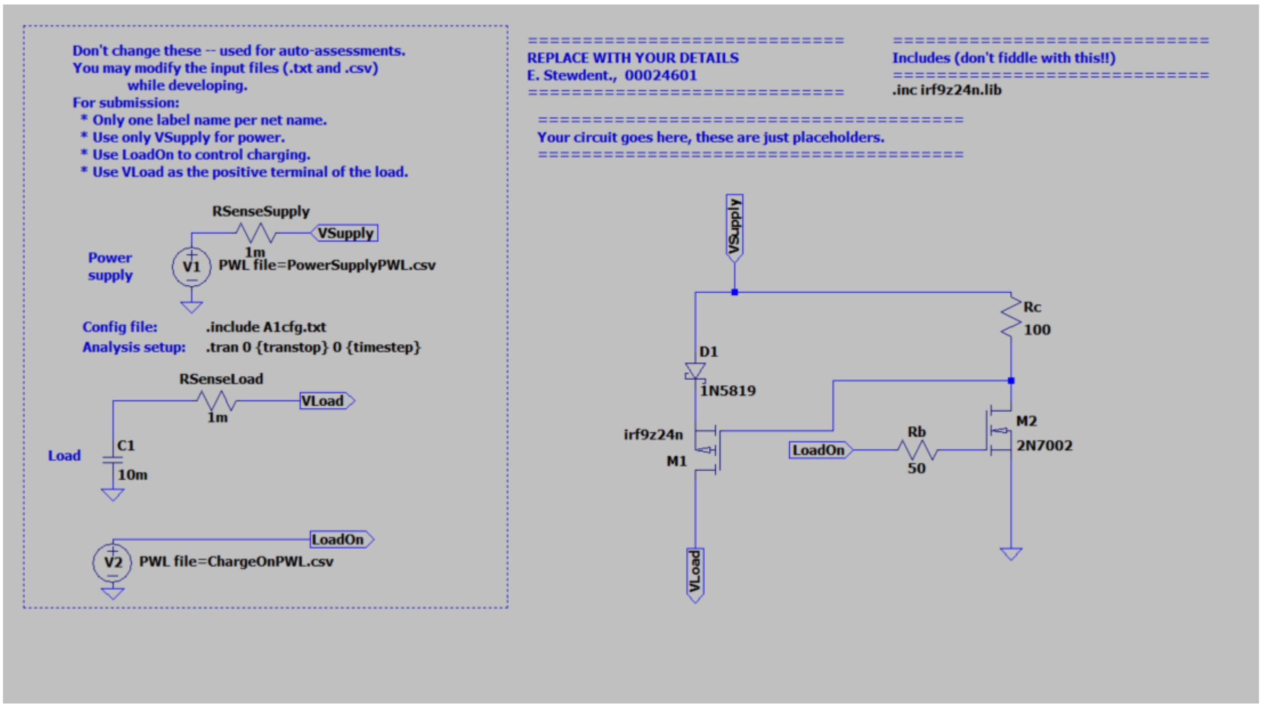

Figure 3.1: The switch design

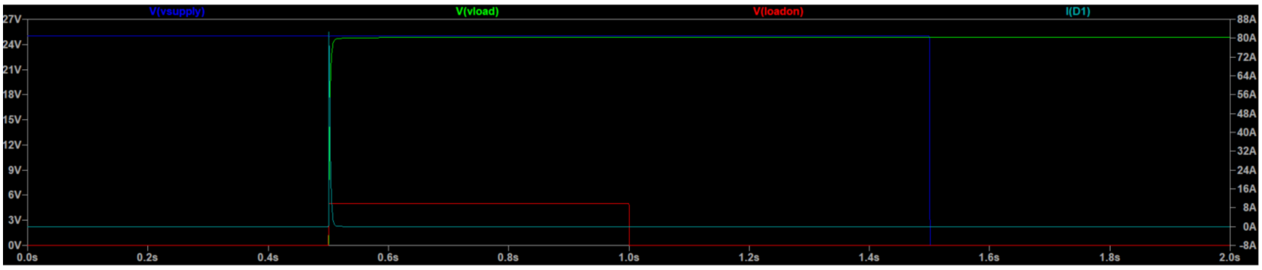

Figure 3.2: This is my caption, make me descriptive! And cite if you borrow figures

3.4. Summary

The switch works as indicated above. It is important to note that this switch is triggered by a low voltage and produces a larger voltage. This makes the switch highly effective and efficient as less power could thus be used to control circuits that require higher voltages. The switch that was designed above is a very simple design and there are many more factors that could be incorporated into the design that will complicated the circuit allot more.

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Appendix A

Social contract

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E-design 344 Social Contract

2021

The purpose of this document is to establish commitment between the student and the organisers of E344. Beyond the commitment made here, it is not binding.

In the months preceeding the term, the lecturer (Thinus Booysen) and the Teaching Assistant (Kurt Coetzer) spent countless hours to prepare for E344 to ensure that you get your money's worth and that you are enabled to learn from the module and demonstrate and be assessed on your skills. We commit to prepare the assignments, to set the tests and assessments fairly, to be reasonably available, and to provide feedback and support as best and fast we can. We will work hard to give you the best opportunity to learn from and pass analogue electronic design E344.

I, MC van der Berg have registered for E344 of my own volition with the intention to learn of and be assessed on the principals of analogue electronic design. Despite the potential publication online of supplementary videos on specific topics, I acknowledge that I am expected to attend the scheduled lectures to make the most of these appointments and learning opportunities. Moreover, I realise I am expected to spend the additional requisite number of hours on E344 as specified in the yearbook.

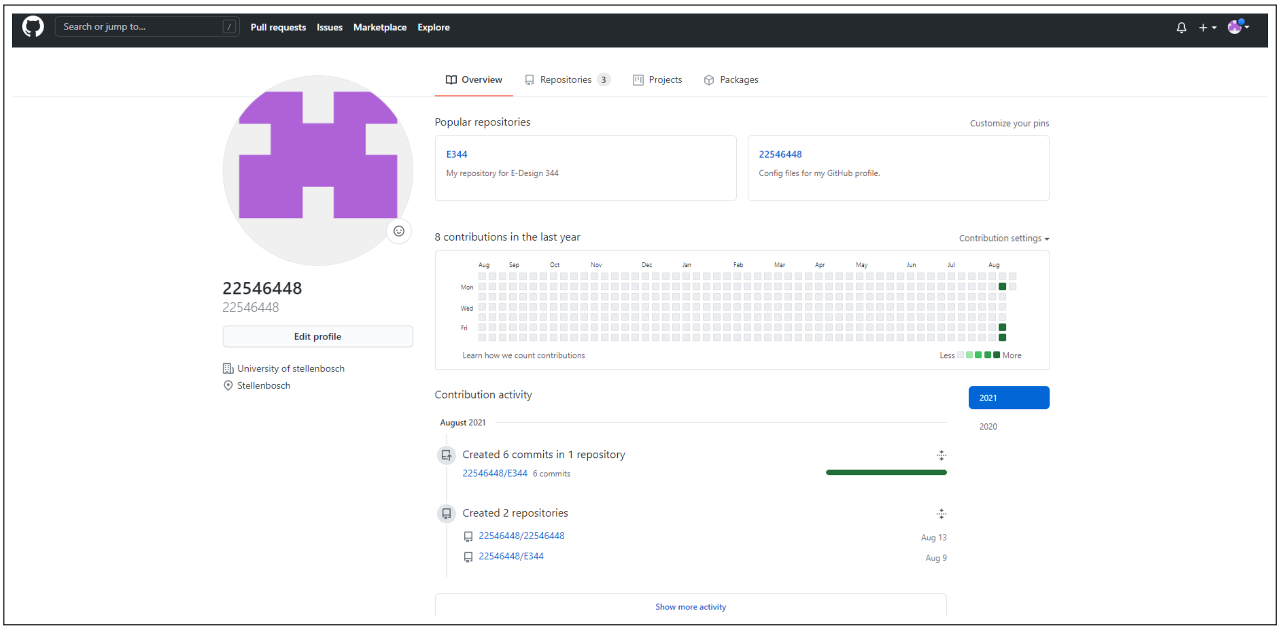
I acknowledge that E344 is an important part of my journey to becoming a professional engineer, and that my conduct should be reflective thereof. This includes doing and submitting my own work, working hard, starting on time, and assimilating as much information as possible. It also includes showing respect towards the University's equipment, staff, and their time.

Prof. MJ Booysen	Student number: 22546448
Signature: Digitally signed by MJ BOOYSEN Date: 2021.08.04 22:12:45 +02'00'	Signature: Michiel Christiaan van der Berg Digitally signed by Michiel Christiaan van der Berg Date: 2021.08.16 00:28:10 +02'00'
Date: 4 Aug 2021	Date: 15 Augustus 2021

1

Appendix B

GitHub Activity Heatmap



Appendix C

Extra Figures

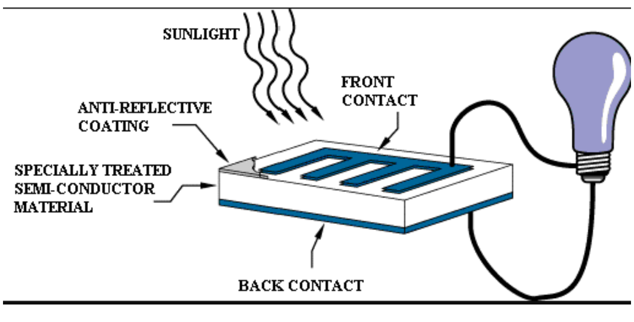


Figure C.1: IV curve of a solar cell showing the open-circuit voltage [1]

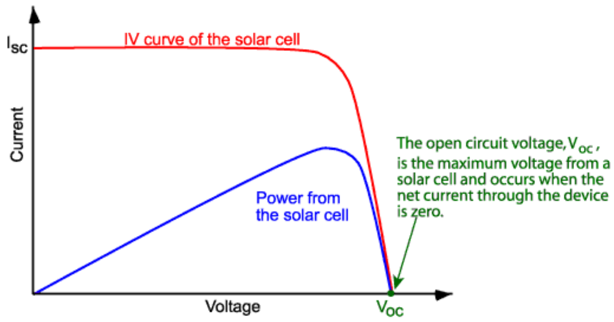


Figure C.2: Terminal voltage of a 537-5422 battery discharded at different currents [2]

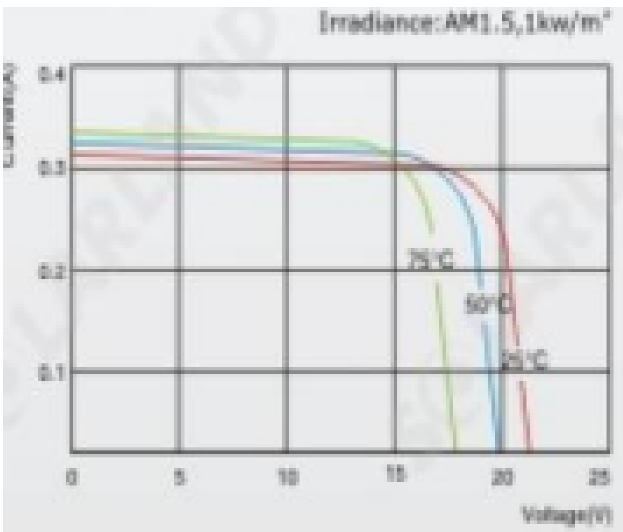


Figure C.3: Temperature effect on IV curve [3]