Układy Cyfrowe i Systemy Wbudowane 1

Układy PLD

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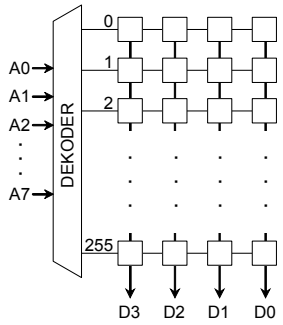
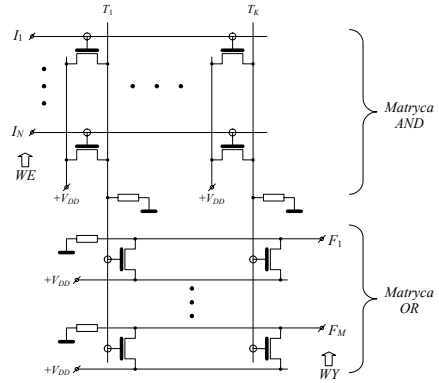
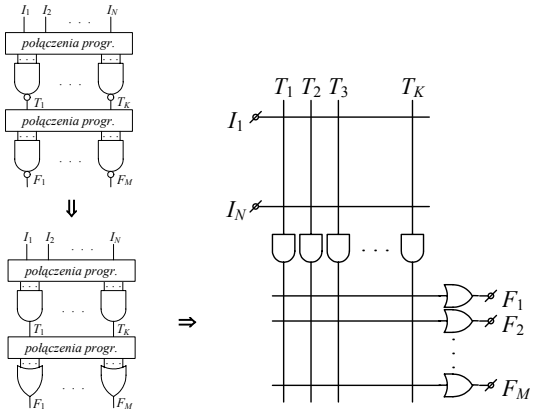
IIAR, pok. 227 C-3

PROM 256x4



Matryca PLD

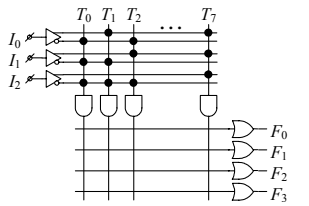


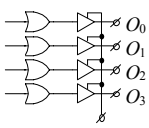


	PAL (*Programmable Array Logic*)	**PLE** (*Programmable Logic Element*)	**PLA** (*Programmable Logic Array*)
Matr. AND:	Progr.	Const.	Progr.
Matr. OR:	Const.	Progr.	Progr.

Układy PLE

Np. 8x4:

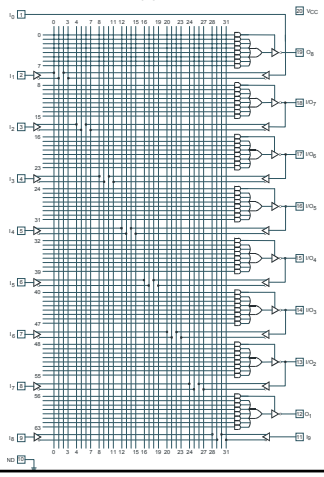


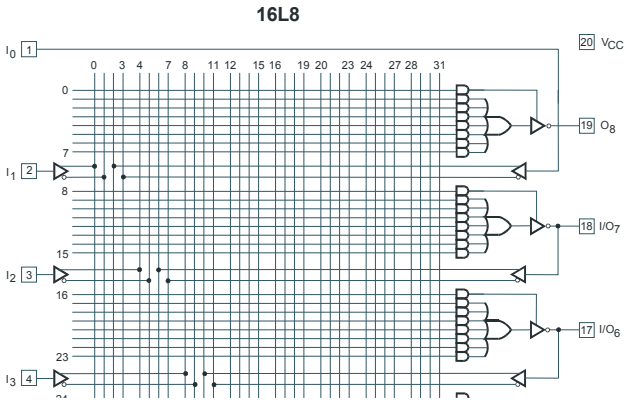


OE (*output enable*)

$OE = 1 \Rightarrow OUT = IN$ (0/1)
$OE = 0 \Rightarrow OUT = Z$ (HighZ)

PAL16L8





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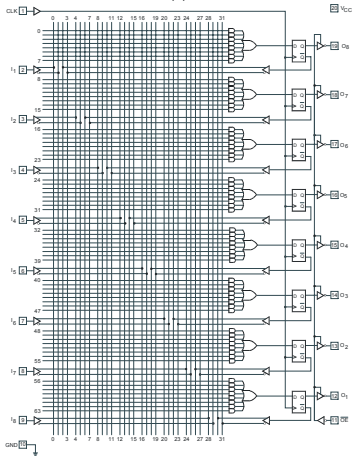
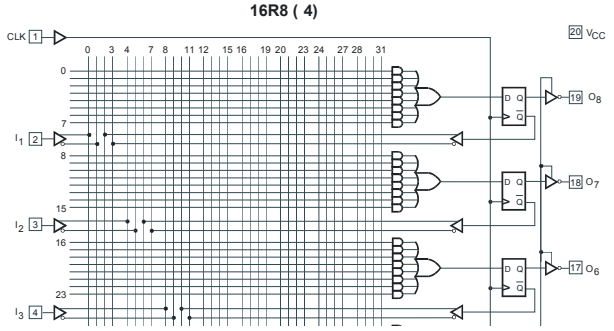
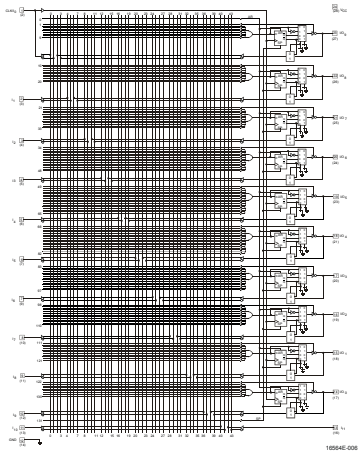
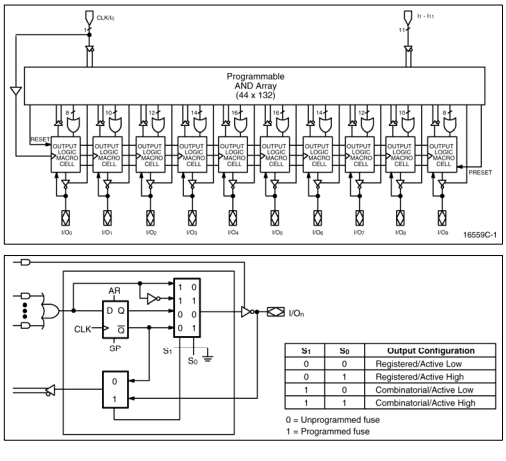




PALCE22V10





S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

Complex PLD

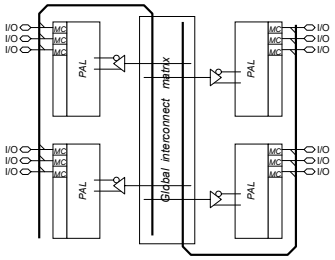
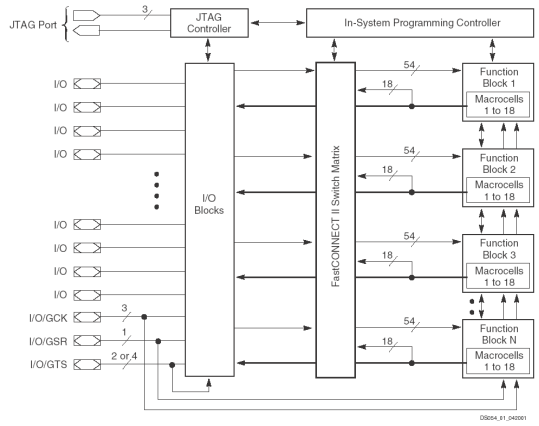


Table 1: **XC9500XL Device Family**

	XC9536XL	XC9572XL	XC95144XL	XC95288XL
Macrocells	36	72	144	288
Usable Gates	800	1,600	3,200	6,400
Registers	36	72	144	288
T_{PD} (ns)	5	5	5	6
T_{SU} (ns)	3.7	3.7	3.7	4.0
T_{CO} (ns)	3.5	3.5	3.5	3.8
f_{SYSTEM} (MHz)	178	178	178	208

Arch. XC9500XL



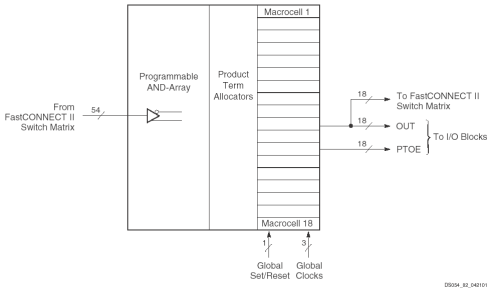


Figure 2: **XC9500XL Function Block**

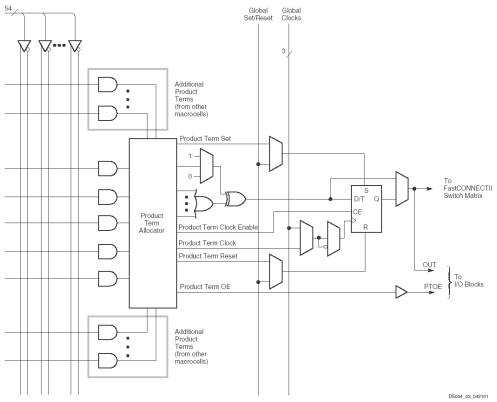


Figure 3: **XC9500XL Macrocell Within Function Block**

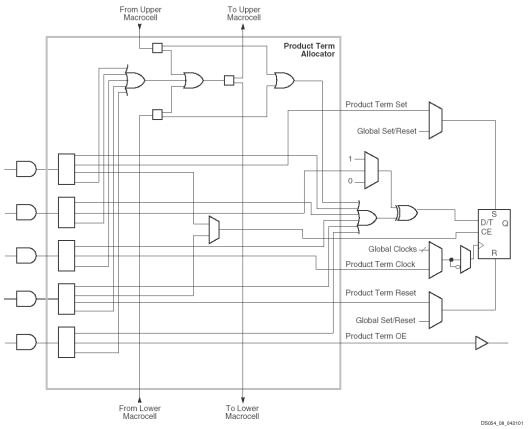
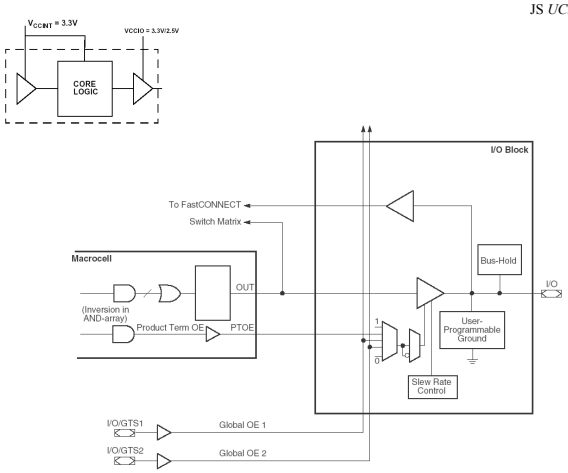
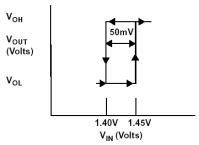
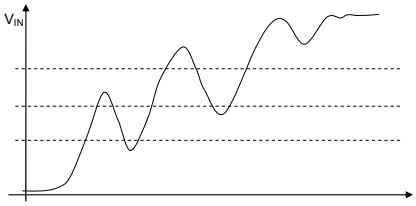
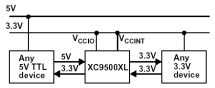


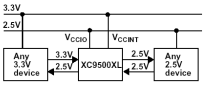
Figure 8: **Product Term Allocator Logic**

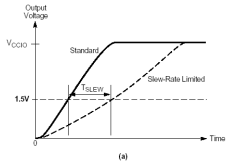


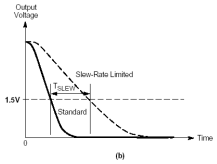












Bus-hold (pin keeper)