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E344 Assignment 5

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Nomenclature

Variables and functions

V_O	The output voltage of the TSC213.
V_{swing}	The output swing of the TSC213.
V_{ref_cs}	The reference voltage of the TSC213.
I_{range}	The current range that the TSC213 is designed for.
R_{shunt}	The resistor value that the TSC213 will measure a differential voltage across.
C	Capacitance used in lowpass circuit.
$V_{ref-Schmidt}$	The voltage used as a reference for the non inverting Schmidt trigger.
V_{SS}	Negative supply rail of the op amp.
V_{DD}	Positive supply rail of the op amp.
V_+	Positive input of the op amp.
V_-	Negative input of the op amp.
V_{TL}	The lower threshold voltage at the input to the non inverting Schmidt trigger.
V_{TU}	The upper threshold voltage at the input to the non inverting Schmidt trigger.
V_s	An intermediate voltage used in calculations to obtain V_{ref} .
V_{out}	The output voltage of the non inverting Schmidt trigger
V_{in}	The input to the non inverting Schmidt trigger
V_H	The high output voltage of the op amp.
V_L	The low output voltage of the op amp.
V_{CM}	The common mode voltage of the op amp.
V_D	The differential voltage of the op amp.
V_{adj}	Voltage at the Adjust terminal of the regulator
I_{adj}	Current flowing into adjust terminal
V_{O-reg}	Voltage at the Output terminal of the regulator
V_i	Voltage at the input terminal of the regulator
V_{bat}	Voltage at the positive battery terminal
$V_{ref-reg}$	The voltage between the adjust and output terminals of the regulator

θ_{j-c}	Thermal resistance from LM317 junction to its case
θ_{s-a}	Thermal resistance from the heat sink to ambient
θ_{j-a}	Thermal resistance from LM317 junction to ambient
$V_{schottky}$	Forward bias Voltage of the schottky diode
T_j	The junction temperature of the LM317 regulator

Acronyms and abbreviations

A	Ampere
μ	micro-
m	mini-
k	kilo-
V	Volts.
NMOS	N-channel metal-oxide semiconductor.
PMOS	P-channel metal-oxide semiconductor.
op amp	Operational Amplifier.
LED	Light emitting diode.
Ω	Ohms- a measure of resistance.
Hz	Hertz- a measure of frequency.
F	Farad- a measurement of Capacitance.
Ah	Ampere Hours.
CA	Cranking Amps.
W	Watts
$^{\circ}\text{C}$	degrees Celcius.
ADC	Analog to Digital Converter.
LDR	Light Dependant Resistor

Chapter 1

Literature

1.1. Solar Voltaic Cells

A solar voltaic cell is able to convert solar energy into electrical energy by means of the photo voltaic effect. The photo voltaic effect occurs when a N-type and P-Type material are connected .This means that light generated carriers are swept across a p-n barrier, electrons move to the n-side and holes move to the p-side. The barrier prevents the holes and electrons from returning to their original locations and this causes a net electric charge [8].

The open circuit voltage of a solar cell is the maximum voltage when no current is flowing [9]. The solar module in question has a rated open circuit voltage of 22.31V. This solar module has 36 cells in series which means the voltage of each cell sums up to 22.31V. This implies that each solar cell at its maximum will have a voltage of $\frac{22.32}{36} = 0.62V$. The open circuit voltage in general is dependant on factors such as temperature. An increase in temperature will lead to a lower V_{OC} [9].

Short circuit current is when the terminals of the solar cell/module is shorted and the voltage across the terminals is 0V. The short circuit current is dependant on the spectrum of the light shining on the PV module, something called the collection probability, the optical properties (absorption and reflection) and the number of photons that the panel is exposed to which can be split into the area of the cell/module and the intensity of the light. The collection probability of the solar cell is dependant on the minority carrier lifetime . This means the average time it takes for the excess minority carrier to recombine [10].

From figure 1.1 it can be seen that there are two points at which the lines have definite changes.The "knee" of the I-V curve and the "elbow" of the PV curve.

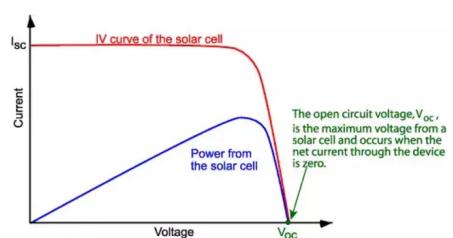


Figure 1.1: Maximum power point tracking [1]

The voltage at which the peak of the PV curve occurs is the voltage at which the maximum power is achieved. When external factors change such as temperature, light intensity and spectrum of the light, it causes the I-V and P-V curves to change [11]. Under standard conditions the MPP of the solar panel in question occurs at 18.21V and 0.28A. To calculate the efficiency of the solar panel you take the radiance of the light shining on the module and multiply it by the area of

the module. This is the ideal maximum power for that light. To get efficiency divide the previous answer by the power output. In general solar panels have an efficiency of 20% [12].

The Standard Test conditions used to test the SLP005-12 solar panel is a light that emits 1000W per square meter and the light used had an AM of 1.5. The tests were completed at 25°C. The Standard Testing conditions are parameter that all solar panel producers use to define the performance of their solar equipment.

Table 1.1: Solar Panel Measurements

	$V_{O.C}$ [V]	$I_{S.C}$ [mA]	V_{pmax} [V]
Theroretical per cell	0.6	340	0.472
Datasheet per module	21.6	340	17
Measured dark	1.1	0	
Measured upside-down 19.19	7.8	1.0	
Measured oblique	19.7	33	
Measured facing	22.66	178.3	

1.2. Lead Acid Battery

The battery capacity of a Lead acid battery can not be used from 100% to 0% but instead the battery data sheet discharges to a minimum of 1.8V per cell (5.4V). The battery in our use case is rated for 4.0Ah@20hr-rate to 1.80V which means that it was able to discharge for 20hr with a load of 0.2A until the voltage of each cell reaches 1.8V. The capacity of a lead acid battery is affected by a number of external factors such as temperature. Higher temperatures will increase capacity at the cost of accelerating ageing of the battery and lower temperatures will decrease the battery capacity [8].

Batteries also have an internal resistance, in our case $45\text{m}\Omega$. This internal resistance will have the effect of heating the battery up. The internal resistance of the battery increases with lower temperatures and decreases with higher temperatures[2]. The battery used in E344 has a self discharge of 3% per month at room temperature. The internal resistance can also cause a voltage drop [13] at the terminals when the battery is connected to a load, this can be seen in figure 1.3.



Figure 1.2: Charging states of lead acid battery [2]

Battery charging tends to take on three different stages, these three stages can be referred to as bulk, absorption and float [14]. In the bulk charging stage the current is held at a constant amount and the voltage increases. For our battery this means 0.2-0.3C until the voltage reaches 6.75V [2]. The bulk stage includes the highest charging rate. During the absorption stage the voltage remains constant and the current decreases which leads to a decreasing charge rate. For our battery this means 0.1C until the voltage reaches 7.2V [2]. At the end of the absorption stage the battery is at

100% capacity. The next stage of charging is float charging where the voltage is decreased slightly (in our case to 6.75 - 6.9) and the current is at approximately 1% of the battery capacity, this charging state is used to keep the battery charged indefinitely [14]. All these different states can be seen in figure 1.2

The C rating is a measurement of the rate at which a battery will discharge relative to

its maximum capacity [15].

As the C rating decreases the run time does not increase linearly (refer to figure 1.3), the reason for this is because a higher discharge rate causes the battery to lose energy to heat as more current flows through the internal resistance [16]. At higher discharge rates the terminal voltage is lower due to the internal resistance causes a voltage drop.

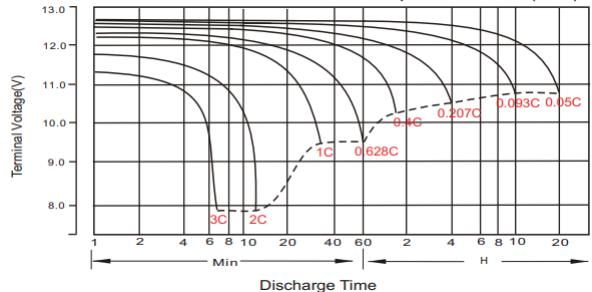


Figure 1.3: Discharge Characteristics

Discharge Characteristics [3]

1.3. Fuse Characteristics

In this section, the different characteristics of the blade fuse that is being used is discussed. A fuse has a **current rating** which refers to the nominal current that the fuse can handle although it is recommended that the current at an ambient temperature of 25°C not be higher than 75% of this value [17]. Fuses operate by blowing when current higher than the nominal rated current flow through the fuse. For this reason when the ambient temperature increases, the current required to reach a point where the fuse will melt is lower than it would be for lower ambient temperatures. This can be seen in figure 1.4a line "B". Current and time have an inverse relationship as can be seen in figure 1.4b, this means that for higher currents the fuse will blow faster.

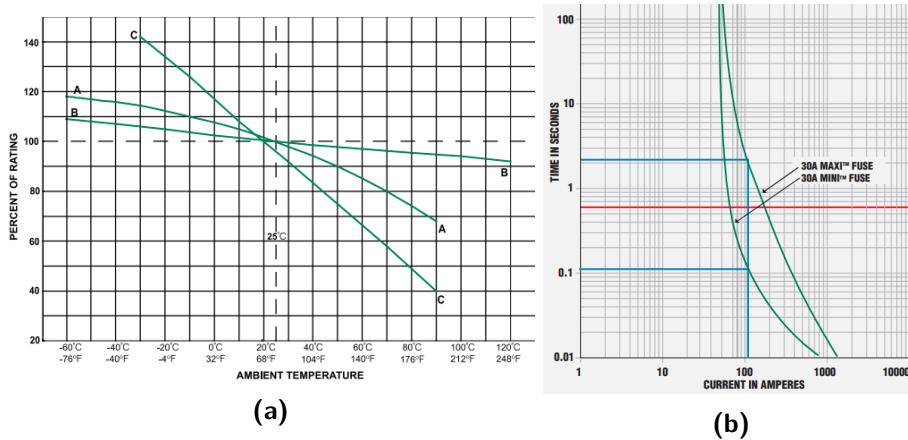


Figure 1.4: Fuse Characteristics Relating to blow time (a) Current Rating versus Ambient Temperature [17] (b) Blow time vs Current [18]

Chapter 2

System Design

2.1. Charging circuit overview

The charging circuit structure can be seen in figure 2.1 as the green highlighted blocks. The 12V supply and the solar panel will connect directly to the linear regulator. The linear regulator is the part of the system that will be tuned to achieve the adequate current limiting, voltage and thermal specifications. The charging circuit will then be intercepted by the high side switch so that the charging can be controlled by a logic high or low to the switch.

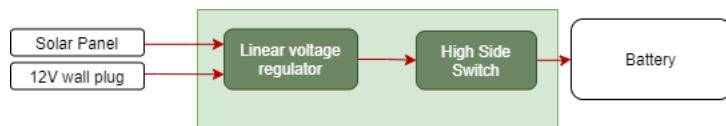


Figure 2.1: Charging System Block Diagram

2.2. Under Voltage and Over Current circuit overview

The circuit structure can be seen in figure 2.2 as the yellow highlighted blocks. The goal of this circuit is to disconnect the battery from the load when the voltage is below a certain voltage and then to reconnect the battery when the voltage is above a certain voltage. The circuit will also protect the battery from abnormally high charging currents with a fuse. The Schmidt trigger block manages the logic of whether the switch should be on or off. This decision is then conveyed to the high side switch which then implements the connection or disconnection of the battery from the load. In order for the Schmidt trigger to work it requires 5V which will be supplied through a regulator from the battery.



Figure 2.2: Under Voltage System Block Diagram

2.3. Current sense circuit overview

The current sense circuit structure can be seen in figure 2.3 as the purple highlighted blocks. The current sense circuit connects the two previous system block diagrams to make up the final block diagram. The current sense circuitry was added at its position after the load so that the current it will measure is the current discharging from the battery or charging into the battery. In order to operate the current sense amplifier will require a 5V from the 5V regulator. The current sense amplifier will be used to produce voltage between 0V and 5V that will correspond proportionally to the current in a designed range of 3V. The current sense amplifier will amplify very small voltages across the current sense resistor. The load can also be connected and disconnected with the help of the designed low side switch. The output of the current sense amplifier will be prone to noise from the 12V wall plug as well as the 5V regulator. In order to fix this a output filter will be required at the output of the current sense amplifier. The directions of the arrows in the block diagrams show the direction that current flow will be enforced. This means schottky diodes will be used at the solar panel the 12V wall plug as well as the output of the charging circuit.



Figure 2.3: Complete System Block Diagram

2.4. Battery and Supply voltage measurement

Chapter 3

Design Details

3.1. LM317 Regulation

The voltage regulation as well as the current limiting feature can be achieved with the LM317 regulator with the use of an application circuit. The LM317 is a linear regulator which means that it uses linear components such as resistors to achieve required variations, thus it is constantly dissipating power. A switching regulator makes use of PWM to get the required variation. Because PWM means it turns on and off it dissipates less power than a linear regulation [19]. Figure B.2 is the application circuit that will be used in the design process to achieve the constant voltage and current limiting specifications. The resistor values will be redesigned. The regulator works on the basis that the difference between the output terminals and adjust terminals is a "fixed" voltage. The current flowing into I_{adj} is typically $50\mu\text{A}$ but can be a maximum of $100 \mu\text{A}$ [4]. The following equation 3.1 is obtained from the data sheet [4] and correspond to figure B.2.

$$V_{O-reg} = V_{ref-reg} \times \left(1 + \frac{R_2}{R_1}\right) + (I_{adj}) \times (R_2) \quad (3.1)$$

$$V_{O-reg} - V_{adj} = 1.25V \quad (3.2)$$

3.1.1. Voltage regulation

A voltage of 7.2V is designed for using equation 3.1. This voltage is slight lower than the 7.35V (2.45×3) specified in the data sheet. It can be considered a safety factor.

$$\frac{R_2}{R_1} = \frac{7.2}{1.25} - 1 = 4.76$$

The resistor values used should be kept low so that the current flowing through R_1 and R_2 is significantly larger than I_{adj} . If this is done then I_{adj} can be neglected. R_2 is chosen to be 1000Ω . Therefore R_1 will be 210Ω . Refer to figure B.2.

$$\frac{7.2}{R_1+R_2} = 6mA >> 100\mu\text{A}$$

Because 5mA is 50 times larger than the maximum, the I_{adj} can be assumed to be negligible as it will have minimal effect on the calculations.

3.1.2. Current limit

The current limiting was implemented by calculating a value for R_4 (refer to 3.2). The maximum current that was designed for was 400mA. This value was chosen because the battery data sheet recommends 0.1C for charging which equates to 400mA [2]. This current will be designed flow when the battery is at its depleted voltage of 6V. To determine R_s V_O must be calculated when $V_{bat}=6V$. Using the calculated V_0 the resistor R_s is designed for the desired current.

$$V_{schottky} = 0.4V$$

$$V_{adj} = (6 + V_{schottky}) - \frac{(6+V_{schottky}) \times R_1}{R_1 + R_2} = 5.29V$$

$$V_{O-reg} = 1.25 + V_{adj} = 6.539V \text{ (refer to equation 3.2)}$$

$$R_s = \frac{V_{O-reg} - (V_{bat} + V_{schottky})}{400mA} = \frac{6.539V - 6.4V}{300mA} = 0.347\Omega$$

The biggest flaw with this method is that $V_{schottky}$ voltage is not accurate. Another problem will be that achieving a resistance of 0.347Ω will be very inaccurate.

3.1.3. Thermal analysis

As the junction temperature increases the output current will decrease for the same $V_i - V_{O-reg}$ [4] (refer to 3.1). All thermal resistance values used can be found at B.1.

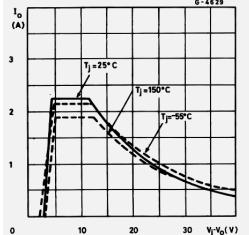


Figure 3.1: Output current vs. input-output differential voltage for different junction temperatures [4]

$$T_j - T_a = P_{tot} \times (\theta_{j-a}) \quad (3.3)$$

$$T_j - T_a = P_{tot} \times (\theta_{j-s} + \theta_{s-a}) \quad (3.4)$$

The most power our regulator will dissipate is:

$$0.3A \times (12V - 6.539V) = 1.64W$$

Without a heat sink, at an ambient temperature of $25^\circ C$ the junction temperature will be(refer to eq. 3.3):

$$T_j = 1.64W \times (50^\circ C/W) + 25^\circ C = 107^\circ C.$$

With the heat sink, at an ambient temperature of $25^\circ C$ the junction(refer to eq. 3.4):

$$T_j = 1.64W \times ((5 + 20)^\circ C/W) + 25^\circ C = 66^\circ.$$

We want out current to be predictable and close to the value calculated, the heat sink enables the calculation to be more accurate. The maximum operating temperature of the regulator is $125^\circ C$ [4]. $107^\circ C$ is quite close and I would definitely recommend that the heat sink is used. For a higher input voltage the regulator could break without a heat sink.

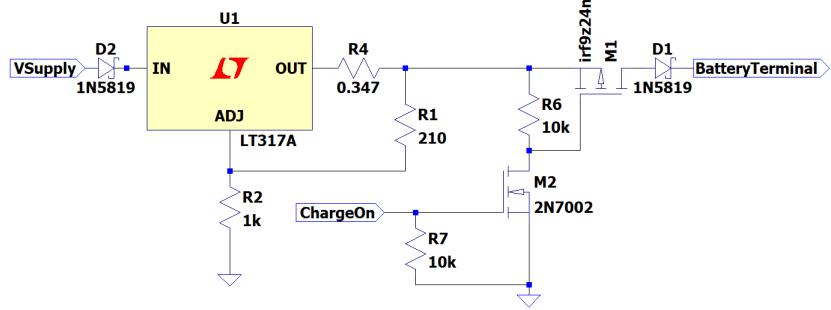


Figure 3.2: Charging Circuit with high side switch implemented

3.2. High side switch on supply side

Switches are often used to control the flow of current within a circuit. In this report only enhancement mode MOSFETs will be used. The MOSFETs we are using have 3 terminals, gate, source and drain as can be seen in figure 3.3.

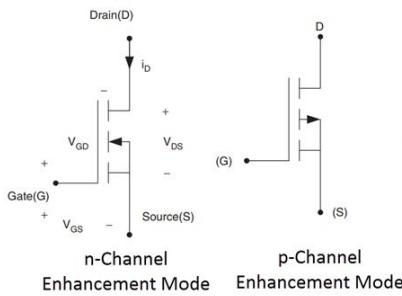


Figure 3.3: The different MOSFET configurations

For a NMOS chip the current will flow from the drain to source when it is in its **ON** state whereas for a PMOS the drain current will flow from the source to the drain. For the NMOS to turn on a positive voltage across the gate and the source must be applied that is larger than a certain threshold (refer to figure 3.4b). For a PMOS the same is true however the voltage is instead negative (refer to figure 3.4a).

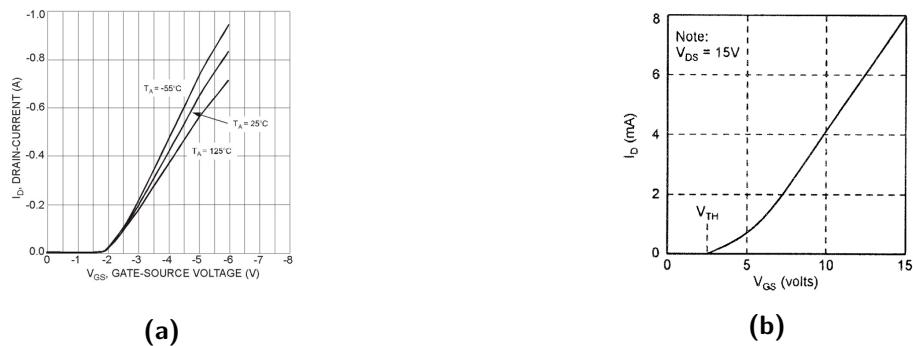


Figure 3.4: Turn on voltages for NMOS and PMOS (a) PMOS [20](b) NMOS [21]

When designing the switch the considerations taken into account was the fact that the PMOS can handle in excess of amps [20] whereas the NMOS can only handle 200mA [22]. For this reason the NMOS is used to switch the PMOS on. The way that this is achieved is by turning the NMOS on with a logic high of 5V, when the NMOS is on current flows through R_1 and R_2 (refer to figure 3.5) and this causes there to be a voltage over the source and gate of the PMOS. This voltage needs to be greater than 4V and less than 20V in order for the

PMOS to turn on and function without breaking [20].The NMOS has a maximum threshold voltage of 3V. The 5V will be enough to turn it on [21]. A resistor is also placed between the gate of the NMOS and ground to prevent the gate from floating.

- To prevent current from the load from flowing back into the supply a schottky diode is placed in series with the load.
- To ensure that all the 25V is not across the PMOS V_{SGp} terminals the voltage is divided using R_1 and R_2 (refer to figure 3.5).
- The magnitudes of the resistors used were decided mainly to restrict excessive current flow through the resistors, $\frac{5}{10k} = 0.5\text{mA}$ or $\frac{25}{20k} = 1.25\text{mA}$ which is relatively small.

$$I_{Dn} = \frac{R_1 + R_2}{V_{supply} - V_{DSn}} \quad (3.5)$$

$$V_{SGp} = V_{R1} = I_{Dn} * R_1 \quad (3.6)$$

$R_1 = 10k\Omega$ $R_2 = 10k\Omega$ $V_{supply} = 25V$. If $V_{DSn} \approx 0$ for $V_{GSn} = 5V$ then using eq.3.5 $I_{Dn} = 1.25\text{mA}$.Using eq.3.6 $V_{SGp} = 12.5V$, this is larger than 4V and smaller than 20V and will "turn on" the PMOS transistor without damaging it.

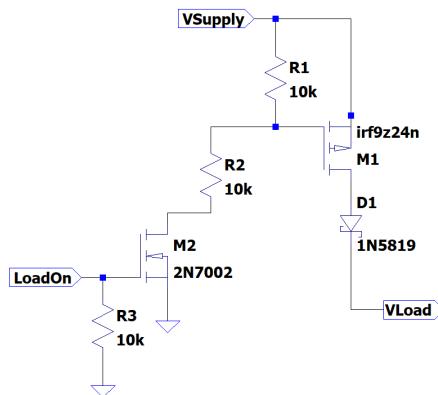


Figure 3.5: High side switch circuit

3.3. Over current protection

From the battery's perspective, it will be able to discharge 60A for 5 seconds as an absolute maximum [2]. The battery also has a maximum recommended charging limit of 1.2A [2]. We will not be charging at 1.2A, we will be charging at approximately 400mA (I chose 300mA refer to 3.1).

The load we are going to use will be made up of 5 ultra bright LEDs. The peak forward current of one of these LEDs is 100mA [23]. This means that for the peak case, just the load will use 500mA of current, however we will be designing for the typical 20mA per LED with current limiting resistors (refer to section 3.6). This is then equated to 100mA for the entire load.

From the previously mentioned information we have 4 different current limit values. Two of these values are limits regarding the battery's limits and 2 are limits regarding what the circuit should charge/discharge. The fuse will be connected between the battery and the complete circuit, all current charging/discharging from the battery will flow through the designed fuse.

The battery's limits are well above what the circuit will require, therefore the upper limit of the circuit charging will be used as the reference for the design. I then doubled the 400mA charging current to set the fuse for an abnormal condition. If 800mA of current flow then something is not working correctly and the battery should stop discharging. The closest fuse we have to this is 1A.

3.4. Undervoltage protection

In the design below the concepts of a op amp voltage comparator is used. A comparator will amplify the difference of the two terminals. A problem with the standard comparator op-amp

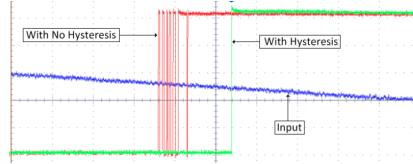


Figure 3.6: Op-Amp with hysteresis implemented compared with no hysteresis [5]

configuration is that if a noisy signal is placed at the input of the op-amp it could cause the op amp output to switch between the two supply rails in a short period of time leading to a signal as can be seen in figure 3.6. A op amp with hysteresis means that the op amp has positive feedback from the output and this causes the output of the op amp to switch from rail to rail at two voltages V_{TU} and V_{TL} , refer to 3.7.

3.4.1. 5V rail

In the circuit that was used in the final design an LM2940 regulator was chosen over a LM7805 regulator because of the respective drop out voltages of 0.5V [25] and 2V [26]. This is important because the voltage input to the regulator can be as low as 6V (battery terminal) and that would mean that the LM7805 would have a regulated voltage of below 5V. The LM7805 is able to output a maximum recommended amperage of 1.5A whereas the LM2904 only has a recommended output current of 1A [25] [26]. The LM2940 does have a typical quiescent current of 10mA which is ideal as we are designing for this current or less than 10mA [25].

3.4.2. High-side switch

The fundamental design is the same as in section 3.2, the only difference is the lack of R_2 and the schottky diode. R_2 is not need to decrease the voltage V_{GS} at the PMOS and no current flow restrictions are needed from the schottky diode. The high side switch is used at the position specified in figure 2.2, it must be able to control the discharge of the battery but not restrict charging from the charging circuit. To ensure that this would not be an issue the reverse current of the PMOS was found in the respective data sheet to be -12A [20].

3.4.3. Voltage monitoring with hysteresis design

The positive supply rail of the op amps in this design will be connected to the 5V regulator and the negative supply rails will be grounded(V_{DD} and V_{SS}). When designing the input voltages to the op amp it was decided to step the voltages down using voltage division because

if the battery terminal (max of 7.2V) is connected and a 0V is connected then the differential voltage maximum will be exceeded. The circuit that was built was based off the non inverting Schmidt trigger as can be seen in figure 3.7 [6].

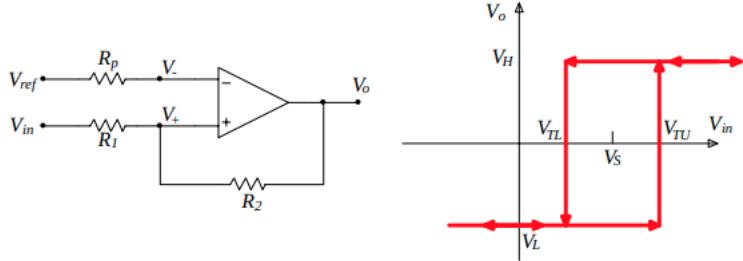


Figure 3.7: Non inverting Schmidt trigger [6]

This configuration compares an input voltage with a constant reference voltage and the output will switch to the positive supply rail at an input voltage of V_{TU} and to the negative supply rail at V_{TL} (refer to 3.7). A divided voltage from the 5V regulator is used as a reference voltage because it will remain "constant". The suitable $V_{ref-Schmidt}$ is calculated below and $V_{ref-Schmidt}$ is connected to a voltage follower op amp to prevent the positive feedback from affecting the input voltage. The battery voltage is divided to be 4.5V ($\frac{7.2 \times 100}{100+60} = 4.5\text{V}$) at the op amp terminal using R_7, R_{10} and R_8 (refer to figure 3.8). With a battery terminal voltage of 6.2V the voltage at the op amp will be $V_{TU} = 3.875\text{V}$ and with 6V the voltage will be $V_{TL} = 3.75\text{V}$. V_L (approx zero volts) is the low output of the Schmidt trigger and V_H is the high output of the Schmidt trigger (approx 5V). Equations below are for a non-inverting Schmidt trigger. **The equations are derived extensively in Appendix C.**

$$\frac{V_{TU}-V_{TL}}{(V_H-V_L)} = \frac{R_1}{R_2}$$

$$V_{REF} = \frac{V_{TL} \times (R_2)}{R_1 + R_2} + \frac{V_H \times R_1}{R_1 + R_2}$$

Using the above equations the $\frac{R_1}{R_2}$ ratio is found to be $\frac{1}{40}$. R_2 is chosen to be $190\text{k}\Omega$ which results in $R_1 = 4.75\text{k}\Omega$. The closest lab resistor is $4.7\text{k}\Omega$. With our resistor values now defined V_{REF} can be calculated to be 3.78V. The relevant voltage division can be found in figure 3.8

Table 3.1: Undervoltage circuit op amp requirements [27]

	Min [V]	Max [V]	Designed [V]
All op amps Difference between supply rails $V_{DD} - V_{SS}$	-	7	5
U2 Common mode voltage $(\frac{V_++V_-}{2} - V_{SS})$	-0.3	5.3	3.75-4.5
U2 Input voltages to V_- and V_+	-1	6	3.75-4.5
U3 Common mode voltage $(\frac{V_++V_-}{2} - V_{SS})$	-0.3	5.3	3.72-4.12
U3 Input voltages to V_- and V_+	-1	6	0-4.51
U3 Differential Voltage ($ V_+ - V_- $)	-	7	4.51

From table 3.1, all op amps are operating within working ranges.

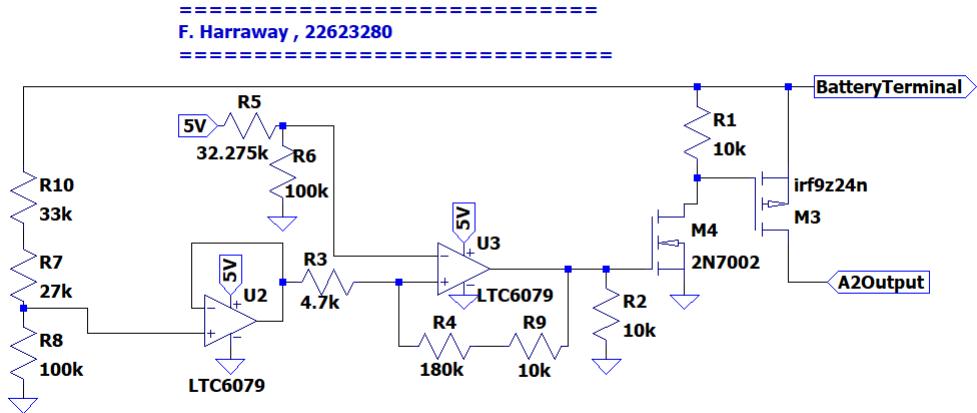


Figure 3.8: Circuit diagram of under voltage circuit connected to the high side switch and the output of the previous assignment as well as the battery terminal

3.5. Current sense

The bidirectional current sense amplifier is an op amp that is setup internally as can be seen in figure B.1. This internal circuitry is necessary because the resistors used need to be very accurate in order for current sensing to be accurate [28]. Another reason that the tsc213 is being used over a conventional op amp is because this device has a absolute differential voltage of 26V and a common mode voltage range of $gnd - 0.3V$ to 26V. This is important for us because we can have differential voltages of up to 7.2V ($7.2 - 0$) and common mode voltages of about 7.2V which would not work with the previously used MCP op amp. We do not want to step down the voltages as we did previously because it would not be accurate for the current measurements. The current sense amplifier will have its positive and negative inputs connected across a shunt resistor, the current sense amplifier will then amplify this difference by 50 (refer to B.1).

When designing the current sense amplifier the current range that will be used should be considered. The most current that should be discharged from the battery should be 100mA. The maximum that the battery should charge at is 400mA. The current range was then determined to be $-150mA < I_{range} < 450mA$, the additional 50mA was added as a safety factor to ensure the tsc213 does not breach the 0-5V output range. We do not want to breach this range because it could damage the micro controller to which the output of the tsc213 will be connected. The output voltage range will be dependant on the differential voltage of the op amp and the reference voltage chosen (refer to eq 3.7). The differential voltage will be dependant on the shunt resistance and the current through the shunt. The final circuit structure can be seen in figure 3.9b.

$$V_o = (R_{shunt} \times I_{shunt}) \times 50 + V_{ref_cs} \quad (3.7)$$

Using eq.3.7 R_{shunt} is designed to give an output voltage swing of 3V for the current sense

amplifier.

$$V_{swing} = ((R_{shunt} \times 0.45) - (R_{shunt} \times -0.15)) \times 50. \quad R_{shunt} = 0.1\Omega$$

This results in voltage range across the shunt of $-15mV < V_{shunt} < 45mV$. With a 0V at V_{ref_cs} the output range (using eq.3.7) would be -0.75V to 2.25V. This is not within 0V to 5V, this is where V_{ref_cs} is used to place the output voltage into a desirable range. The minimum V_{ref_cs} to get the output into the desired range would be 0.75V. The maximum V_{ref_cs} that would place the maximum output voltage at 5V would be 2.75V (i.e. 5-2.25). The average of the maximum and minimum V_{ref_cs} is then taken and found to be 1.75V. By doing this output voltage will be equally far from the upper and lower bounds of the 0V to 5V specification. To achieve this 1.75V the voltage from a 5V regulator is divided with resistors (refer to figure 3.9a).

To reduce the noise at the output a passive filter was designed and placed at the output of the TSC213. This can be seen in figure 3.9a. The larger this capacitor the slower the response of the TSC213 output will be. If the value is too small then the output noise will not be sufficiently reduced. The passive filtering is needed because the 5V regulator as well as the 12V wall supply introduces a lot of noise into the system.

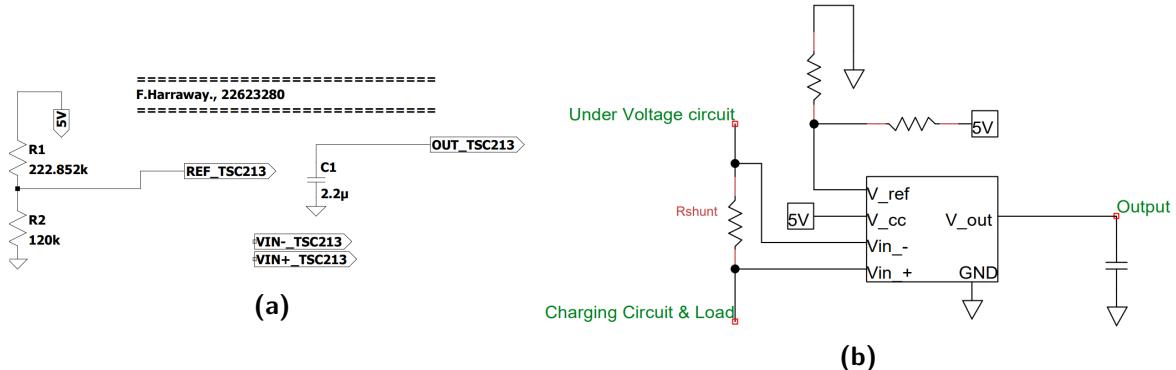


Figure 3.9: Current sense circuitry (a) LT Spice current sense circuit (b) Current sense circuit

3.6. Low Side Switch and Load

In this design notable factors that will affect the design will be outlined. The load that will be used is made up of 5 LEDs that will be designed in such a way so that together 100mA is drawn. The NMOS we are going to use is able to sink a maximum continuous drain current of 200mA [22]. A low side switch means that the "switching element" is place in between ground and the load. This can be seen in figure 3.10.

Because 100mA is the maximum current a 2n7000 NMOS chip was deemed enough to be used as a switch for the load. To "turn on" the NMOS a 5V control signal will be used. To ensure that the gate of the NMOS can not float a pull down resistor will be used. For a drain current of 100mA, according to the data sheet the V_{DSon} voltage will be approximately 0.2V for a V_{gs} of 5V [22]. The LED we are using has a typical forward bias voltage of 3.2V at 20mA [23]. To limit the current to 20mA ($7.2V - 20mA * R_{limit} = 3.2V + 0.2V$) a resistor of 190Ω would be ideal ,but only 220Ω 's are available in the labs. The LEDs will be in series with the current limiting resistor. The LED-resistor units will then be placed in parallel to each other (refer to figure 3.10).

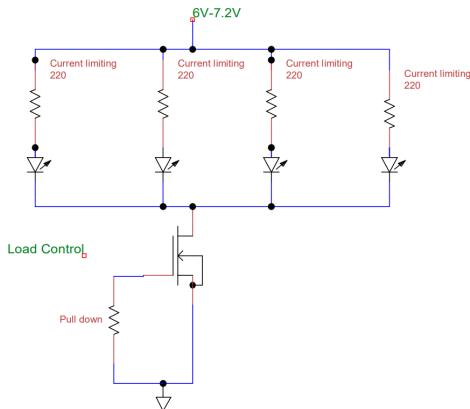


Figure 3.10: Load circuitry with low side switch implemented

3.7. Supply voltage measurement

The Supply voltage of supply will vary from voltages of zero volt to just below 23V. To measure the supply measurement needs to converted to a voltage between zero and five volts in order for the arduino beetle to successfully read a voltage without breaking. There should be a boundary between 5V and the maximum converted voltage. To implement this a maximum voltage of 24V is designed for instead of 23V. One of the two possible supplies, the AC wall plug will introduce noise into the circuit (50Hz from the mains). This noise will likely be 50Hz which will be designed for adequately using a low pass RC filter.

$$\frac{R_{10}}{R_{10}+R_9} \times 24V = 5V$$

If R_9 is chosen to be $100k\Omega$ R_{10} will be $26.3k\Omega$.

$$f_c = \frac{1}{2 \times \pi \times R \times C} \quad (3.8)$$

To prevent the noise of the ac wall plug from interfering with the measurement the low pass cut off filter is designed to cut off at half of 50Hz to ensure a cleaner signal. The capacitor is chosen to be $200nF$. Cutting off at a lower frequency would get rid of more noise and attenuate 50Hz noise better, however the rise time is dependant on the cut off frequency. $T_r \approx \frac{0.35}{f_c}$. For this reason the cut off frequency is not designed too low. As an example the error that a $100mV$ offset on the input to the ADC will have is calculated as $\frac{100mV \times 26}{126} = V_{error}$, V_{error} is then equal to $0.48V$. This indicates the need for a filter.

Using eq.3.8 with a chosen capacitor of $200nF$ the required resistance for a $25Hz$ cut off is found to be $32k\Omega$.

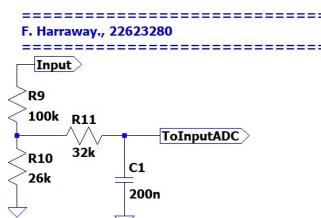


Figure 3.11: Supply measurement circuit

3.8. Battery voltage measurement

In this design the battery voltage will go through a signal conditioning process to make it readable from the perspective of an ADC. The ADC we are going to use requires a voltage between 0 and 5V. The battery voltage will vary between 6V and 7.2V if the complete system is working as designed.

For the purpose of the design an additional 0.3V will be extended on to either side of the boundaries to give a margin for error (5.7V to 7.5V). Using Op Amps the battery voltage will be designed to vary linearly with an output swing of 4.3V (0.5V to 4.8V). As the battery voltage increases the ADC voltage will increase. The ADC output is less than five volts in order to prevent damage to the ADC as well as the op amps. The chosen resistors are chosen to be bigger than $20\text{k}\Omega$ in order to minimise current drawn from the battery and the five volt regulator. To fit op amp spec requirements the input voltage is divided with resistors to be four volts at the maximum designed voltage of 7.5V as can be seen in figure 3.13, this will result in a voltage of 3.04V when the battery voltage is 5.7V.

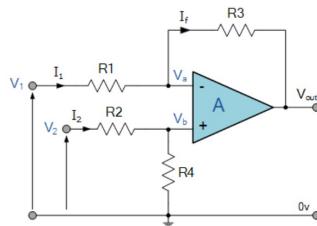


Figure 3.12: Differential amplifier op amp setup [29]

To achieve the differential amplifier setup from figure 3.12 is used. In this design $R_1=R_2$ and $R_3=R_4$ [29]. The corresponding equation is as seen in equation 3.9. V_1 will be used as the reference voltage and V_2 will be our input from the battery. **The derivation can be found in Appendix D D.2.**

$$V_{out} = \frac{R_3}{R_1} \times (V_{2(bat)} - V_{1(ref)}) \quad (3.9)$$

Using eq.3.9, $V_{1(ref)}$ and the gain is solved for simultaneously by setting the equations for the scenarios when the battery voltage is 7.5V and 5.7V.

$$4.8V = \frac{R_3}{R_1} \times (4V - V_{1(ref)}) \quad 0.5 = \frac{R_3}{R_1} \times (3.04V - V_{1(ref)})$$

$$\frac{4.8V}{(V_{1(ref)} - 4V)} = \frac{0.5V}{(V_{1(ref)} - 3.04V)} \quad V_{1(ref)} = 2.93V \quad \frac{R_3}{R_1} = 4.48$$

R_3 is then chosen to be $100\text{k}\Omega$. R_1 is calculated to be $22.32\text{k}\Omega$. Both V_1 and V_2 need to be divided to a lower voltages 2.93V and four volts (when battery is at 7.5V), the relevant resistors for the voltage division can be seen in figure 3.13. V_1 requires a buffer in between the divided battery voltage and the differential op amp to prevent the negative feedback from

interfering with the input voltage. V_2 also requires a buffer because otherwise R_2 and R_4 will change the effective voltage division and 2.93V would not be achieved.

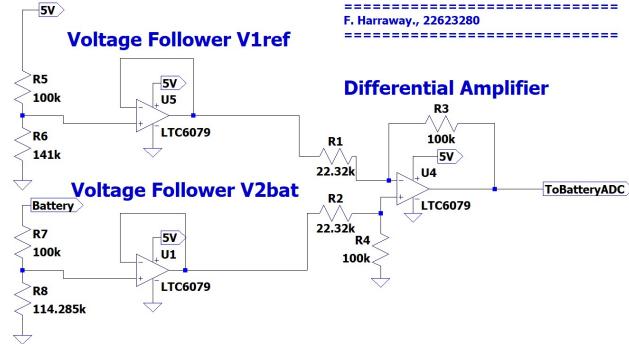


Figure 3.13: Battery measurement circuit

Table 3.2: Battery voltage measurement circuit op amp requirements [27]

	<i>Min</i> [V]	<i>Max</i> [V]	<i>Designed range/value</i> [V]
All op amps Difference between supply rails $V_{DD} - V_{SS}$	-	7	5
U1 Common mode voltage ($\frac{V_+ + V_-}{2} - V_{SS}$)	-0.3	5.3	3-4
U1 Input voltages to V_- and V_+	-1	6	3-4
U5 Common mode voltage ($\frac{V_+ + V_-}{2} - V_{SS}$)	-0.3	5.3	2.92
U5 Input voltages to V_- and V_+	-1	6	3-4
U4 Common mode voltage ($\frac{V_+ + V_-}{2} - V_{SS}$)	-0.3	5.3	2.48-3.28
U4 Input voltages to V_- and V_+	-1	6	2.48-3.28
U4 Differential Voltage ($ V_+ - V_- $)	-	5	3.28

From table F.1, all op amps are operating within working ranges.

3.9. Ambient light sensor

The LDR will be used to produce a voltage that will fall within the boundary of zero to five volts in order to work correctly with an ADC when "measuring" the light. From dark to light a resistance range of 500 Ω to over 1M Ω was measured. To get a voltage between zero and five volts, the voltage from the 5V regulator is divided as can be seen in figure 3.14. This means that unless the regulator exceeds its values the zero to five volt range of the LDR circuit will not be breached. In the labs the highest "light" measured LDR resistance is 15k Ω . When we are at this point the ADC output is designed to have a voltage of 2.5V. This 2.5V will be used in the next section. As it gets darker the resistance and voltage across the LDR will increase.

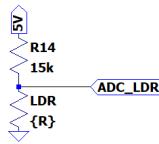


Figure 3.14: Light measuring circuit

3.10. Load and pilot LED control

The following design will achieve the output of the Load LED and pilot LED that can be seen in table 3.3. This consists of defining a "dark" and "light" point for the LDR in the previous section. This is implemented with non inverting Schmidt trigger. The hysteresis band is designed to be 0.2V around the centre voltage of 2.5V ($V_{TU}=2.6V$, $V_{TL}=2.4V$). When it is dark enough the voltage across the LDR will be greater than 2.6V and the trigger will output five volts. **The following equations are derived in Appendix C.**

$$\frac{V_{TU}-V_{TL}}{(V_H-V_L)} = \frac{R_1}{R_2}$$

$$V_{REF} = \frac{V_{TL} \times (R_2)}{R_1 + R_2} + \frac{V_H \times R_1}{R_1 + R_2}$$

Using the above equations for $V_H = 5$ and $V_L = 0$, $\frac{R_1}{R_2} = \frac{1}{25}$. With R_2 chosen as 12k Ω (R_1 in figure 3.15) R_1 will be 300k Ω ($R_2 + R_8$ in figure 3.15). V_{REF} is then calculated to be 2.5V (5V voltage divided with R_3 and R_4 in figure 3.15). A voltage following op amp is connected between the LDR circuit and the hysteresis to prevent the positive feedback from changing the actual input voltage.

To achieve the one **on** condition for the load LED in table 3.3 the **light condition** is sent to an NMOS gate that is in series with the lowside switch from section 3.6. This then requires the "light condition" **and** "load control" to be high for current to flow through the load. The same concept is applied for the PWM signal. This can be seen in the load control part of figure 3.15. A momentary switch is implemented by using a op amp sr-latch [?]. The output of the SR latch is connected to the same output as the load control from section 3.6. Diodes

are connected between the two signals to prevent interference with the sr-latch. This enables either the momentary switch or the beetle load control to enable the load control Mosfet, but current will only flow through the load if **light condition** and PWM are also high.

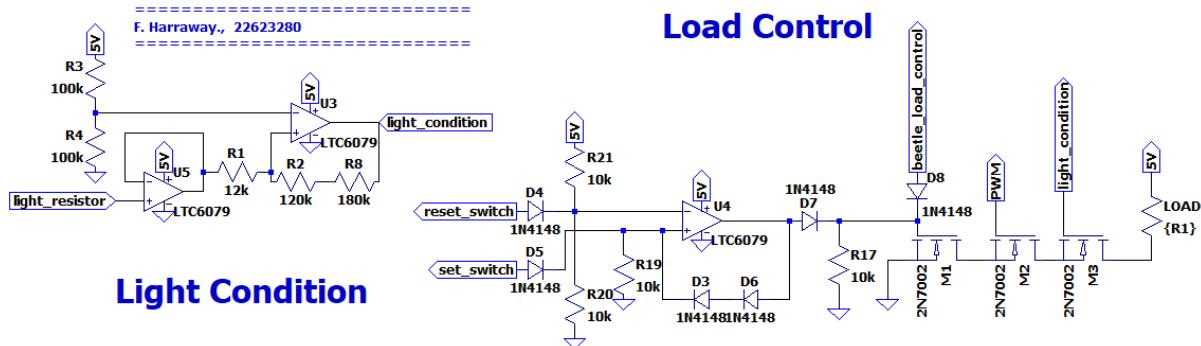


Figure 3.15: Light condition and Load Control circuit

Table 3.3: Truth table of pilot & load control

PWM [0-off/1-on]	beetle load Control [0-off/1-on]	LightCondition [0-Light/1-Dark]	LoadLED [0-off/1-on]	PilotLED [0-off/1-on]
1	0	0	0	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

3.10.1. Pilot light control design

This circuit will drive a current limited red LED with an op amp in the case that the beetle load control is high and there is a "dark" light condition. This is achieved by using a op amp as a comparator. A Schmidt trigger is unnecessary because there will be fixed logic levels.

V_- of U1 is designed to be 0.4V when the beetle load control is off, and 3.5V when the beetle load control is on (refer to appendix E). With this configuration making use of the equation $V_O = A_{OL}(V_+ - V_-)$, when the load control is on $V_+ - V_- = (2.5 - 3.5)$ and therefore the output is 0. When the load control is off $V_+ - V_- = (2.5 - 0.4)$ and therefore the output is 5V. When nothing is on $V_+ - V_- = (0 - 0.4)$ and this results in an output of 0V.

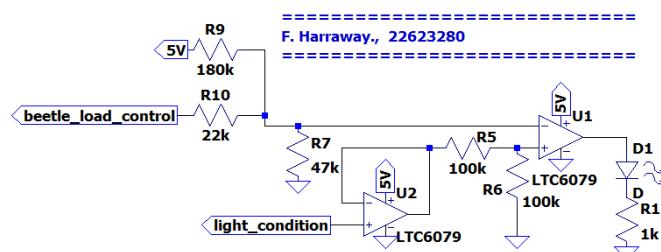


Figure 3.16: Pilot LED circuit

All op amp differential and common mode voltage are tabulated in appendix F

3.11. Firmware

3.11.1. Code flow

In arduino's "version" of C there are two main structural components to the code. The void setup and the void loop. In the setup the necessary initialisations are done such as the setup of the serial communication and required output pins. The loop runs over and over again as the name implies. The implemented code inside this loop includes Reading in ADC analogue values and then converting & calibrating those values to their practical values. After this step the necessary steps are taken to read in strings from the serial input. When reading strings from serial each character is received individually. A while loop is used to append each character to a single string. Depending on the received string the over charge control will be changed. All calibrated values and the status of the charging is then printed to serial, then there is a second delay after which the loop is repeated again.

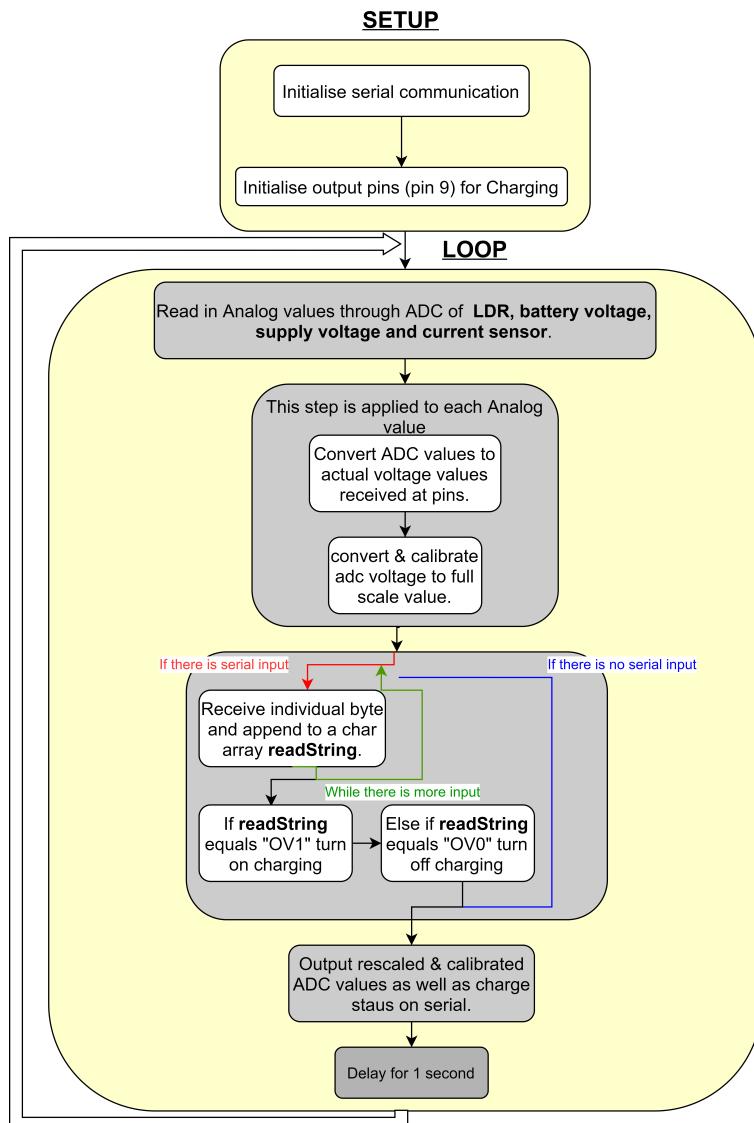


Figure 3.17: Firmware flow diagram

3.11.2. Calibration of ADC

Using $V_{in} = \left(\frac{5V \times ADC_{val}}{1023}\right)$ the ADC values are converted to the input voltages at the ADC. Then this value is used uniquely for each adc measurement to get the representative value. All the methods of calibration are linearly done.

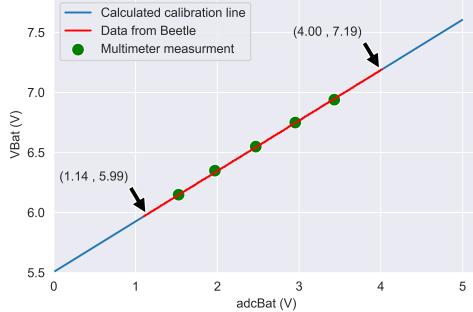


Figure 3.18: Battery ADC calibration

Using the below equation the ADC is calibrated to be the same as the measured values. $V_{adcHMeas}$ and $V_{adcLMeas}$ are voltages measured at the input to the adc when the battery voltage is at its min an max value. V_{batADC} is the calculated input voltage that the arduino beetle is receiving.

$$V_{Bat} = (V_{adcBat} - V_{adcMax}) \times \frac{(V_{batMax} - V_{batMin})}{(V_{adcHMeas} - V_{adcLMeas})} + V_{batMax}$$

The calibration points used can be seen in the annotations of figure 3.18. In figure 3.18 the data from the beetle is shown in comparison to multimeter measurements and it can be said that the calibration equation worked very well.

The supply voltage starts at zero and reaches a maximum, this makes it easier to calibrate because a single measurement close to the maximum can be taken to determine the ratio of the adc input voltage to the actual supply voltage as can be seen in the following equation.

$V_{Supply} = V_{supplyADC} \times \frac{V_{measuredSup}}{V_{measuredADCSup}}$. The measured calibration point was at a adc voltage of 4.85V corresponding to 23.08V at the supply. Once again in figure 3.19 it can be seen that the multimeter measurements very closely resemble the calibrated ADC values.

To calibrate the current to the correct value the value of R_{shunt} was first determined from calculations. This was done by rearranging equation 3.7 to $R_{shunt} = \frac{(adcCurr - V_{ref})}{(50 * currMeas)}$. To do this the output voltage of 1.322V was measured as well as the discharge current of 85mA. An additional calibration point is the V_{ref} value that is also measured. From figure 3.20 it can be confirmed that the calibrated values are very close to the multimeter measurements.

The LDR value read does not need to specific final output only 100 at its maximum brightest and 0 at its darkest. To achieve this the ADC value was divided by 10 and subtracted from 110.

Figure 3.19: Supply ADC calibration

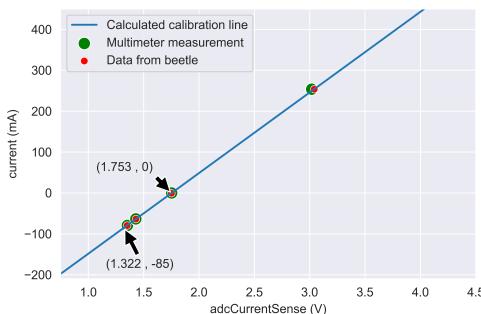


Figure 3.20: Current ADC calibration

$light_{out} = 110 - ADC_{light}/10$.

Chapter 4

Subsystem results

4.1. Voltage regulation

In the following graphs three different conditions will be setup to analyse the simulations performance. The three setups include having the supply powered on and then turning the NMOS off when it was initially on. The second setup is with the supply on and then turning the initially off NMOS, on. The last setup will be with the NMOS off and the supply off.

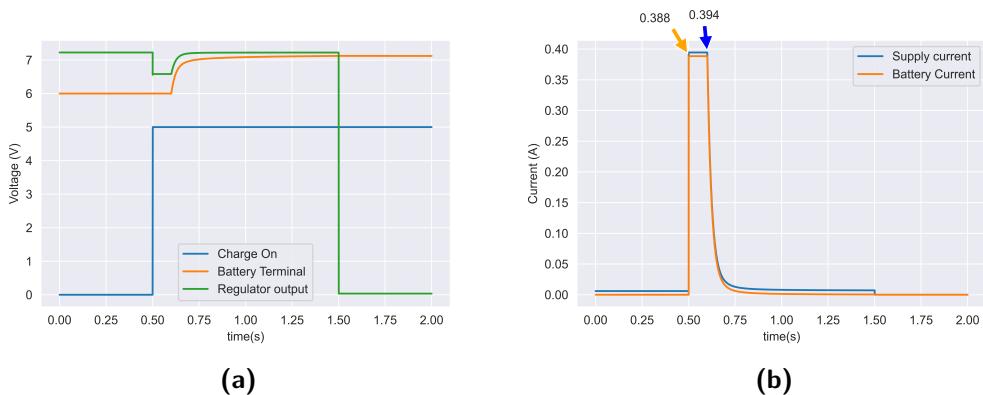


Figure 4.1: LTSPICE Results for switch turning on (a) Relevant Voltages (b) Relevant currents

From figures 4.1b it can be seen that the maximum current flowing into the battery is just under 400mA. This 400mA should correspond exactly to the Supply current, but it has an error of 1.5% which is likely to the assumptions made in the design section. The current only starts flowing when "charge on" (the control signal to the high side switch) goes high.

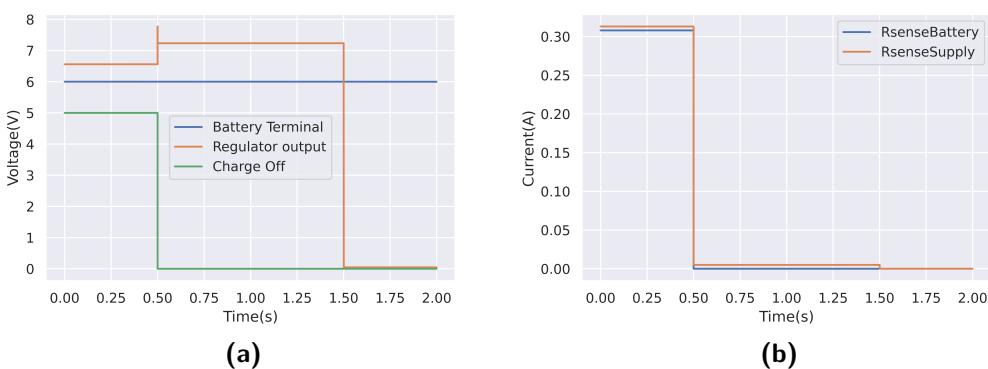


Figure 4.2: LTSPICE Results for switch turning off (a) Relevant Voltages (b) Relevant currents

In figure 4.2 it can be seen that as soon as Charge Off goes low (NMOS turns off) the current to the battery stops flowing and the battery voltage remains at 6V.

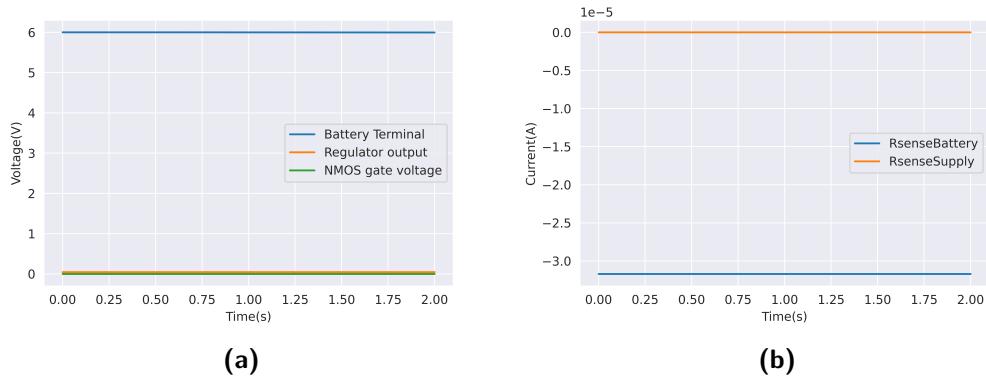


Figure 4.3: LTSpice Results for supply off and NMOS gate pulled low
 (a) Relevant Voltages
 (b) Relevant currents

In figure 4.3 both the supply and the switch are off. This then shows the discharge current of just above $30\mu\text{A}$. It is small enough that I would say specifications are met.

Table 4.1: Measured Values

Voltage at battery connection terminal [V]	
Open Circuit	7.27
1K Load	7.1
10K load	7.0

From table 4.1 it can be seen that voltage is operating in the correct region of less than 7.2V. More results regarding the charging can be found in section 5 in table 5.1.

4.2. High side switch on supply side

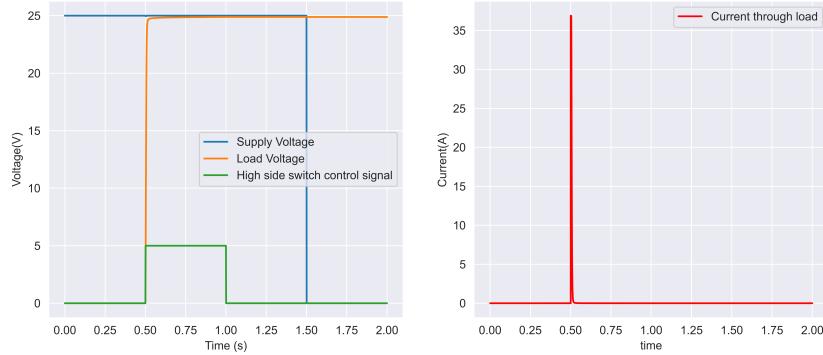


Figure 4.4: LTSPICE simulation results for high side switch on the supply side

From figure 4.4 it can be seen that as soon as the high side switch control signal goes high, the load voltage changes to approximately the supply voltage. The current spikes as seen because the capacitor at the load charges up to the supply voltage very quickly.

Table 4.2: Highside switch measurements

	voltage from source to gate of the PMOS [V]
Control signal at NMOS gate high	6.94
Control signal at NMOS gate low	0

From the values in table 4.2 it can be seen that when the NMOS gate voltage goes high a voltage above the threshold voltage of the PMOS is applied, thus turning the switch on. For additional proof that the switch works, refer to table 4.5 where this switch successfully controlled the switching on and off of the charging circuit.

4.3. Undervoltage protection

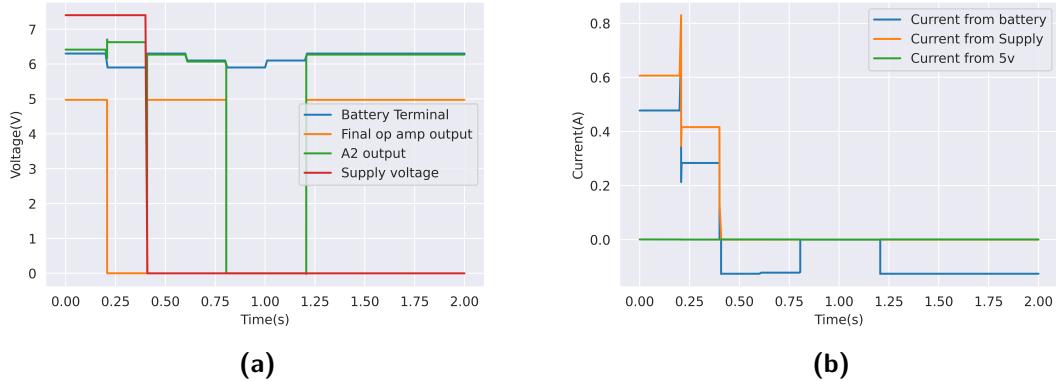


Figure 4.5: LTSPICE Under voltage circuit results (a) Relevant Voltages (b) Relevant Currents

From figure 4.5a it can be seen that the op amp transitions at the correct of 6V and 6.2V respectively. From figure 4.5b it can be seen that the current out of the 5V regulator is less than 10mA and that the op amp output corresponds to the discharging from the battery.

Table 4.3: Under voltage circuit measurements

	A2 Output [V]	Battery terminal voltage [V]
Stage 1	6.52	6.48
Stage 2	5.98	0.14
Stage 3	6.20	0.13
Stage 4	6.40	6.33

Stage 1: Battery voltage is above 6V threshold and A2 output allows discharge.

Stage 2: Battery voltage is below above 6V threshold and A2 output is 0V stopping battery discharge.

Stage 3: Battery voltage is above 6V but not 6.2V (after under-voltage circuit disconnected battery) therefore A2 output is 0V, stopping battery discharge.

Stage 4: Battery voltage is above 6.2V threshold after under-voltage circuit disconnected battery, therefore A2 is approximately equal to the battery voltage and is discharging.

4.4. Current sense

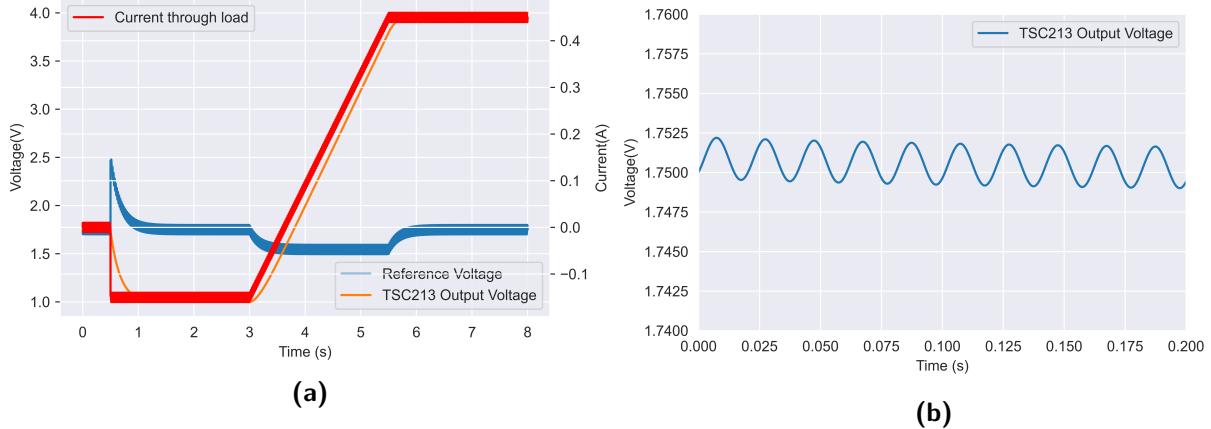


Figure 4.6: LT Spice results (a) Simulation results (b)Noise in output signal

From figures 4.6b and 4.6a it can be seen that the necessary noise specifications are achieved and that the correct output range of 3V lies within the 0-5V boundary. The output voltage also follows the current through the load as required.

Table 4.4: Voltage across resistors when LEDs are on

	Resistor Voltage [V]	Calculated Current [mA]
R1	3.35	15.23
R2	3.34	15.18
R3	3.36	15.27
R4	3.35	15.23
R4	3.37	15.32

Table 4.5: Measured results compared to actual results

	TSC213 output voltage [V]	Measured current flow [mA]	Indicated current flow [mA]	Error [%]
Both switches off	1.75	0	0	0
Highside switch on	2.28	-	-	-
Both switches on (3 LEDs)	2.06	-	-	-
Low side switch on(3 LEDs)	1.525	45.8	45	1.75
Low side switch on(5 LEDs)	1.383	73.4	76.2	3.85

For the following explanation eq.3.7 will help explain reasoning. When both switches are off the current flowing through the sense resistor is 0A. For this reason the output is equal to the reference voltage. When the High side switch turns on a positive current flows through the sense resistor, therefore the output increases. As the low side switch switches on, both switches are now on. The output voltage is still higher than the reference voltage because the charging current is greater than the discharging current resulting in a net positive current flow.

When the high side switch then turns off the output voltage moves to below the reference voltage because now there is a net negative current through the resistor. As the last 2 LEDs are turned on the output of the TSC213 drops further as the negative (discharging) current increases.

The measured noise on the output of the TSC213 was found to be 40mV (V_{PK-PK}) on the oscilloscope. Larger capacitors were added to try reduce the noise, this was not successful. When the wall plug was powered off and only the battery was supplying the peak to peak voltage dropped to 8mV. This then identified the largest source of noise as the wall plug. Once again a large capacitor was used to try filter out the noise from the 12V, however this also did not decrease the output noise. The current through the LEDs is slightly less than 20mA as can be seen in table 4.4 as a result of the resistors chose in section 3.6. Regardless of the noise relatively accurate current measurements were obtained from the TSC213 output as can be seen in table 4.5.

4.5. Low-side switch

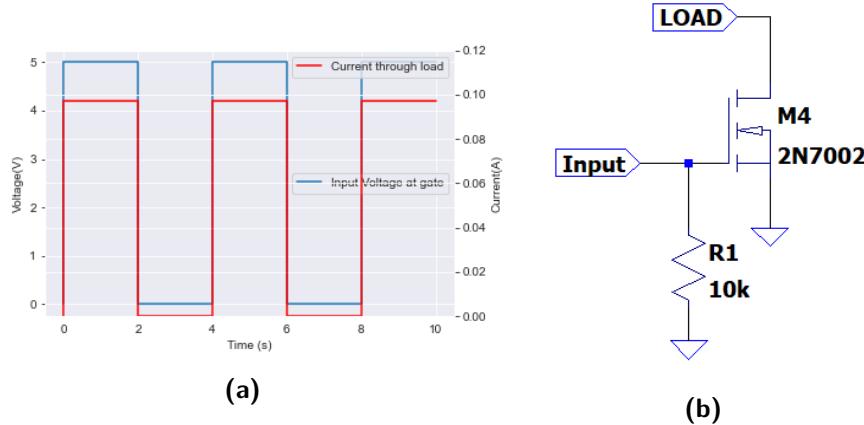


Figure 4.7: NMOS final Results (a) LT Spice simulation (b)Lowside circuit used

The above LTspice simulation in figure 4.7a was setup to have a load that had 100mA flowing through it. It shows that the NMOS was able to switch this amount of current with ease using a 5V control signal. Using this circuit practically the low side switching in figure 4.8 was achieved, indicating that it was able to enable and disable discharge through the load.

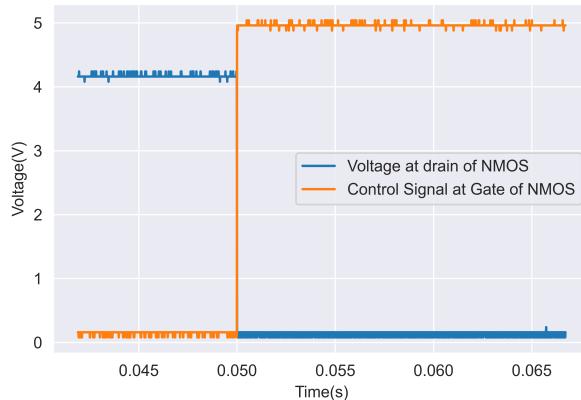


Figure 4.8: Oscilloscope Measurements of NMOS while switching

From figure 4.8 it can be seen that the switching time of the NMOS is virtually instantaneous and also simply that the NMOS switching capability is working correctly. The NMOS source is connected to ground, therefore when the control signal goes high the NMOS "connects" its drain to its source which is ground.

4.6. Supply Voltage measurement

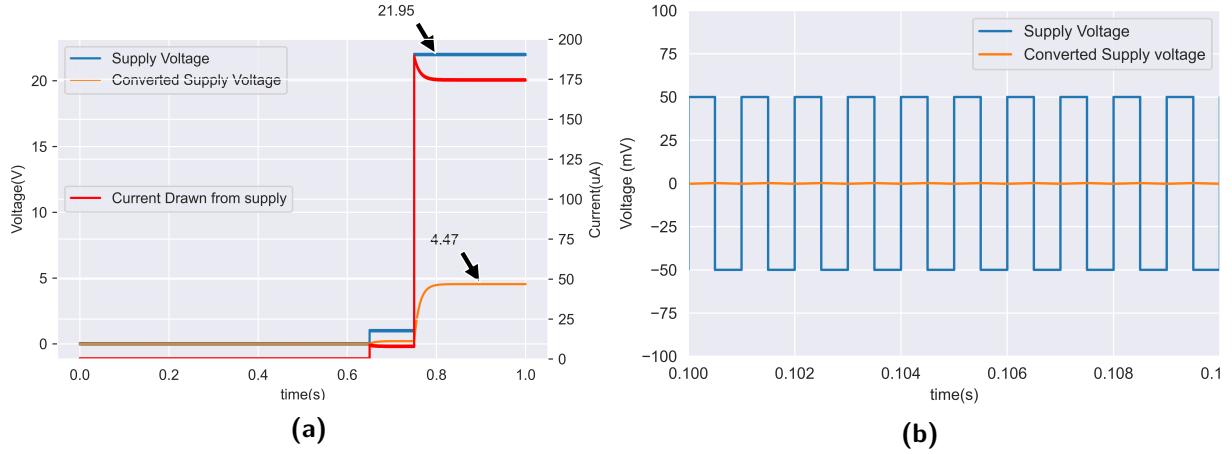


Figure 4.9: LTSPICE supply measurement simulation results (a) Supply before and after signal conditioning with current drawn from supply (b) Noise on supply input compared to converted supply voltage

From figure 4.9a the converted supply signal is the voltage measured by the ADC. As the supply voltage increases the converted supply signal varies between zero and 4.54V. It does not vary between 0 and exactly 5V because of the additional precaution of 24V as the maximum input voltage where the max input voltage here is 22V. The noise that can be seen in figure 4.9b is significantly reduced in the converted signal. The speed of the signal is not severely slowed as can be seen in figure 4.9a where the converted supply voltage nearly changes 5V in less than 100ms.

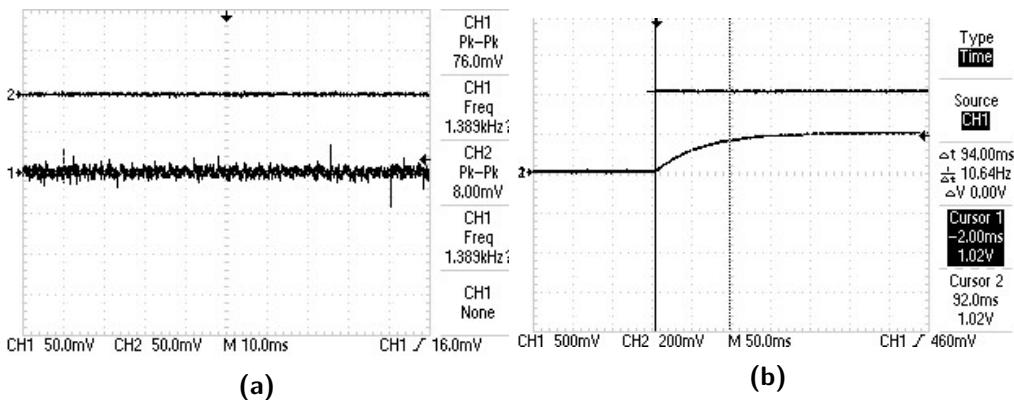


Figure 4.10: Oscilloscope Measurements of response time and noise of Supply measuring (a) Input vs Output battery signal noise (b) Response time of converted battery signal

From figure 4.9a it can be seen that the rise time for a step input of one volt is only just less than 100ms, and therefore meets the requirements. The noise in figure 4.9b can be seen to have significantly decreased from 76mV to 8mV giving a significantly cleaner output signal.

4.7. Battery Voltage measurement

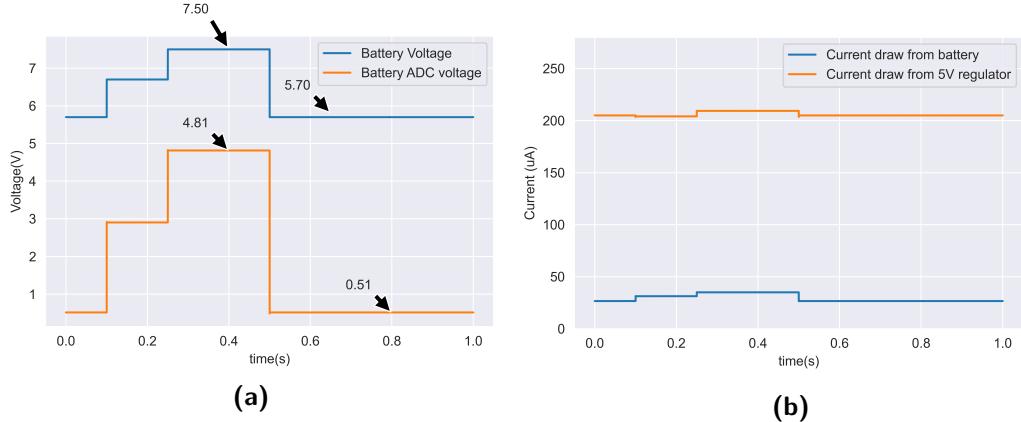


Figure 4.11: LTSPICE battery measurement simulation results (a) Battery before and after signal conditioning (b)Battery Current and 5V regulator current

From the results seen in figure 4.11a the ADC battery voltage increases as the battery voltage increases. The ADC battery voltage should vary between 0.5V and 4.8V. The simulation is only 0.01V from the expected values, this is likely a result of resistor values that are chosen. The current drawn from the battery directly as well as indirectly through the 5V regulator sum to less than $300\mu A$ indicating minimal current usage.

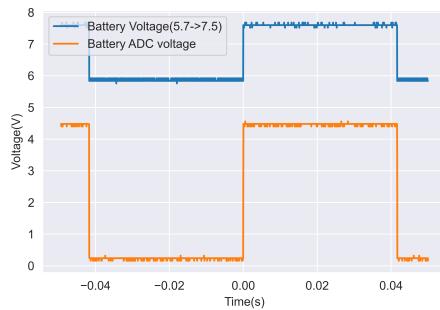


Figure 4.12: Oscilloscope data of rise time of battery voltage measuring circuit

Table 4.6: Battery Measuring circuit measurements

Battery voltage [V]	ADC Voltage [V]	Expected ADC voltage [V]	error [%]
6	1.29	1.23	4.88
6.6	2.80	2.76	1.45
7.2	4.04	4.10	1.46

From figure 4.12 it can be seen that the rise time of channel 1 (ADC voltage) is practically instant and that the designed range is approximately achieved. Table 4.6 represents the ADC voltage at the specific battery voltages and the error between the ADC voltage and the theoretical ADC voltage.

4.8. Ambient light sensor circuitry

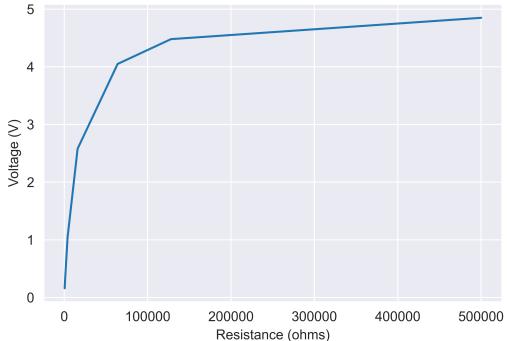


Figure 4.13: LTSPICE LDR graphed simulation results

Light condition	ADC voltage [V]
Complete darkness	4.88
Torch level 1-box elevate 2cm	3.42
Torch level 1-box elevate 4cm	2.88
Torch level 1-no box	1.6
Torch level 3	1.135
Torch level 5	0.84

Table 4.7: LDR ADC measured results

To get the large range of measurements in table 4.7 a phone with five different torch brightness settings is held above the LDR and the ADC voltage is measured. Initially at "torch level 1" a box is placed over the LDR and the box is elevated in increments. Then the box is removed and the torch brightness is increased. The simulated results do achieve a larger range than the practical results. This may be because exact conditions for "darkness" and "light" in the measurements were not achieved.

4.9. Load and pilot LED control

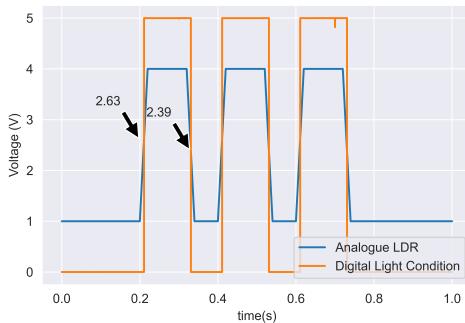


Figure 4.14: LTSPICE Digital light condition results

Table 4.8: Hysteresis Measurement of light condition circuit

Measured Voltage [V]	Expected Voltage [V]
V_{TU}	2.58
V_{TL}	2.37

From figure 4.14 it can be seen that as the analogue LDR signal goes above and below the annotated thresholds, an digital signal is produced that represents whether it is light or dark. This is correct however both the measured thresholds are different to what is expected as can be seen from table 4.8. This is likely due to the resistors chosen to match lab resistors for the simulation, and resistor tolerances for the practical circuit.

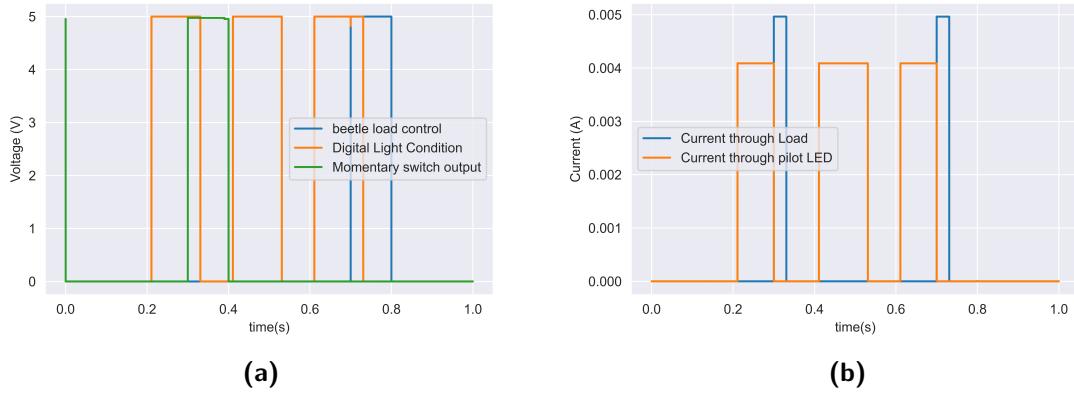


Figure 4.15: LTSPICE Load Control results (a) Voltages relevant to load control (b) Current through load

In figure 4.15 the current flow indicates when the load LED is on (magnitude unimportant). It should only be on when it is dark and when either the beetle load control or the momentary switch is high. From the current graph in figure 4.15b it can be seen that current flows at two intervals, and when looking at figure 4.15a, it happens at the same time that both the load control (this includes both the beetle and switch) and the light condition are high as expected. The pilot LED should only be on when it is dark and the load control is off (both momentary and beetle). In figure 4.15b this happens when both the momentary switch and the load control voltage is off and light condition is on. This means it is working as expected.

Table 4.9: Measured Voltages for Load control and pilot LED

PWM [V]	MomentarySwitch [V]	LightCondition [V]	Load [V]	PilotLED [V]
4.97	0	0	0	0
4.97	0	4.95	0	1.91
4.97	4.95	0	0	0
4.97	4.95	4.95	6.03	0

The above table 4.9 was taken to indicate that the truth table in the design section corresponds to the practical circuit. The Momentary switch and the "light condition" were controlled manually. The tables do correspond indicating that the design worked as indicated. One thing that must be taken into consideration is that when the load was being powered a voltage of 0.38V was measured across the three NMOS's at the load, this is a significant voltage.

Chapter 5

System results

The complete circuit charging characteristics are documented in table 5.1. The current measurements are calculated from the TSC output using eq.3.7. A2 output refers to the output of the second assignment which can be seen in figure 3.8. When comparing the tabulated results to graph 4.1 it can be said that these values are definitely comparable meaning that the practical circuit achieves its purpose.

Table 5.1: Charging circuit measurements

Battery voltage while charging [V]	Charging current [mA]	A2 output voltage [V]
6.38	210	6.48
6.42	192	6.51
6.46	164	6.57
6.53	152	6.60
6.63	134	6.69
6.64	132	6.7

With the circuit built up until this stage it was deemed necessary to recheck the hysteresis thresholds V_{TU} and V_{TL} . From table 5.2 it can be seen that the thresholds are very close to the designed thresholds. The voltage following op amps likely stopped the external circuit from interfering with the voltages at the inputs of the op amps.

Table 5.2: Hysteresis Measurement

Measured Voltage [V]	Expected Voltage [V]
V_{TU}	6.22
V_{TL}	6.02

From the 2 figures in figure 5.1 it can be said that the switches worked effectively in conjunction with the battery under voltage and charging circuits because as each switched changed state current discharged (NMOS ON, TSC output is below 1.75V) or charged (PMOS ON TSC output is above 1.75V). From these graphs it can also be seen that the time it takes for the output to change is less than 20 milliseconds which is fast.

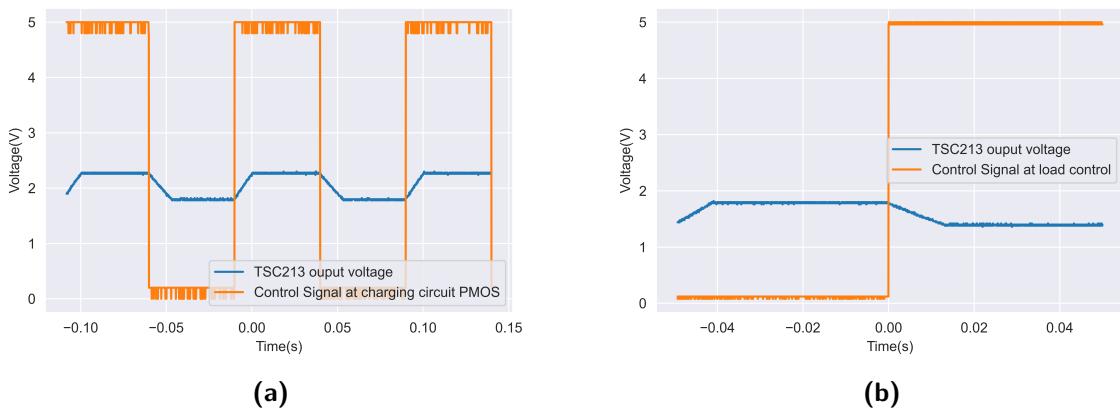


Figure 5.1: Oscilloscope switch evaluation of in system (a) High Side switch used to change TSC213 output (b) Low side circuit used to change TSC213 output

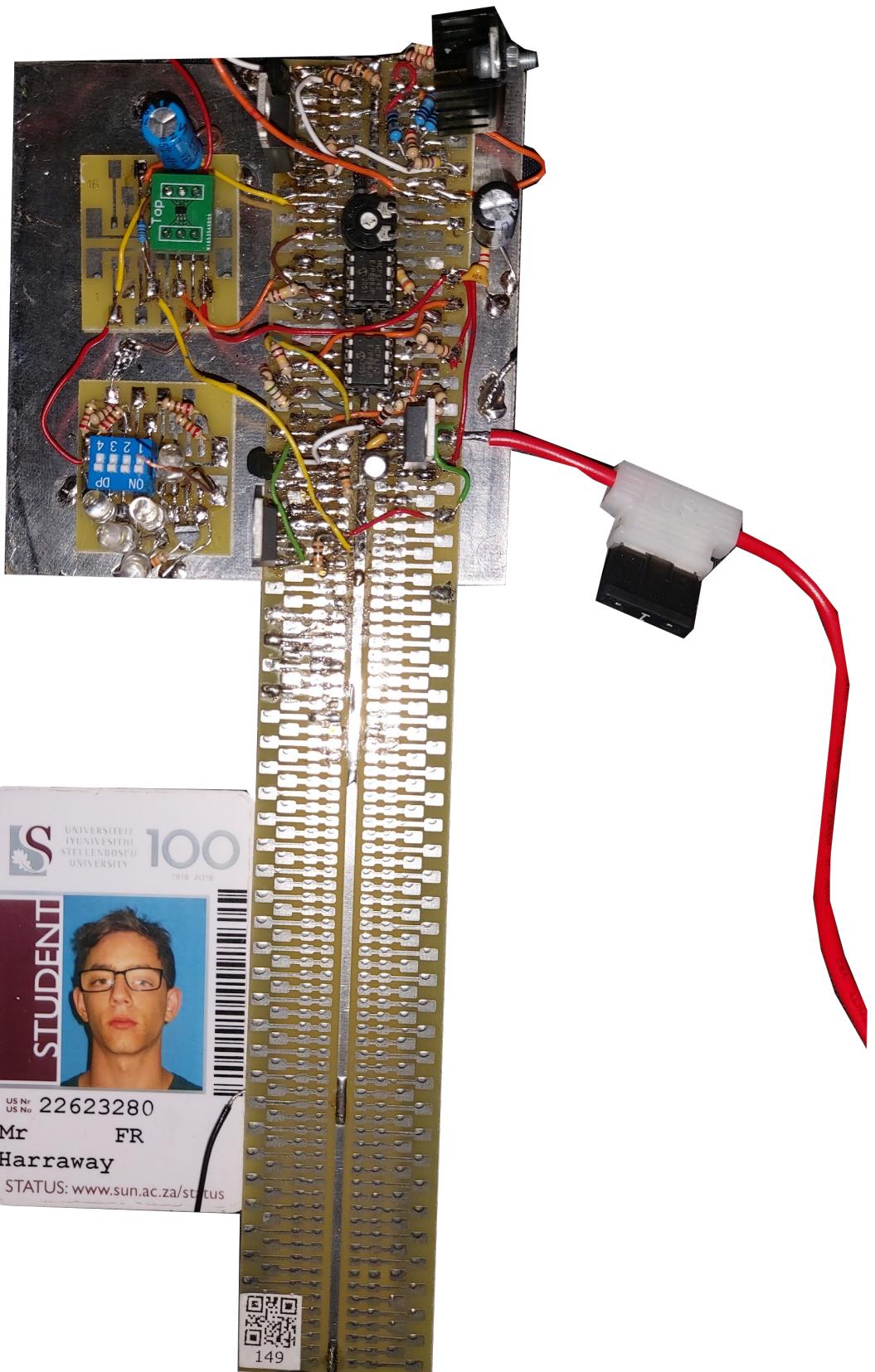


Figure 5.2: Circuit with barcode and Student Card

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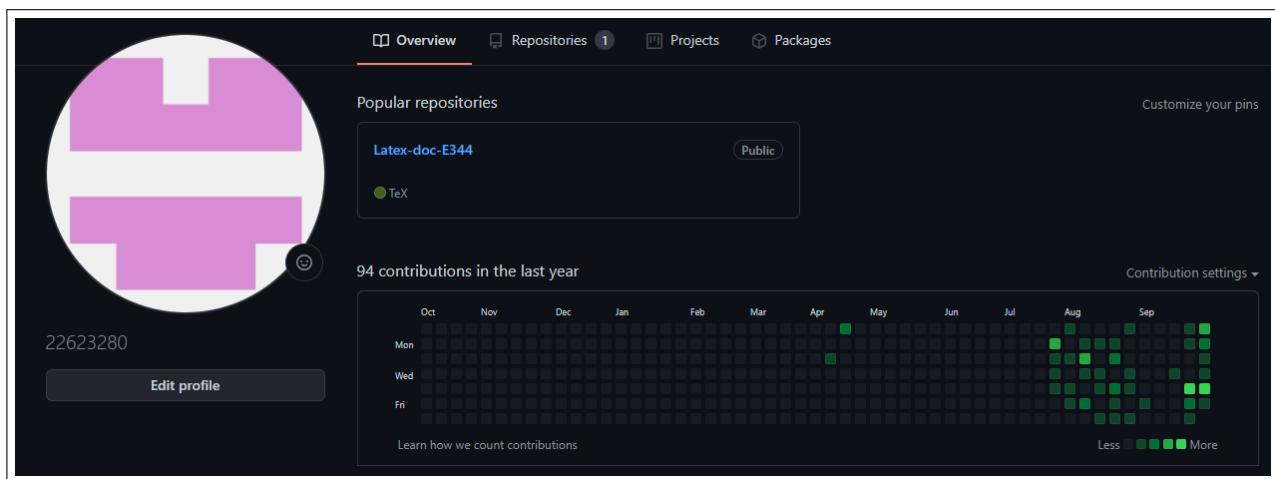
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Appendix A

GitHub Activity Heatmap



Appendix B

Data sheet info

Figure 2. Block diagram

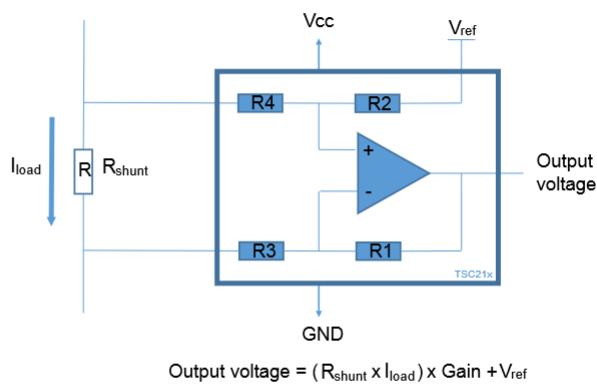


Table 2. Resistors and gain values

Product	R1 and R2	R3 and R4	Gain
TSC210	1 MΩ	5 kΩ	200
TSC212	1 MΩ	1 kΩ	1000
TSC213	1 MΩ	20 kΩ	50

Figure B.1: tsc213 data sheet information

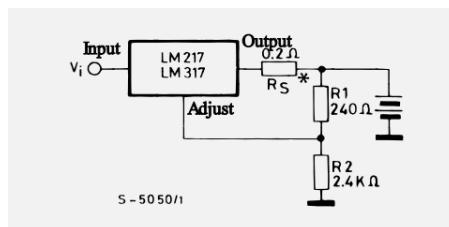


Figure B.2: Application Circuit For LM317 [4]

Table B.1: Thermal Resistance Values [7] [4]

Thermal Resistance [°C/W]	
θ_{j-c}	5
$\theta_{s-a}(\text{worstcase})$	20
θ_{j-a}	50

Appendix C

Hysteresis Calculations

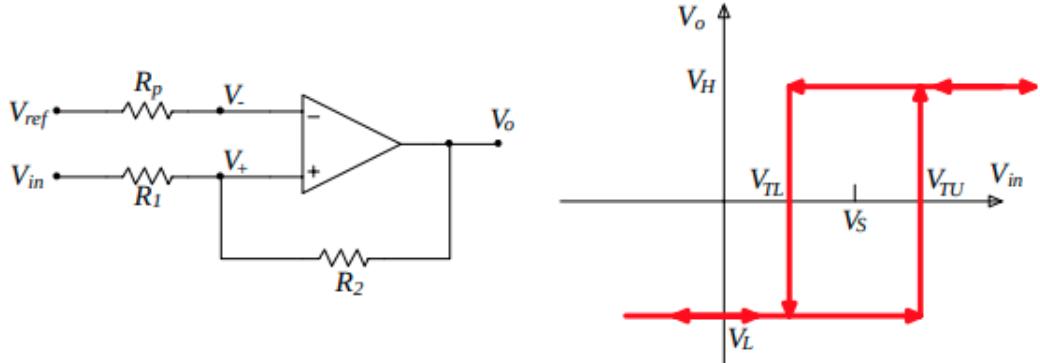


Figure C.1: Non inverting Schmidt trigger [6]

For this analysis it will be assumed that we are working with an ideal op amp.

$$V_+ = V_- \quad (C.1)$$

Take a KCL at V_+ in figure C.1:

$$\frac{V_+ - V_{in}}{R_1} + \frac{V_+ - V_o}{R_2} = 0 \quad (C.2)$$

Take a KCL at V_- in figure C.1:

$$\frac{V_- - V_{REF}}{R_p} = 0 \quad (C.3)$$

From equation C.3 the following result is achieved.

$$V_- = V_{REF} \quad (C.4)$$

After rearranging eq. C.2 with V_{in} as the subject. Also substitute C.4 into C.2:

$$V_{in} = \frac{V_{REF} \times (R_1 + R_2)}{R_2} - \frac{V_o \times R_1}{R_2} \quad (C.5)$$

The following two equations C.6 and C.7 are derived for the two scenarios where the output is at V_H as well as V_L . At V_H we want to find the voltage V_{TL} where the the output will change rails to V_L . At V_L we want to find the voltage V_{TU} where the the output will

change rails to V_H :

$$V_{TL} = \frac{V_{REF} \times (R_1 + R_2)}{R_2} - \frac{V_H \times R_1}{R_2} \quad (\text{C.6})$$

$$V_{TU} = \frac{V_{REF} \times (R_1 + R_2)}{R_2} - \frac{V_L \times R_1}{R_2} \quad (\text{C.7})$$

Now to achieve the following equation, subtract eq. C.6 from eq. C.7:

$$V_{TL} - V_{TU} = \frac{(V_H - V_L) \times R_1}{R_2} \quad (\text{C.8})$$

Rearrange eq. C.8 to achieve the following equation:

$$\frac{V_{TL} - V_{TU}}{(V_H - V_L)} = \frac{R_1}{R_2} \quad (\text{C.9})$$

After calculating $\frac{R_1}{R_2}$ and therefore suitable resistors V_{REF} can be found using the following equation. The following equation is obtained by making V_{REF} the subject of equation C.6:

$$V_{REF} = \frac{V_{TL} \times (R_2)}{R_1 + R_2} + \frac{V_H \times R_1}{R_1 + R_2} \quad (\text{C.10})$$

Appendix D

Differential amplifier calculations

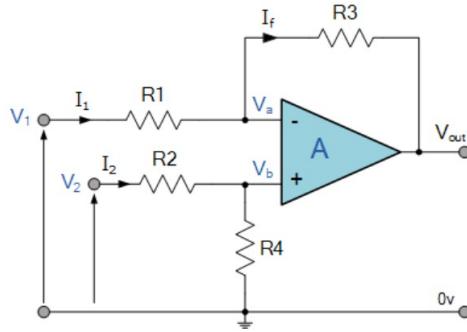


Figure D.1: Differential amplifier op amp setup [29]

$$I_1 = \frac{V_1 - V_a}{R_1}, \quad I_2 = \frac{V_2 - V_b}{R_2}, \quad I_f = \frac{V_a - (V_{out})}{R_3}$$

$$\text{Summing point } V_a = V_b$$

$$\text{and } V_b = V_2 \left(\frac{R_4}{R_2 + R_4} \right)$$

$$\text{If } V_2 = 0, \text{ then: } V_{out(a)} = -V_1 \left(\frac{R_3}{R_1} \right)$$

$$\text{If } V_1 = 0, \text{ then: } V_{out(b)} = V_2 \left(\frac{R_4}{R_2 + R_4} \right) \left(\frac{R_1 + R_3}{R_1} \right)$$

$$V_{out} = -V_{out(a)} + V_{out(b)}$$

$$\therefore V_{out} = -V_1 \left(\frac{R_3}{R_1} \right) + V_2 \left(\frac{R_4}{R_2 + R_4} \right) \left(\frac{R_1 + R_3}{R_1} \right)$$

Figure D.2: Differential amplifier op amp setup derivation [29]

If $R_1 = R_2$ and $R_3 = R_4$ then the equation will simplify to :

$$V_{out} = \frac{R_3}{R_1} \times (V_2 - V_1) \quad (\text{D.1})$$

Appendix E

Pilot LED calculations

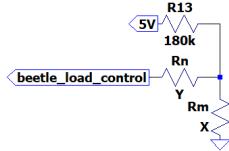


Figure E.1: V_- pilot LED calculations

R_{13} is chosen to be $180\text{k}\Omega$. When the load control is high the following equation can be found:

$$3.5 = \frac{R_m}{R_n || 180k + R_m} \quad (\text{E.1})$$

$$R_m = \frac{R_n \times 180k}{R_n + 180k} \times \frac{3.5}{1.5} \quad (\text{E.2})$$

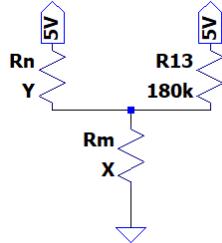


Figure E.2: V_- pilot LED calculations with load control on

When the load control is low the following equation can be found:

$$0.4 = \frac{R_x}{R_x + 180k} \quad (\text{E.3})$$

$$R_x = 15650\Omega$$

Where R_x is equal to R_n in parallel with R_m :

$$R_x = \frac{R_n \times R_m}{R_m + R_n} \quad (\text{E.4})$$

If eq.E.2 is substituted into eq. E.4 R_n can be solved for:

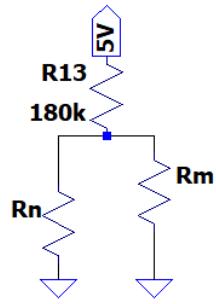


Figure E.3: V_- pilot LED calculations with load control off

$$15650 = \frac{\frac{R_n \times 180k}{R_n + 180k} \times \frac{3.5}{1.5} \times R_n}{\frac{R_n \times 180k}{R_n + 180k} \times \frac{3.5}{1.5} + R_n} \quad (\text{E.5})$$

$R_n = 23.22\text{k}\Omega$ (lab resistor of $22\text{k}\Omega$)

$R_m = 48\text{k}\Omega$ (lab resistor of $47\text{k}\Omega$)

Appendix F

Load control and pilot LED op amp voltages

Table F.1: Load control and pilot LED circuit op amp requirements [27]

	<i>Min</i> [V]	<i>Max</i> [V]	<i>Designed range/value</i> [V]
All op amps Difference between supply rails $V_{DD} - V_{SS}$	-	7	5
U1 Common mode voltage ($\frac{V_+ + V_-}{2} - V_{SS}$)	-0.3	5.3	1.45-3
U1 Differential Voltage ($ V_+ - V_- $)	-	5	1-2.1
U1 Input voltages to V_- and V_+	-1	6	0.4-3.5
U2 Common mode voltage ($\frac{V_+ + V_-}{2} - V_{SS}$)	-0.3	5.3	0-5
U2 Input voltages to V_- and V_+	-1	6	0-5
U3 Common mode voltage ($\frac{V_+ + V_-}{2} - V_{SS}$)	-0.3	5.3	1.27-3.67
U3 Input voltages to V_- and V_+	-1	6	0.03-4.85
U3 Differential Voltage ($ V_+ - V_- $)	-	5	1-2.47
U4 Common mode voltage ($\frac{V_+ + V_-}{2} - V_{SS}$)	-0.3	5.3	2.5-4.5
U4 Input voltages to V_- and V_+	-1	6	0-4.5
U4 Differential Voltage ($ V_+ - V_- $)	-	5	2.5-4.5
U5 Common mode voltage ($\frac{V_+ + V_-}{2} - V_{SS}$)	-0.3	5.3	0.01-2.92
U5 Input voltages to V_- and V_+	-1	6	0.03-4.85

All op amps are within boundaries.