

Combinational Logic

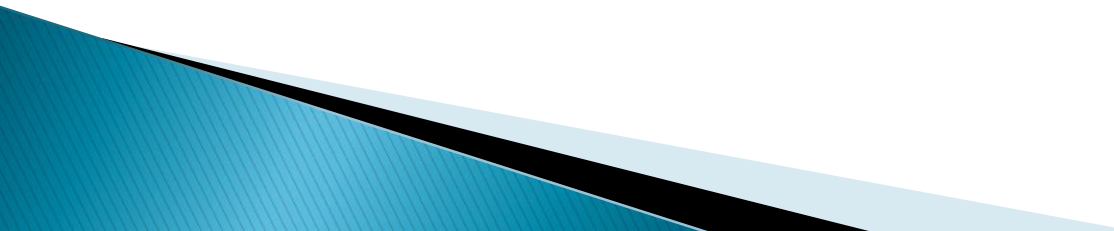
Part II: Arithmetic Circuits

- Binary Adder and Subtractor

Adders

- ▶ A combinational circuit that performs the addition of two bits is called a **half-adder**. One that performs the addition of three bits (two significant bits and a previous carry) is a **full-adder**. The name of the former stems from the fact that two half-adders can be employed to implement a full-adder.

Half-Adder

- ▶ The input variables designate the **augend** (first bit) and **addend** (second bit); the output variables produce the **sum** and **carry**. It is necessary to specify two output variables because the result may consist of two binary digits. We arbitrarily assign symbols x and y to the two inputs and S (for sum) and C (for carry) to the outputs.
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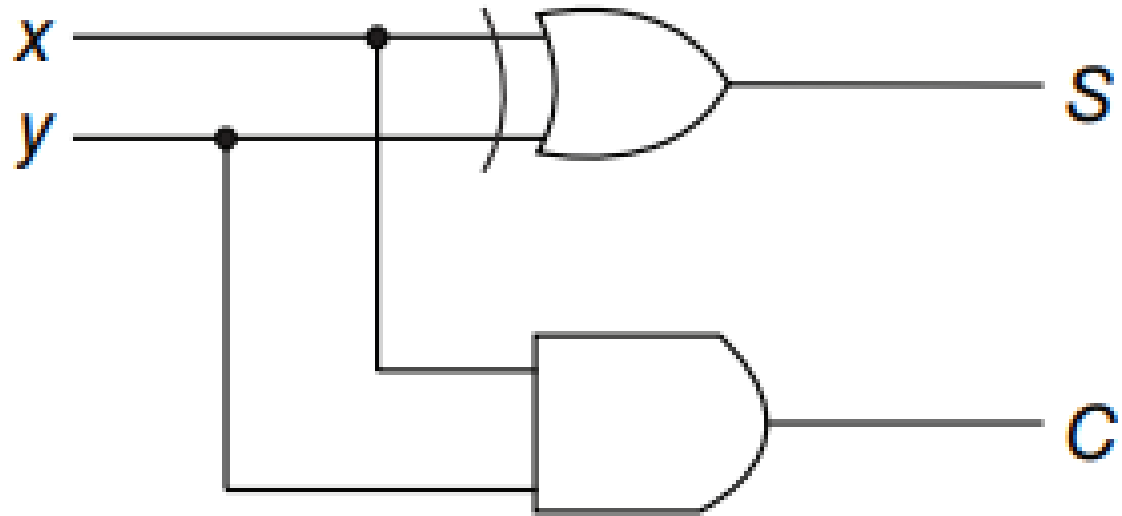
Truth table for Half-Adder:

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$S = x'y + xy'$$

$$C = xy$$

Logic Diagram:



$$S = X \oplus Y$$

$$C = XY$$

Full Adder

- ▶ Design a combinational circuit that adds 3 input bits (x, y, z) to generate a Sum (S) bit and a carry-out (C) bit.

Truth Table

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Simplification using K-map:

		y			
		yz			
		00	01	11	10
x	0		1		1
x	1	1		1	
		z			

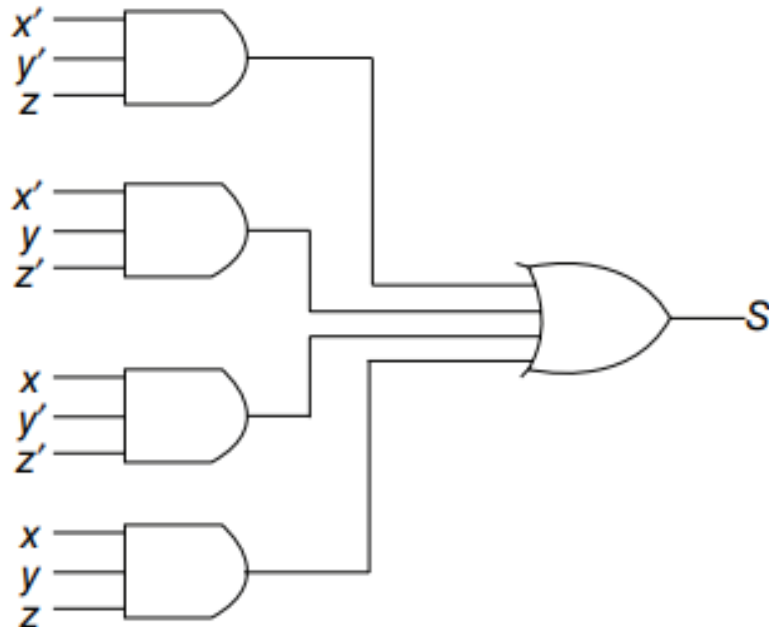
$$S = x'y'z + x'yz' + xy'z' + xyz$$

		y			
		yz			
		00	01	11	10
x	0			1	
x	1		1	1	1
		z			

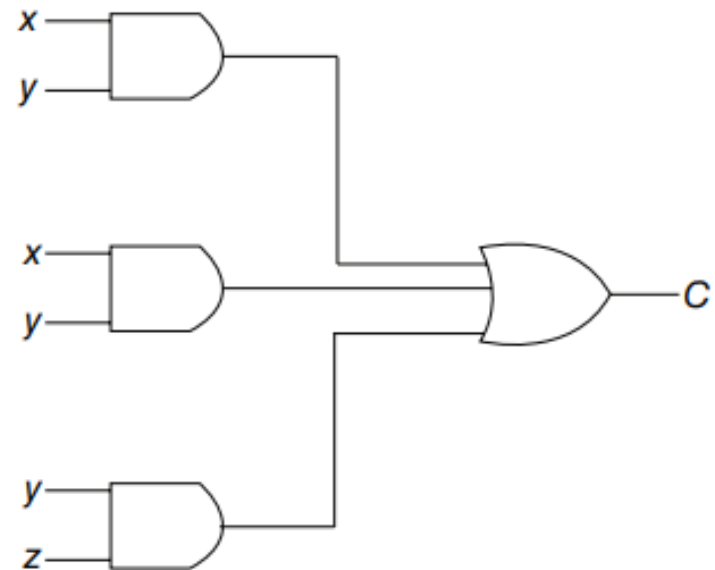
$$C = xy + xz + yz$$

Logic diagram (SOP)

$$S = x'y'z + x'yz' + xy'z' + xyz$$



$$C = xy + xz + yz$$



Seatwork #2: (Final Term)

- ▶ Implement a Full Adder using two-half adders and an OR gate.

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

- ▶ Hint: Use this table to get minterms for C and S.

Full Adder using two half-adders and an OR gate

$$\begin{aligned} S &= x'y'z + x'yz' + xy'z' + xyz \\ &= z'(x'y + xy') + z(xy + x'y') \rightarrow \text{XNOR} \\ &= z'(x'y + xy') + z(x'y + xy')' \rightarrow \text{complement of XNOR is XOR} \\ &= z'(x \oplus y) + z(x \oplus y)' \text{ let } x \oplus y = w \\ &= z'w + zw' \\ &= z \oplus w \end{aligned}$$

Therefore:

$$S = z \oplus (x \oplus y)$$

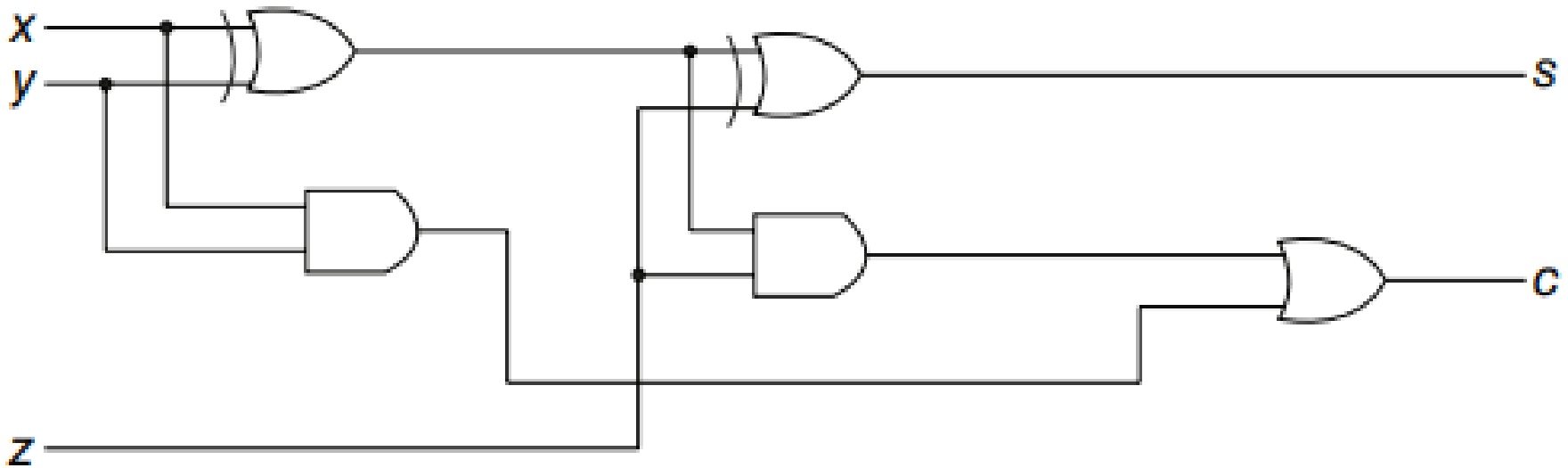
$$C = xy'z + x'yz + xy = z(xy' + x'y) + xy$$

$$C = z(x \oplus y) + xy$$

Implementation of full-adder with two half-adders and an OR gate

$$S = z \oplus (x \oplus y)$$

$$C = z(x \oplus y) + xy$$

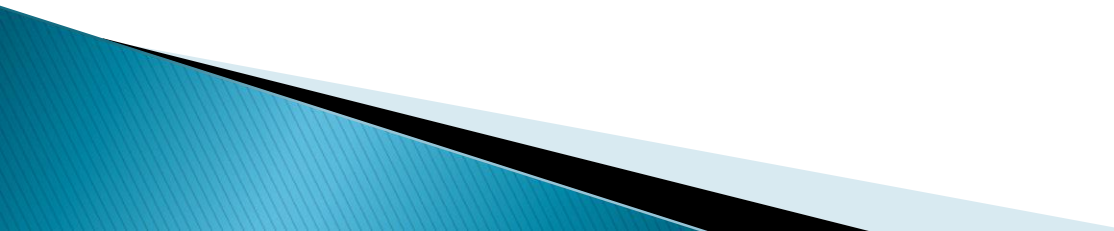


BINARY SUBTRACTOR



Binary Subtraction Circuits

Another basic arithmetic operation to be performed by Digital Computers is the Subtraction. Subtraction is a mathematical operation in which one integer number is deducted from another to obtain the equivalent quantity. The number from which other number is to be deducted is called as 'Minuend' and the number subtracted from the minuend is called 'Subtrahend'.



Binary Subtraction Circuits

Similar to the binary addition, binary subtraction is also has four possible basic operations. They are:

$$0 - 0 = 0$$

$$0 - 1 = 1 \text{ (Borrow) } 1$$

$$1 - 0 = 1$$

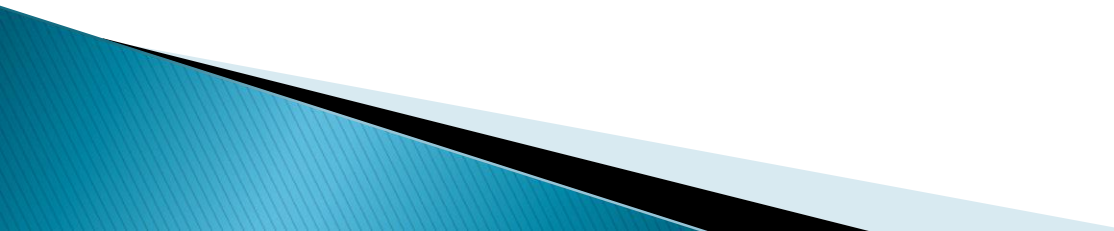
$$1 - 1 = 0$$

Similar to the adder circuits, basic subtraction circuits are also of two types:

- ▶ Half Subtractor
- ▶ Full Subtractor

Half Subtractors

A Half Subtractor is a multiple output Combinational Logic Circuit that does the subtraction of two 1-bit binary numbers. It has two inputs and two outputs. The two inputs correspond to the two 1-bit binary numbers and the two outputs corresponds to the Difference bit and Borrow bit (in contrast to Sum and Carry in Half Adder).



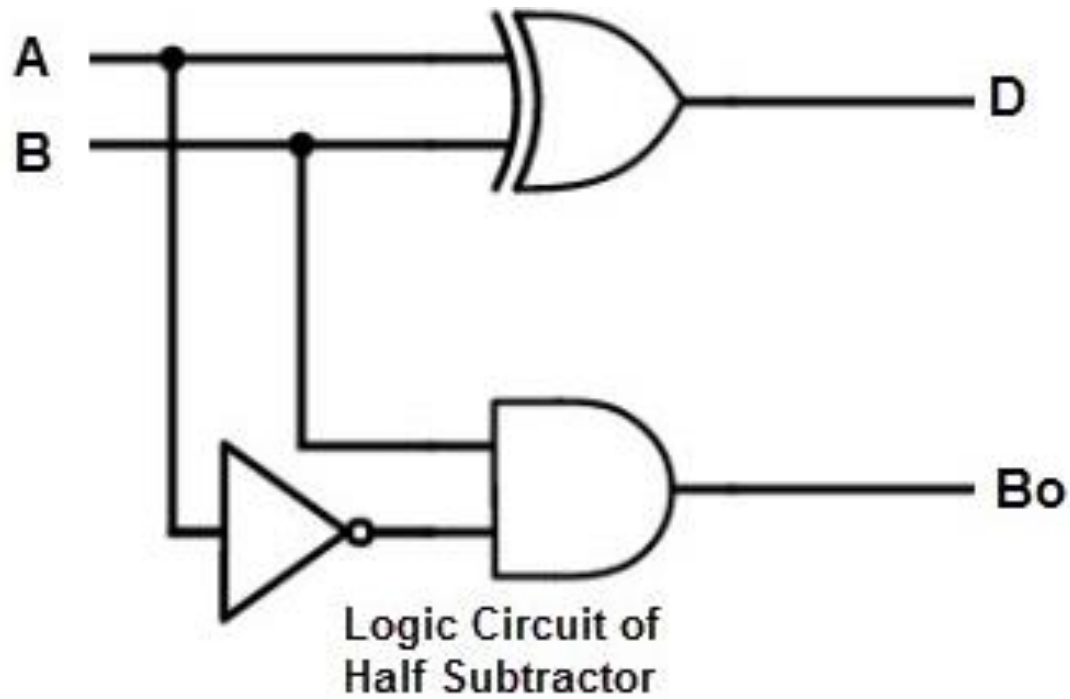
Truth Table

A	B	D	B ₀
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$D = A'B + AB' = A \oplus B$$

$$B_0 = A'B$$

Logic Circuit



Assignment #1: (40 pts)

- ▶ Design a combinational circuit for Full Subtractor having 3 inputs (A,B,C) and 2 outputs, difference D and borrow bits B. Implement the circuit using two half subtractors and an OR gate.