Digital electronics

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MINISTRY OF EDUCATION,
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The Study of Modern and Developing Engineering BUT
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The repository contains VHDL lab exercises for bachelor course *Digital Electronics* at Brno University of Technology, Czechia.

Exercises

EDA Playground

1. Introduction to Git and VHDL
2. Combinational logic

Vivado

3. Introduction to Vivado
4. Seven-segment display decoder
5. Binary counter
6. Driver for multiple seven-segment displays
7. Latches and Flip-flops
8. Stopwatch
9. Traffic light controller

VHDL project

9.-13. General instructions

Materials

The following hardware and software components are mainly used in the lab.

Hardware

- Nexys A7 Artix-7 FPGA Trainer Board: reference manual, schematic, XC7A50T-1CSG324C FPGA, Nexys-A7-50T-Master.xdc
- Oscilloscope Keysight Technologies DSOX3034T (350 MHz, 4 analog channels), including 16 logic timing channels DSOXT3MSO and serial protocol triggering and decode options D3000BDLA

Software

- EDA Playground
- Vivado Design Suite 2020.1: installation
- git

References

1. ES 4 VHDL reference sheet
2. Digital electronics 1 wiki
3. ASHENDEN, Peter J. *The designer's guide to VHDL.* 3rd ed. Boston: Morgan Kaufmann Publishers, c2008. ISBN 978-0-12-088785-9.
4. CHU, Pong P. *FPGA prototyping by VHDL examples.* Hoboken, N.J.: Wiley-Interscience, c2008. ISBN 978-0-470-18531-5.
5. MANO, M. Morris. Digital Design: With an Introduction to the Verilog, HDL, VHDL, and System Verilog. Pearson, 6th edition, 2018. ISBN-13: 978-1292231167.
6. KALLSTROM, P. A Fairly Small VHDL Guide. Version 2.1.
7. GitHub GIT CHEAT SHEET