NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2024-2025

EE6306 – DIGITAL INTEGRATED CIRCUIT DESIGN

April / May 2025 Time Allowed: 3 hours

INSTRUCTIONS

1. This paper contains 5 questions and comprises 5 pages.
2. Answer all 5 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.

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1. (a) An NMOS transistor is fabricated using the 0.25-μm CMOS technology. The process uses a doping level of $N_A = 8\times10^{16}$ cm^{-3}, $\beta = 350$ μA/V^2, $W = 6\lambda$, and $L = 2\lambda$. The transistor has a nominal threshold voltage of 0.7 V, and its body is tied to the source. Assume that $\varepsilon_{ox} = 3.9\varepsilon_o$, $\varepsilon_{Si} = 11.7\varepsilon_o$, $\varepsilon_o = 8.85\times10^{-14}$ F/cm, thermal voltage $V_T = 26$ mV and $n_i = 1.6\times10^{10}$ cm^{-3}.

   (i) The SiO_2 gate oxide of the NMOS transistor is 3-nm thick. When SiO_2 is replaced by a high-k material of the same thickness, the gate capacitance tripled. Calculate the dielectric constant of the high-k material and explain the purpose of using a high-k dielectric gate material.

   (ii) Calculate the I_{ds} current of the NMOS transistor for the below following biasing conditions:

   I. $V_{gs} = 3$ V and $V_{ds} = 3$ V.

   II. $V_{gs} = 0.5$ V and $V_{ds} = 1$ V.

   III. $V_{gs} = 5$ V and $V_{ds} = 3$ V.

(10 Marks)

Note: Question No. 1 continues on page 2.

(b) If a potential difference exists between the source and body of the NMOS transistor, such that $V_{sb} > 0$, what will happen to the threshold voltage? How will the threshold voltage vary if the doping level in the transistor is also reduced?

(5 Marks)

(c) State two main differences between the long-channel and short-channel devices?

(5 Marks)

2. (a) (i) Deduce the logic function of the CMOS circuit shown in Figure 1.

(ii) Based on CMOS *n*-well process, and using continuous *p*- and *n*-diffusion lines, draw a stick diagram for the circuit in Figure 1.

(10 Marks)

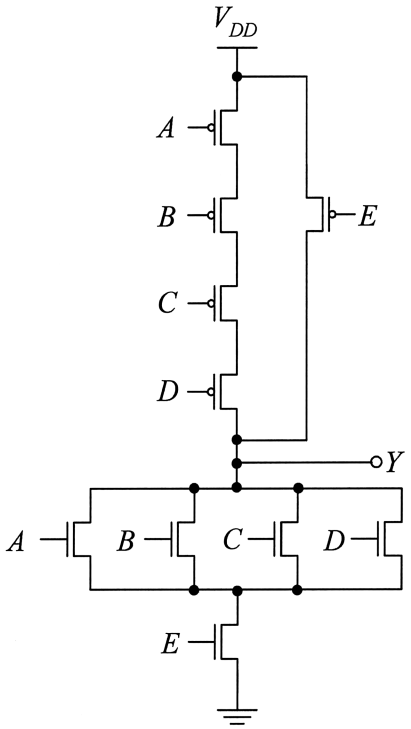

Figure 1

Note: Question No. 2 continues on page 3.

(b) Describe the operation of the BiCMOS circuit shown in Figure 2 and state the key advantages of this circuit.

(10 Marks)

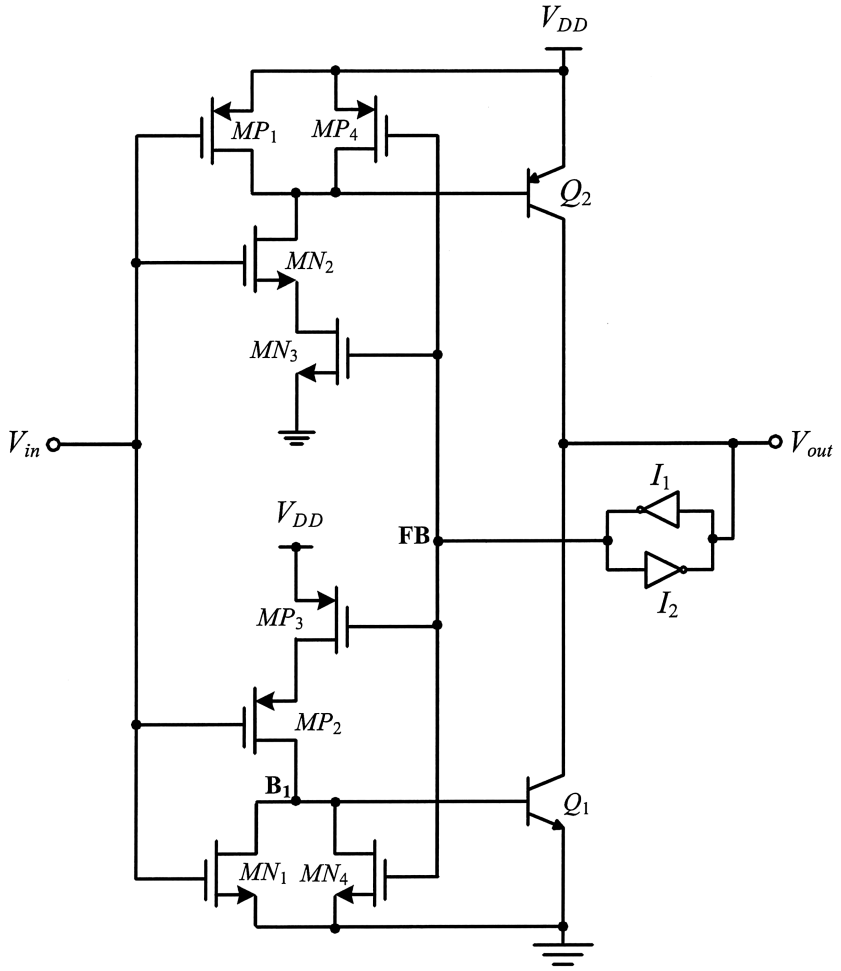

Figure 2

3. (a) (i) The power dissipation in a digital CMOS circuit can typically be categorized into two main components, static power and dynamic power. List the various contributing factors for static and dynamic power dissipation.

(ii) Unnecessary glitches can be reduced to lower switching activity. Using a chain of five 2-input NAND gates, where one input of all five gates undergoes a logic 0-to-1 transition and the other input of the first gate is tied to 5V, show how glitches can occur with appropriate waveforms.

(10 Marks)

(b) (i) Sequential circuits typically incorporate latches or registers in the design. Draw a static multiplexer-based D-latch and a dynamic multiplexer-based D-latch with MOS transistors, logic NOT gates and any other necessary components.

(ii) In general, the C^2MOS latch can be re-designed using a single-phase clock into a True Single-Phase Clock (TSPC) latch. Sketch your design of a TSPC latch and briefly describe the circuit operation.

(10 Marks)

4. (a) In architecture synthesis of VLSI systems, one of the main tasks is data path allocation. Briefly explain data path allocation. State and explain the major sub-tasks in data path allocation.

(10 Marks)

(b) Testing is one of the important processes in the manufacture of digital integrated circuits. One of the algorithms used to generate test patterns is the D algorithm. Use the D algorithm to derive a test vector for the inputs (a, b, c, d, e) of the logic circuit in Figure 3 to detect a stuck-at-0 (SA0) fault at the point X. Determine the values at the nodes X, Y, P and Q for this test vector. What is the value at the output f, and what does the output value indicate?

(10 Marks)

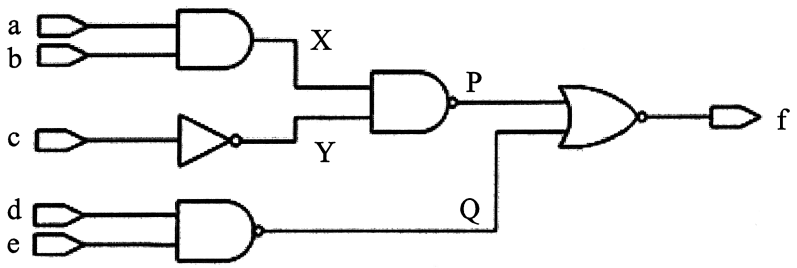

Figure 3

5. The dot diagram representing the partial products of a 4-bit by 4-bit binary multiplication is shown in Figure 4. Carry-save technique is often used to reduce the carry propagation delay in the summation of partial products. Wallace adder tree and Dadda adder tree use the carry-save technique.

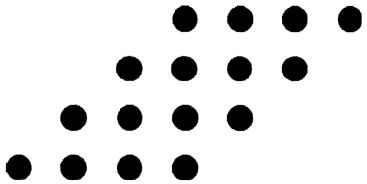

Figure 4

(a) Explain the concept of carry-save technique and how the carry propagation delay is reduced.

(6 Marks)

(b) Using the usual notation, draw a Wallace adder tree for the summation of the partial products in the dot diagram in Figure 4 with clear indications of the stages. State how many full adders and half adders are used in each stage.

(6 Marks)

(c) Repeat Part (b) for a Dadda adder tree.

(6 Marks)

(d) Compare the advantages and disadvantages of the Wallace adder tree and the Dadda adder tree.

(2 Marks)

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.