NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2024-2025

EE6306 – DIGITAL INTEGRATED CIRCUIT DESIGN

November / December 2024 Time Allowed: 3 hours

INSTRUCTIONS

1. This paper contains 5 questions and comprises 7 pages.
2. Answer all 5 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.

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1. (a) (i) For the circuit shown in Figure 1 on page 2, derive an expression for the output Z.

(ii) Prove that the function of Z in Figure 1 on page 2 is equivalent to $\overline{(A \cdot C)} \cdot (A + B + C)$ and draw a CMOS circuit for this given expression.

Note: Question No. 1 continues on page 2.

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(iii) Explain if the circuit drawn based on the Boolean expression in part (a) (ii) is better than the circuit shown in Figure 1.

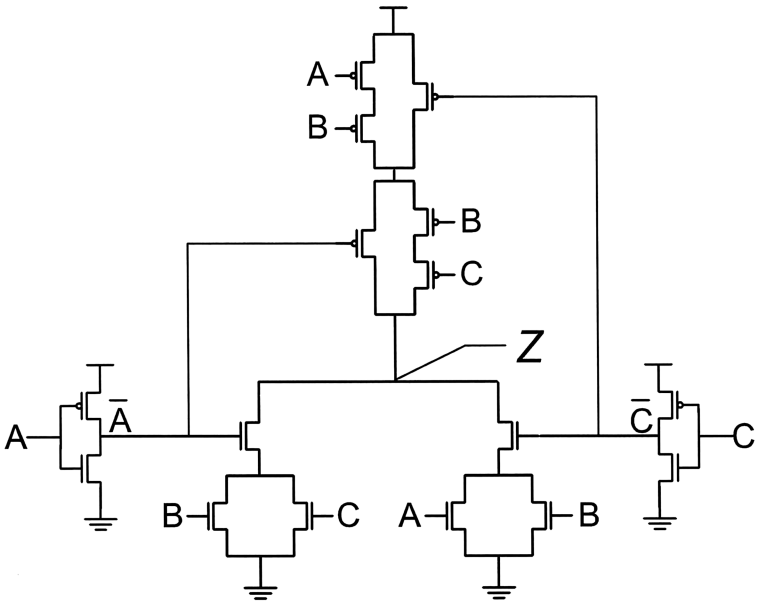

Figure 1

(10 Marks)

Note: Question No. 1 continues on page 3.

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(b) The process flow of a self-aligned silicide process for a MOSFET is shown in Figure 2.

(i) State the key advantage of using metal silicide on MOSFET.

(ii) List two popular metal silicides.

(iii) What does it mean by self-aligned silicide?

(iv) What is the purpose of using sidewall spacer?

(v) Briefly describe each of the process steps shown in Figure 2.

(10 Marks)

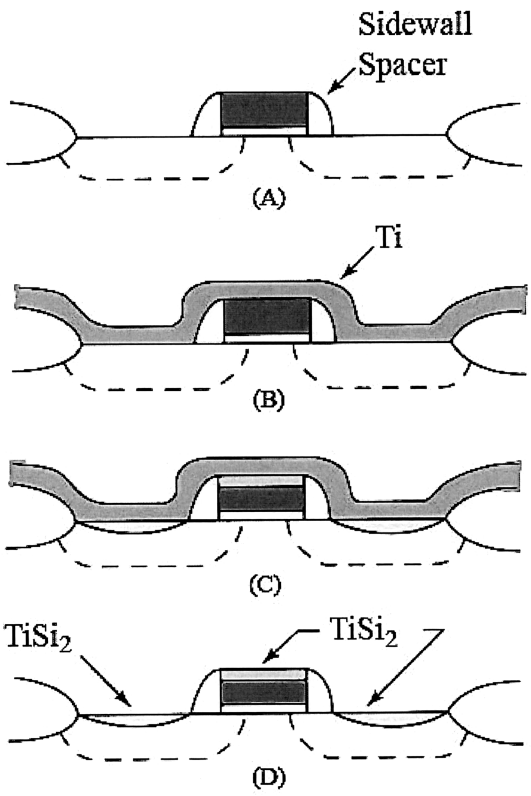

Figure 2

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2. (a) (i) Briefly describe the hot carrier effects and name the process module commonly used for controlling the hot carrier effects.

(ii) For a simple n-channel MOSFET with a gate oxide thickness less than 150 Å and gate length less than 0.5 μm, the peak electric field can be approximated using the following equation.

$$E_{\max} \approx \frac{V_{ds} - \dfrac{E_{sat} L (V_{gs} - V_t)}{V_{gs} - V_t + E_{sat} L}}{1.7 \times 10^{-2} t_{ox}^{1/8} x_j^{1/3} L^{1/5}}$$

where E_{sat} is the critical electric field for velocity saturation (~40 kV/cm), L is the gate length, V_{ds} is the drain-to-source voltage, V_{gs} is the gate-to-source voltage, V_t is the threshold voltage, t_{ox} is the gate oxide thickness and x_j is the junction depth.

Given an n-channel MOSFET with $L = 0.5$ μm, $t_{ox} = 125$ Å, $x_j = 0.2$ μm, and $V_t = 0.7$ V. Assume $V_{gs} = V_{ds}/2$, calculate the maximum electric fields when $V_{ds} = 5$ V and $V_{ds} = 3.3$ V.

State two consequences of velocity saturation and explain briefly how V_{ds} can be increased.

(12 Marks)

(b) Given the BiCMOS inverter gate in Figure 3, modify it to obtain a BiCMOS circuit for the function $F = \overline{A \cdot (B + C + D) + E}$. Note that no simplification of the function is required. State if your circuit permits rail-to-rail voltage swings.

(8 Marks)

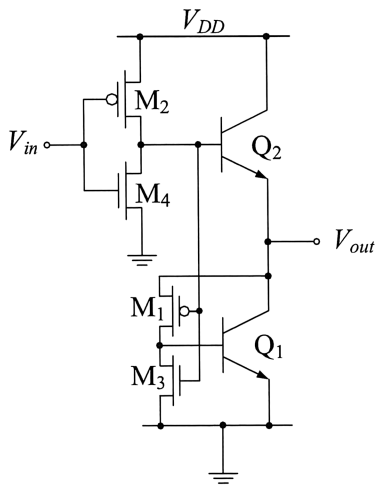

Figure 3

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3. (a) Given the following Boolean expression:

$$Y = A + \overline{B} \cdot (C\overline{D} + E)$$

Implement the function Y in Differential Cascode Voltage Switch Logic (DCVSL) through transistor-level circuit with minimum number of transistors. Determine the $\left(\frac{W}{L}\right)$ ratios of the transistors in the Pull-down Network (PDN) such that the driving capability of the PDN is equal to the inverter designed for the worst-case scenario. Assume that the $\left(\frac{W}{L}\right)$ ratio of the NMOS transistor for the inverter is $\left(\frac{3}{1}\right)$. List the advantages of DCVSL logic circuit over static CMOS logic circuit.

(10 Marks)

(b) A 4-stage pipeline circuit consists of 4 combinational logic blocks. It is assumed that the propagating delays of the various stages are 1T, 1.2T, 1.3T and nT ps respectively, where $1.5 < n < 2.5$.

(i) Show your design of the pipeline datapath using a block diagram.

(ii) Determine the clock period of the non-pipelined and pipelined datapaths.

(iii) If the throughput of the pipelined datapath is 2.75× of the non-pipelined datapath, determine n.

(iv) Show an alternative design to improve the throughput of the pipelined datapath and determine the throughput of this improved design.

(10 Marks)

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4. (a) Figure 4 shows part of a digital circuit with an n-bit input $x_{n-1}x_{n-2} \ldots x_3x_2x_1x_0$, a 3-bit input $z_4z_2z_1$, and an n-bit output $y_{n-1}y_{n-2}\ldots y_3y_2y_1y_0$.

(i) Analyze the circuit and explain its operation when $z_4z_2z_1 = 010$.

(ii) Identify the function of the circuit.

(iii) What are its advantages compared to other circuits with similar functions?

(8 Marks)

(b) Testing is an important step in manufacture of digital integrated circuits.

(i) Explain the importance of testing.

(ii) State the test categories and give each of them a brief explanation.

(12 Marks)

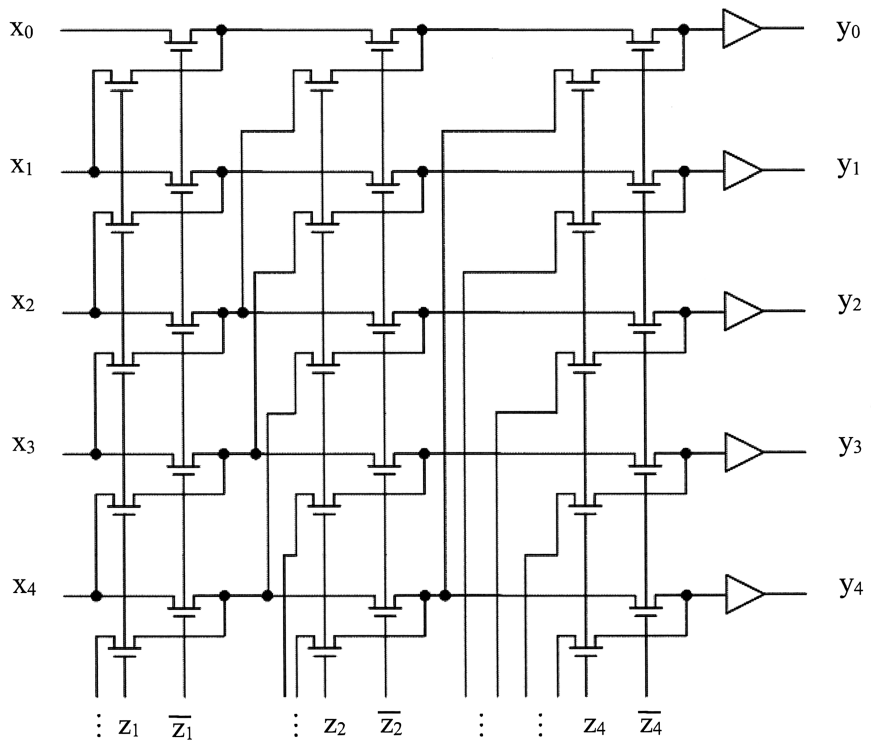

Figure 4

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5. (a) In digital integrated circuits, the adder is usually a performance-critical component.

(i) Carry-bypass technique can be used to improve the speed of an adder. Draw a 4-bit carry-bypass circuit with clear signal labels and definitions. Use the diagram to explain how this technique improves the speed performance.

(ii) Using the circuit in part (a) (i) as one stage, draw a block diagram of a 16-bit carry-bypass adder. Label clearly the function of each block, as well as inputs and outputs.

(12 Marks)

(b) Logic synthesis is a key aspect of design synthesis. Explain what logic synthesis is and outline its objectives. Briefly describe the main stages involved in the logic synthesis process.

(8 Marks)

END OF PAPER

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EE6306 DIGITAL INTEGRATED CIRCUIT DESIGN

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3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.

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