NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2022-2023

EE6306 – DIGITAL INTEGRATED CIRCUIT DESIGN

November / December 2022 Time Allowed: 3 hours

INSTRUCTIONS

1. This paper contains 5 questions and comprises 6 pages.
2. Answer all 5 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.

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1. (a) The stick diagram of a 5-input logic gate based on an n-well CMOS process is given in Figure 1.

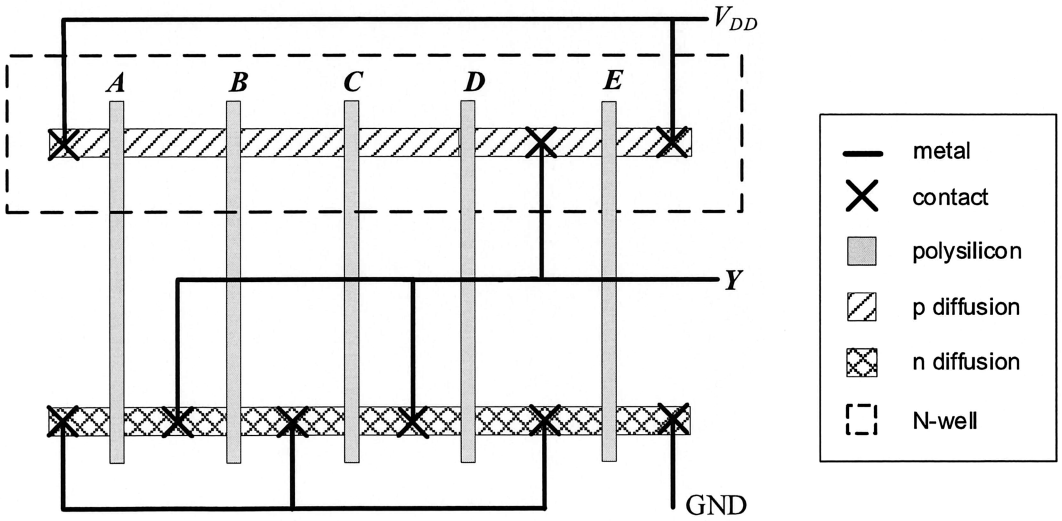

Figure 1

Note: Question No. 1 continues on page 2.

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(i) Sketch the transistor-level schematic of the logic gate of Figure 1 (on page 1) and deduce the logic function of the gate.

(ii) From the stick diagram of Figure 1 on page 1, calculate the minimum area of the logic gate using the following simplified λ-based design rules:

- Metal and diffusion have a width and spacing of 4λ.
- Contacts are 2λ×2λ with a metal overlap of 1λ.
- Polysilicon has a width of 2λ and a spacing of 1λ from diffusion.
- Polysilicon overlaps diffusion by 2λ at a transistor position.
- Polysilicon and contacts have a spacing of 3λ from other polysilicon and contacts.
- N-well surrounds pMOS transistors by 6λ and is 6λ from nMOS transistors.

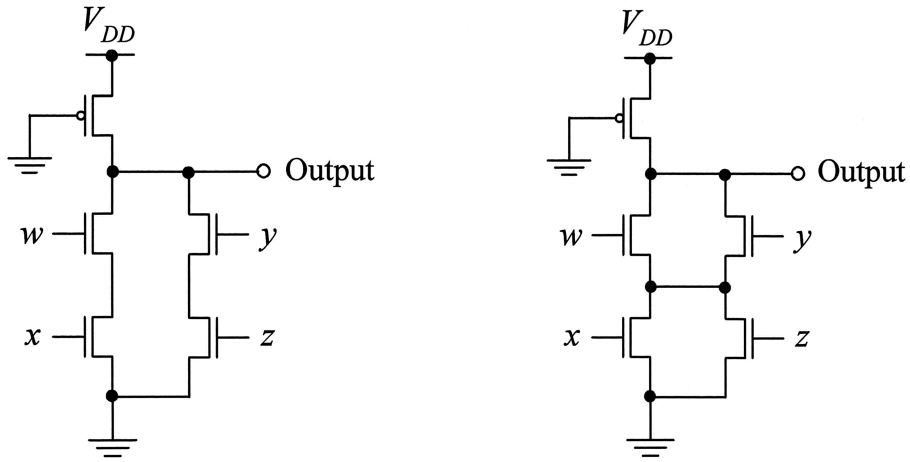
(10 Marks)

(b) With the aid of a diagram, describe the latchup phenomenon. Briefly explain how an electrostatic discharge event can cause latchup on a CMOS chip and how latchup can be prevented.

(6 Marks)

(c) Given the two circuits of Figure 2, state which circuit will operate faster in terms of switching speed and explain your choice of answer.

(4 Marks)



Circuit 2(a) **Circuit 2(b)**

Figure 2

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2. In a 0.18-μm process, the nMOS transistor was designed to have the parameters shown in Table 1.

Table 1

Transistor Parameter	Value
Channel length of nMOS, L	0.4 μm
Channel width of nMOS, W	1.2 μm
Gate oxide thickness	80 Å
Doping level, N_A	7×10^{16} cm^{-3}
Intrinsic carrier concentration, n_i	1.5×10^{10} cm^{-3}
Substrate bias voltage between source and body, V_{sb}	2.5 V
Threshold voltage without body bias ($V_{sb} = 0$), V_{th0}	0.65 V
Gain factor, β	300 μA/V^2
Thermal voltage, v_T	25.9 mV
Dielectric constant of SiO_2, ε_{ox}	$3.9\varepsilon_o$
Dielectric constant of Si, ε_{Si}	$11.7\varepsilon_o$
Permittivity of free space, ε_o	8.854×10^{-14} F/cm
Electronic charge, q	1.6×10^{-19} C

(a) Calculate the gate capacitance of the nMOS transistor.

(3 Marks)

(b) The threshold voltages of MOS transistor with and without body bias are defined as V_{th} and V_{th0}, respectively. Given below is the equation of V_{th}. Calculate V_{th} for an nMOS transistor based on the parameters provided in Table 1.

$$V_{th} = V_{th0} + \gamma\left(\sqrt{\varphi_s + V_{sb}} - \sqrt{\varphi_s}\right)$$

where surface potential, $\varphi_s = 2v_T \, ln\left(\frac{N_A}{n_i}\right)$

and the body effect coefficient, $\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{ox}}$

(5 Marks)

Note: Question No. 2 continues on page 4.

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(c) Calculate the drain current I_{ds} of the nMOS transistor for the following biasing conditions:

(i) $V_{gs} = V_{ds} = 2.5$ V.

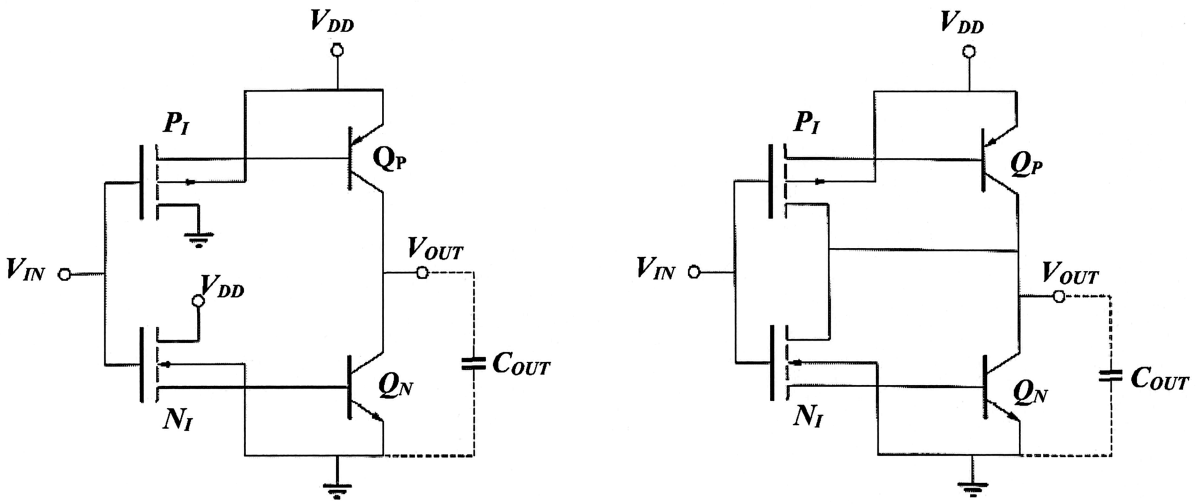
(ii) $V_{gs} = 5$ V and $V_{ds} = 2.5$ V.

(iii) $V_{gs} = 0.5$ V and $V_{ds} = 3$ V.

(6 Marks)

(d) Shown in Figure 3 are two basic BiCMOS drivers. These circuits have their own merit(s) and limitation(s) in terms of speed, power dissipation and output swing. Comment on these performance metrics for each circuit.

(6 Marks)



Circuit 3(a) **Circuit 3(b)**

Figure 3

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3. (a) Derive the Boolean expression for the 4-to-1 multiplexer circuit shown in Figure 4. The function table of the multiplexer is given in Table 2.

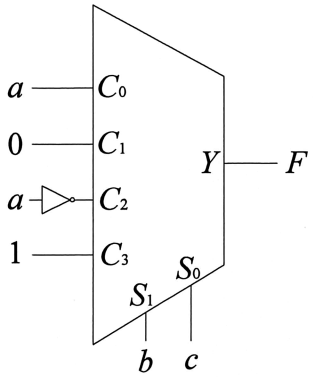

Figure 4

Table 2

Input		Output
S_1	S_0	Y
0	0	C_0
0	1	C_1
1	0	C_2
1	1	C_3

Implement the same logic function in Pass Transistor Logic (PTL) and in Pseudo nMOS Complex logic transistor level circuit with minimum number of transistors. Briefly describe the advantages and disadvantages of PTL logic circuit compared to Pseudo nMOS logic circuit.

(12 Marks)

(b) A pipelined design can generally increase the throughput considerably. The propagation delays of the 4 combinational logic blocks in a datapath are 27ns, 36ns, 28ns and 15ns, respectively, assuming that the delay associated with the latches and flip-flops are negligible and ignoring clock skew. Determine the data throughput improvement and the pipeline clock frequency when the 4-stage pipelined design is implemented. Suggest a method to increase the pipeline clock frequency and discuss the additional overhead(s) incurred in the new design. State any assumption made.

(8 Marks)

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4. The carry chain delay in an adder is the main factor that limits the speed of the adder. Carry-select technique can be used to reduce the carry chain delay and improve the performance.

(a) With the aid of a block diagram, explain how the carry-select technique reduces the carry chain delay.

(4 Marks)

(b) Draw a 16-bit 4-stage linear carry-select adder. Label clearly the blocks as well as the inputs and outputs of each block.

(6 Marks)

(c) Explain how the carry chain delay of the linear carry-select adder can be further reduced.

(4 Marks)

(d) Draw a 14-bit square-root carry-select adder. Label clearly the blocks as well as the inputs and outputs of each block.

(6 Marks)

5. (a) With the aid of a block diagram, explain briefly how the scan-based test technique is used in testing of digital integrated circuits, including a brief description of the test procedure.

(10 Marks)

(b) The retiming technique (also known as register balancing) is used to optimize logic circuit performance during logic synthesis. State a circuit performance factor that can be optimized by the retiming technique and explain briefly how the performance is improved with the aid of logic block diagrams.

(10 Marks)

END OF PAPER

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EE6306 DIGITAL INTEGRATED CIRCUIT DESIGN

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1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.

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