Digital Logic Circuits

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Course Outline:

- Number systems and codes.
- Logic gates
- Boolean algebra, postulates, theorems and algebraic functions
- Representation and simplification of logic functions using AND-OR
- SOP and POS , Minterms, Maxterms
- K-maps, NAND-NAND, NOR- NOR
- Design of digital circuits, BCD, Adder circuits (HA, FA), 4-bit Binary Adder
- Design using decoders and multiplexers
- Flip-flops, T FF, D FF, JK FF and sequential circuit design and analysis
- Register, shift register, universal shift register
- 3-bit counter, binary ripple counter, binary down counter, ring and BCD counter
- Memory and PLD components.

Textbook: "Digital Design: With an Introduction to the Verilog HDL" M. M. Mano & M.D. Ciletti, Pearson Prentice-Hall, 5th edition (International Edition). ISBN-13: 978-8131794746

Grading Scheme:

Homework	15%
Midterm	35%
Final/Project	50%

Tests would be closed book and closed notes. Material covered will be discussed in the class. Only calculators (simple scientific calculators). Smart phones will not be allowed and should be placed in your book bags.

EAC Outcomes and Student Learning Objectives:

Outcome 3b: an ability to design and conduct experiments, as well as to analyze and interpret data

SLO-1: conduct an experiment to learn the logic design and prototyping process in order to acquire requisite hands-on skills and report the results through a well-defined and formatted written document.

SLO-2: document the data acquired from an experiment, compare to the expected theoretical values and discuss any differences.

SLO #5: Students will be able to design an experiment to validate through empirical means one of the following: a hypothesis, a Boolean logic law or identity, dependency among variables, etc. Students will also be able to conduct the experiment designed, measure quantities of interest, collect and compile data, interpret the results and make engineering inferences.

Outcome 3c: an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.

SLO-3: design a digital module with combinational and sequential logic components to be able to address any problem in the applicable domain and report the results in a typical engineering design document.

SLO-4: build a prototype of a digital logic circuit and demonstrate that it meets performance specifications, which are limited to functional correctness and resource minimization; i.e., minimal product-of-sums or sum-of-products only for combinational design only.

SLO-5: document the data acquired from an experiment, compare to the expected theoretical values and discuss any differences.

Outcome 3g: an ability to communicate effectively

SLO-6: write an effective technical report for lab experiments.

Outcome 3k: an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

SLO-7: Use state-of-the-art combinational and sequential logic design methodologies, techniques, and paradigms.

SLO-8: Use tools including a scope and a logic analyzer to prototype, debug and test a combinational and sequential logic circuit at the gate level utilizing the MSI/LSI technology

SLO-9: Use online resources to obtain current literature on engineering components.

Instructor's Policies

You must have required prerequisite for this course. Hand in homework just before the class on the due date. A grade of zero will be assigned for a late work. Makeup tests will not be given. If a student is not able to take the test for a valid reason (communicated before the test.), the course grade will be assigned based on the available data. Do your own homework. Copied "group solutions" will receive no credit. Students are responsible for being familiar with the contents of the College of Engineering Dishonesty Policy. Any form of dishonesty will require an automatic "0" for the associated work for the first offense. You will get a grade of "F" on the second offense. No, "drops" or "incompletes" will be assigned to avoid a failing grade in the course. It is the student's responsibility to drop the course before the deadline published in the course catalog. Requests for re-grading must be received no later than one week following the return of the assignment in the class.

Please review "missed class policy" and dishonesty policy available at BUCT website.