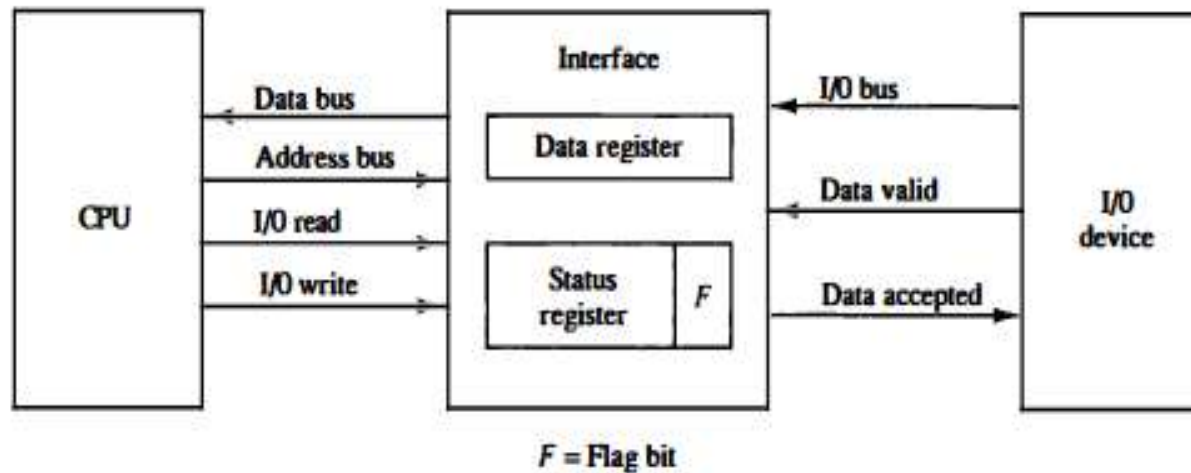# Modes of Transfer

■ Data transfer between the CPU and the I/O devices may be handled in variety of modes. Some modes use the CPU as an intermediate path and others transfer the data directly to and from the memory unit.

■ Data transfer to and from peripherals may be handled in three ways:

◆ Programmed I/O

◆ Interrupt-initiated I/O

◆ Direct Memory Access (DMA)

Programmed I/O

- Programmed I/O operations are the result of I/O instructions. Each data item transfer is initiate by an instruction in the program.

- Usually the transfer is to and from a CPU register and peripheral. Other instructions are needed to transfer data between memory and CPU.

- Once a data transfer is initiated, the CPU is required to monitor the interface to see when a transfer can again be made.

Programmed I/O

Figure 11-10   Data transfer from I/O device to CPU.

CPU		Interface		I/O device

Data bus

Address bus

I/O read

I/O write

Data register

Status register F

I/O bus

Data valid

Data accepted

F = Flag bit

Interrupt Initiated I/O

- In the programmed I/O CPU stays in program loop until the I/O indicates that it is ready for data transfer.

- This is time consuming process since it makes CPU busy needlessly.

- This can be avoided by using an interrupt facility.

- When the interface determines that device is ready for data transfer, it generates an interrupt request.

- Upon detecting external interrupt signal, the CPU momentarily stops the task it is processing.

- It then branches to fulfill the I/O request and return to the original task.

Direct Memory Access (DMA)

- The transfer of data between a fast storage device such as magnetic disk and memory often limited to the speed of CPU.

- Removing the CPU and letting the peripheral device manage the memory bus directly improve speed of transfer.

- Such transfer technique is called Direct Memory Access (DMA).

- A DMA controller takes over the buses to manage the transfer directly between I/O device and memory.

- During DMA transfer, the CPU is idle and has no control over memory buses.

- By using **Bus Request(BR)** and **Bus Grant(BG)** the buses are released to DMA controller.
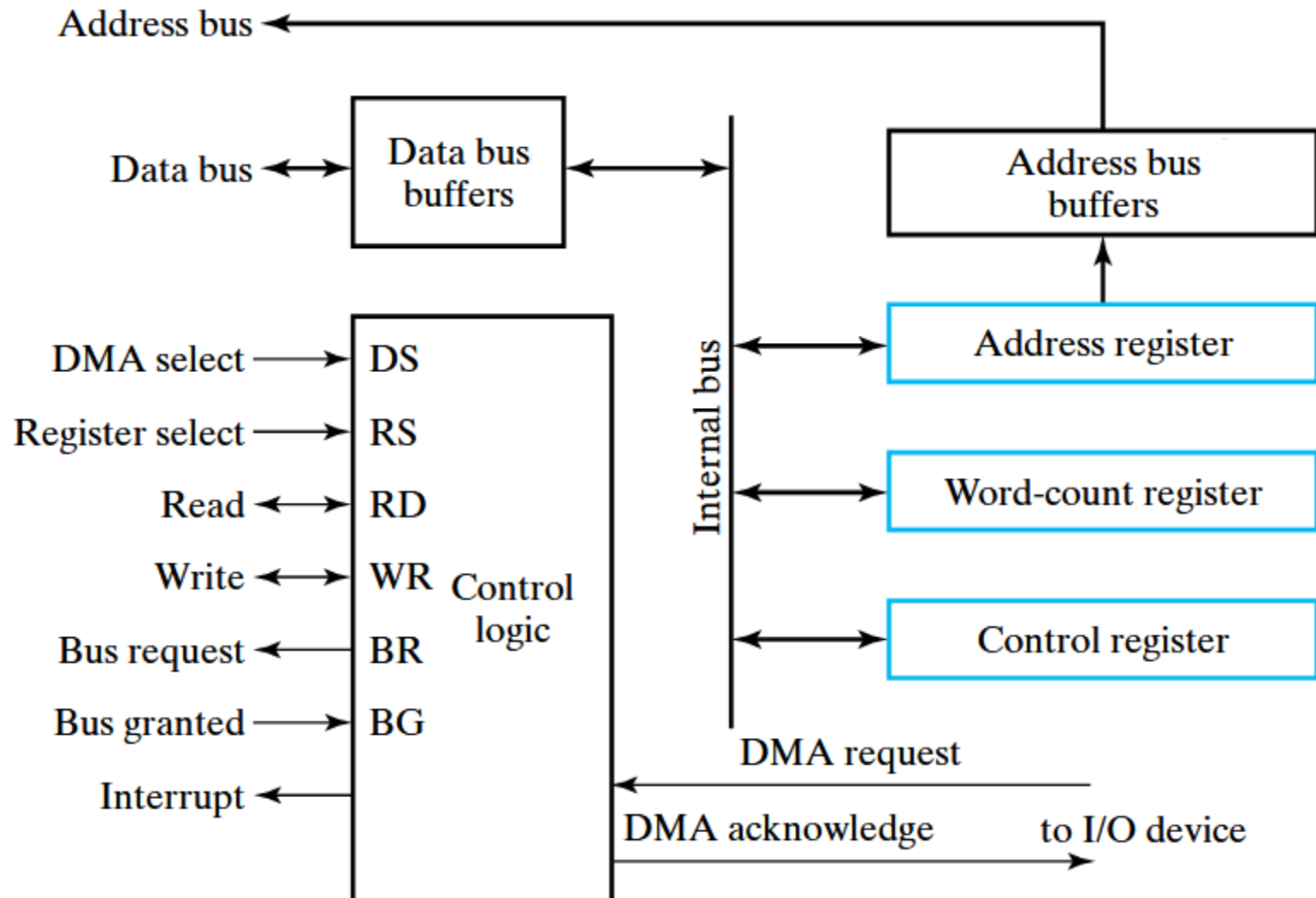
DMA

Figure 6.13 CPU bus signals for DMA transfer.
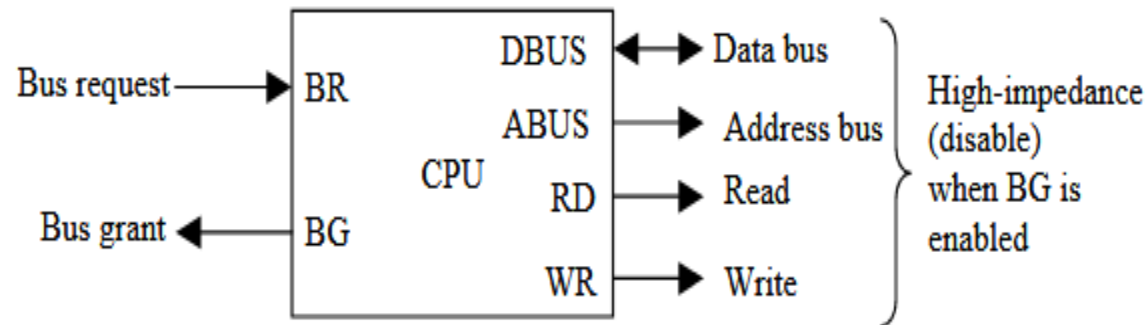
- Data transfer ways:

  ◆ Burst Transfer: Here number of words are transferred in a block. Example: Magnetic disk.

  ◆ Cycle stealing: Allows the DMA controller to transfer one data word at a time after it must return the control of buses to CPU.

DMA Controller

Initialization of DMA

■ The CPU initializes the DMA by sending the following information through the data bus.

◆ The starting address of the memory block where data are available(for read) or where data are to be stored(for write).

◆ The word count, which is the number of words in the memory block.

◆ Control to specify the mode of transfer such as read or write.

◆ A control to start the DMA transfer.

DMA Transfer in a computer system