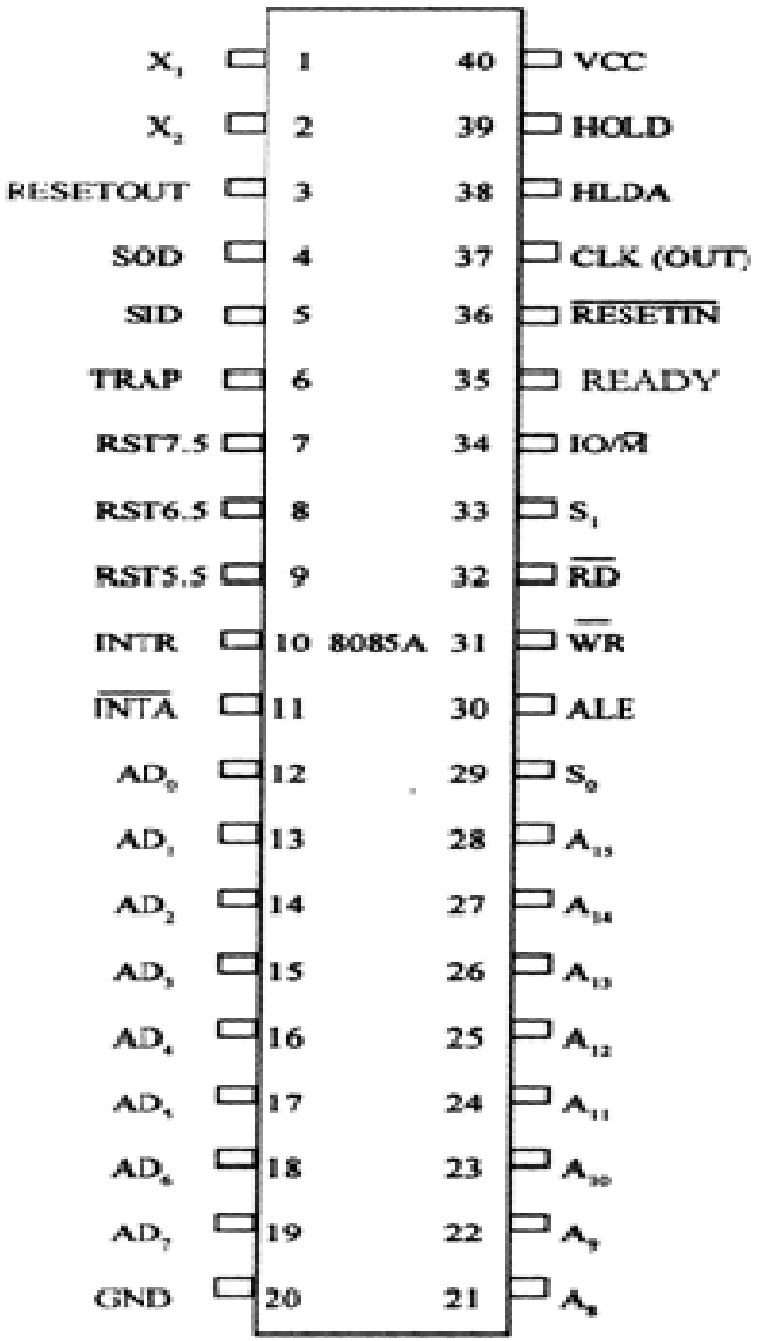
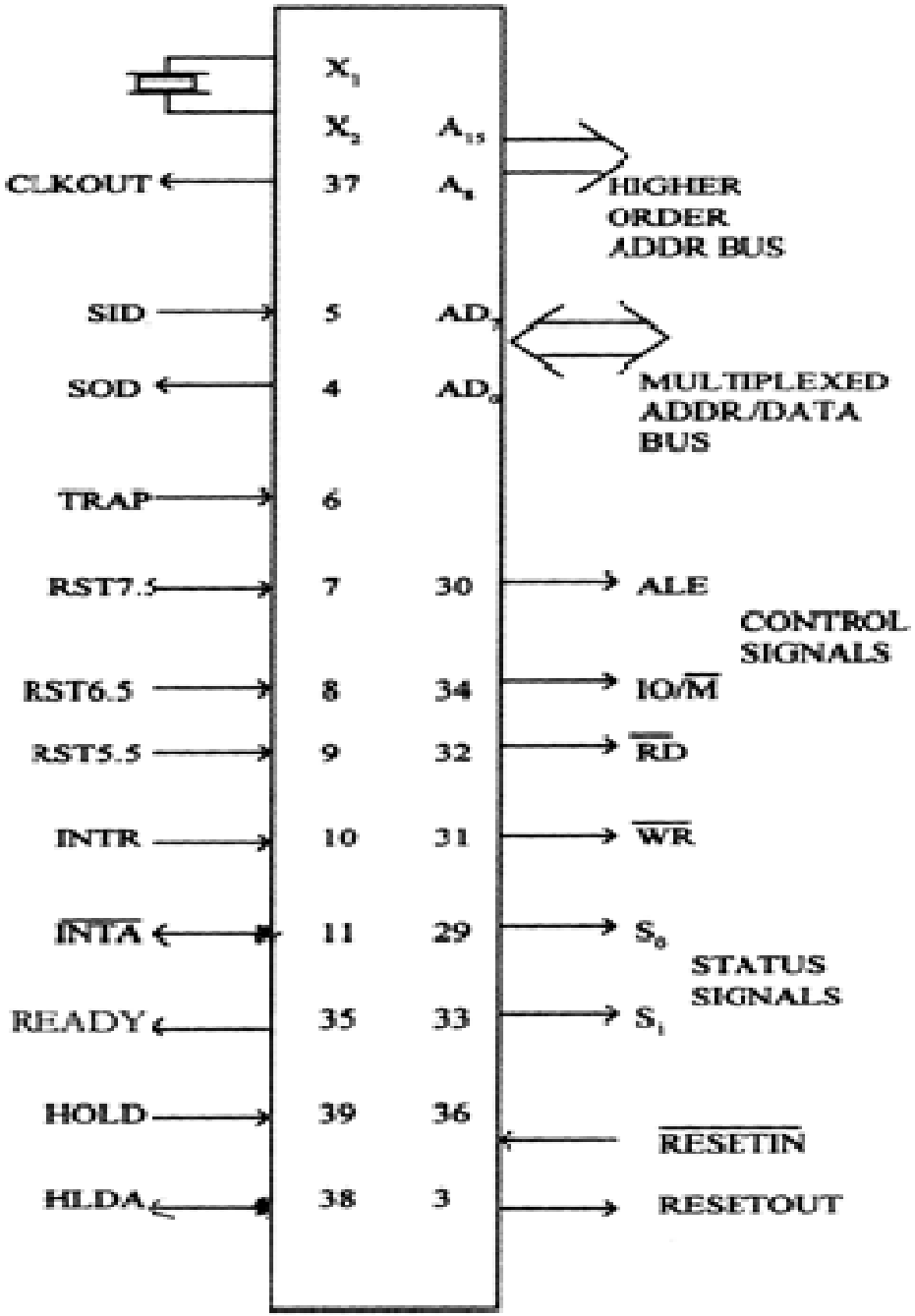
Pin Configuration of 8085

- *It has 40 pins and uses +5V power supply. It can run at a maximum frequency of 3 MHz.*
  - *The pins on the chip can be grouped into 6 groups:*
    - *Address Bus.*
    - *Data Bus.*
    - *Control and Status Signals.*
    - *Power supply and frequency.*
    - *Externally Initiated Signals.*
    - *Serial I/O ports.*

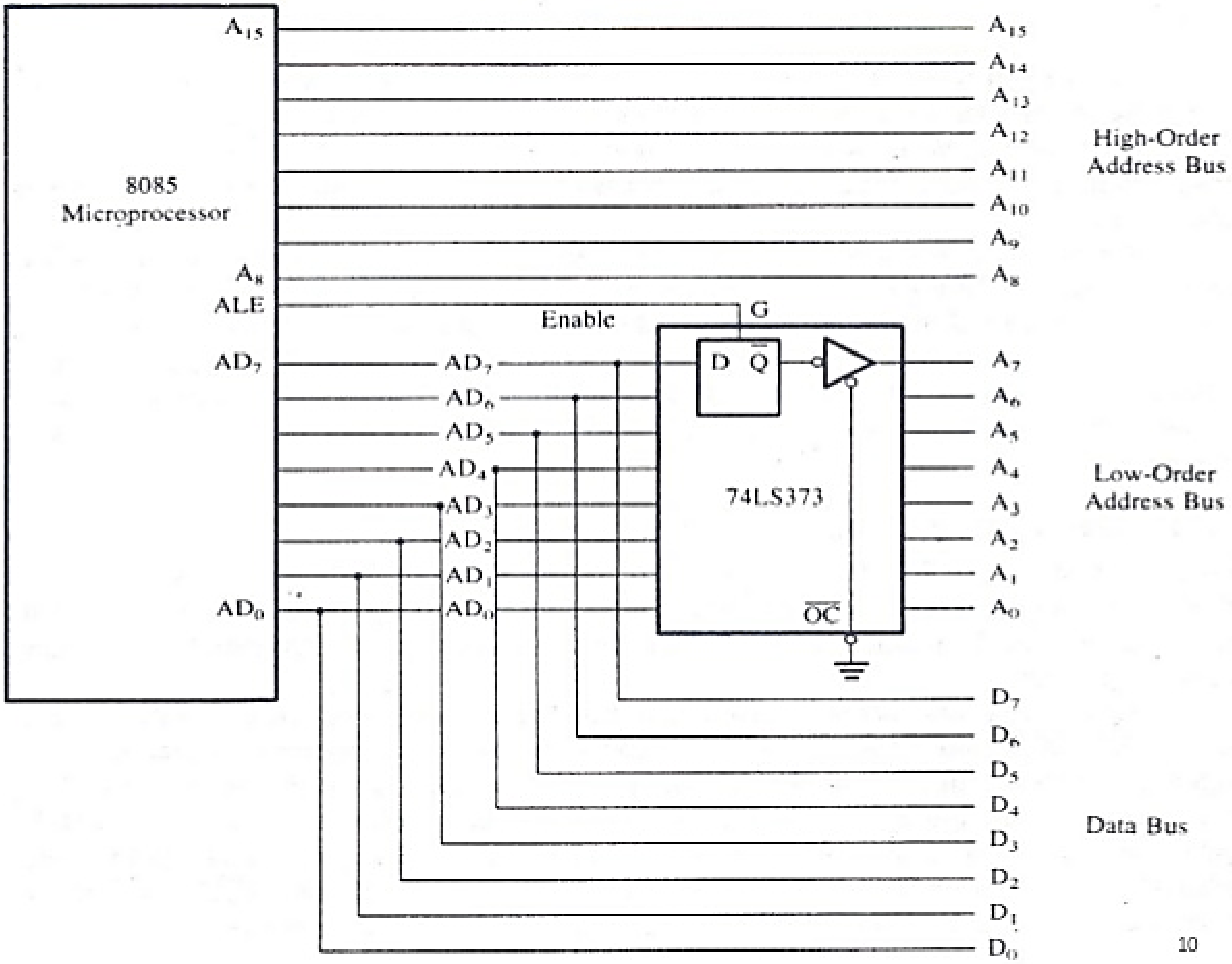

X1 1
X2 2
RESETOUT 3
SOD 4
SID 5
TRAP 6
RST7.5 7
RST6.5 8
RST5.5 9
INTR 10
INTA 11
AD0 12
AD1 13
AD2 14
AD3 15
AD4 16
AD5 17
AD6 18
AD7 19
GND 20
8085A
40 VCC
39 HOLD
38 HLDA
37 CLK (OUT)
36 RESETIN
35 READY
34 IO/M
33 S1
32 RD
31 WR
30 ALE
29 S0
28 A15
27 A14
26 A13
25 A12
24 A11
23 A10
22 A9
21 A8

8085 Pinout


X1
X2
CLKOUT
37
A15
A8
HIGHER ORDER ADDR BUS
SID
5
AD7
AD0
SOD
4
MULTIPLEXED ADDR/DATA BUS
TRAP
6
RST7.5
7
30
ALE
CONTROL SIGNALS
RST6.5
8
34
IO/M
RST5.5
9
32
RD
INTR
10
31
WR
INTA
11
29
S0
STATUS SIGNALS
READY
35
33
S1
HOLD
39
36
RESETIN
HLDA
38
3
RESETOUT

The Address and Data Busses

- The address bus has 8 signal lines A8 – A15 which are unidirectional.
- The other 8 address bits are multiplexed (time shared) with the 8 data bits.
  - So, the bits AD0 – AD7 are bi-directional and serve as A0 – A7 and D0 – D7 at the same time.
    - During the execution of the instruction, these lines carry the address bits during the first clock cycle, and in the subsequent clock cycles of the execution, they carry the 8 data bits.
  - In order to separate the address from the data, we can use a latch to save the value before the function of the bits changes.


8085
Microprocessor
A15
A8
ALE
AD7
AD0
Enable
G
D Q
74LS373
OC
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
High-Order
Address Bus
Low-Order
Address Bus
Data Bus

Power Supply & Clock Frequency Signals

Vcc : ***+ 5 volt power supply***

Vss : ***Ground***

–X0 and X1 are the inputs from the crystal or clock generating circuit.

•The frequency is internally divided by 2.

–So, to run the microprocessor at 3 MHz, a clock running at 6 MHz should be connected to the X0 and X1 pins.

–CLK (OUT): CLK (output)-Clock Output is used as the system clock for peripheral and devices interfaced with the microprocessor.

The Control and Status Signals

- There are 3 control and 3 status signals. These are:
  - ALE: Address Latch Enable. This signal is a pulse that become 1 when the AD0 – AD7 lines have an address on them. It becomes 0 after that. This signal can be used to enable a latch to save the address bits from the AD lines.
  - $\overline{RD}$: Read. Active low indicates that the data must be read from the selected memory location or I/O port via data bus.
  - $\overline{WR}$: Write. Active low indicates that the data must be written into the selected memory location or I/O port via data bus..
  - IO/$\overline{M}$: This signal specifies whether the operation is a memory operation (IO/$\overline{M}$=0) or an I/O operation (IO/$\overline{M}$=1).
  - S1 and S0 : Status signals to specify the kind of operation being performed .

IO/$\overline{M}$, S1 & S0

Operations	IO/$\overline{M}$	S_0	S_1
Opcode Fetch	0	1	1
Memory Read	0	1	0
Memory Write	0	0	1
I/O Read	1	1	0
I/O Write	1	0	1
Interrupt Ack.	1	1	1
Halt	High Impedance	0	0

Externally Initiated Signals

- ***RESET IN − This signal is used to reset the microprocessor by setting the program counter to zero.***
- ***RESET OUT − This signal is used to reset all the connected devices when the microprocessor is reset.***
- ***READY − This signal indicates that the device(slow peripheral) is ready to send or receive data. If READY is low, then the CPU has to wait for READY to go high.***
- ***HOLD − This signal indicates that DMA controller is requesting the use of the address and data buses.***
- ***HLDA (HOLD Acknowledge) − It indicates that the CPU has received the HOLD request and it will relinquish the bus in the next clock cycle. HLDA is set to low after the HOLD signal is removed.***