Module – A
The 8085 Microprocessor

8085

MICROPROCESSOR ARCHITECTURE & PIN CONFIGURATION

Addressing Modes

Register Organization

Instruction Set

Types of operations

8085 Microprocessor

- It is an 8-bit microprocessor designed by Intel in 1977 using NMOS technology.
- 8085 uses a single +5-volt(V) power supply.
- The 8085 is supplied in a 40-pin DIP package.
- Address up to 64k locations.(consist 16 Address lines)
- Word Size-: 8 bits (It can process 8 bits at a time.(consist 8 data lines)
- It can run at a maximum frequency of 3 MHz.

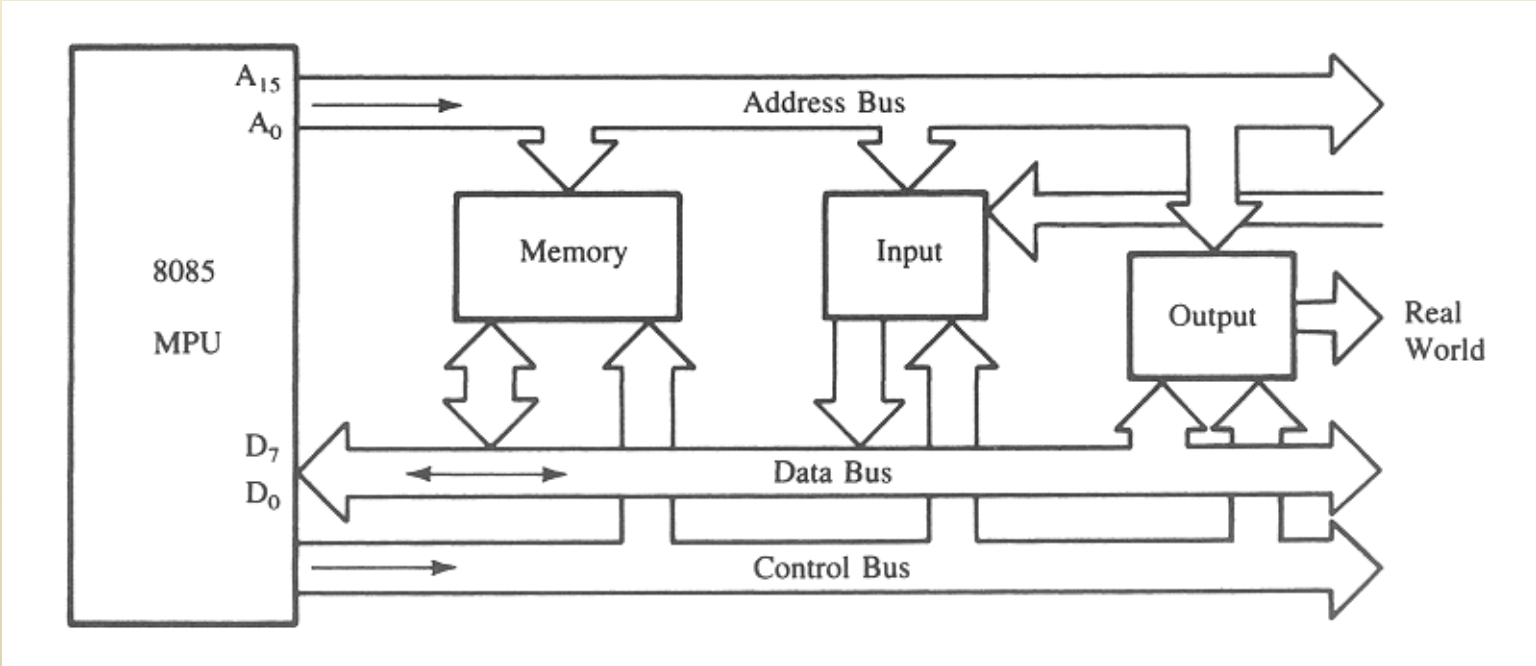
The 8085: CPU Internal Structure

The internal architecture of the 8085 CPU is capable of performing the following operations:

- *Store 8-bit data (Registers, Accumulator)*
- *Perform arithmetic and logic operations (ALU)*
- *Test for conditions (IF / THEN)*
- *Sequence the execution of instructions*
- *Store temporary data in RAM during execution*

The 8085 Bus Structure

The 8-bit 8085 CPU (or MPU – Micro Processing Unit) communicates with the other units using a 16-bit address bus, an 8-bit data bus and a control bus.



The 8085 Bus Structure

Address Bus

- Consists of 16 address lines: $A_0 - A_{15}$
- Operates in unidirectional mode: The address bits are always sent from the MPU to peripheral devices, not reverse.
- 16 address lines are capable of addressing a total of 2^{16} = 65,536 (64k) memory locations.
- Address locations: 0000 (hex) – FFFF (hex)

The 8085 Bus Structure

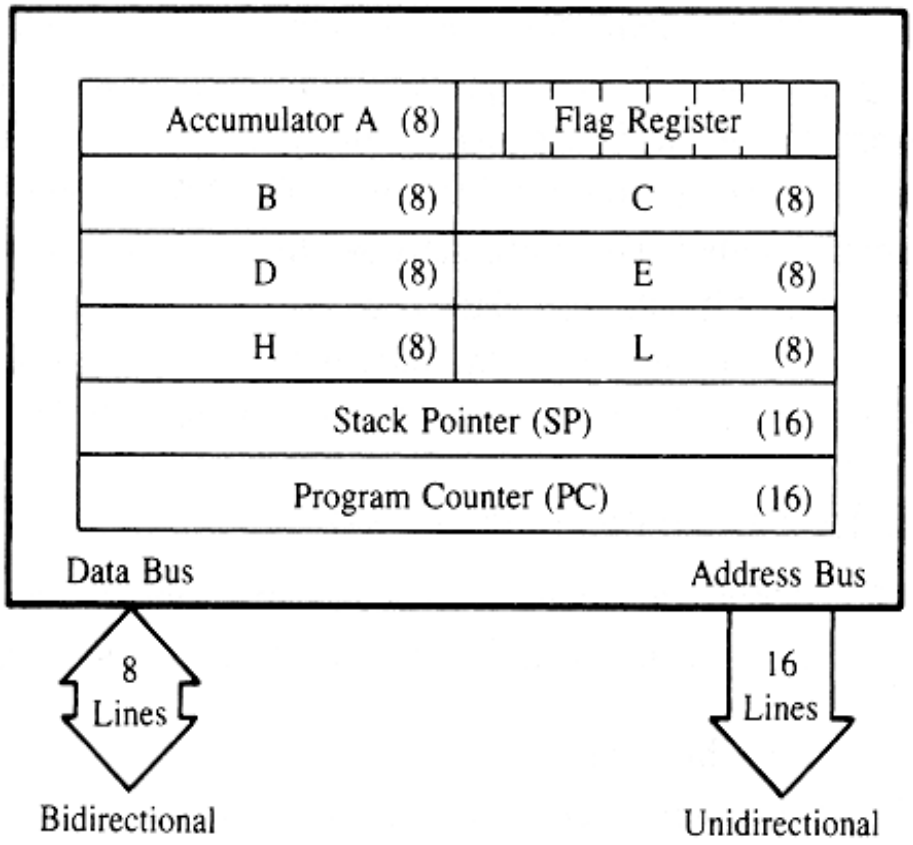
Data Bus

- Consists of 8 data lines: $D_0 – D_7$
- Operates in bidirectional mode: The data bits are sent from the MPU to peripheral devices, as well as from the peripheral devices to the MPU.
- Data range: 00 (hex) – FF (hex)

Control Bus

- Consists of various lines carrying the control signals such as read / write enable, flag bits.

Registers



- ***General purpose Registers***
- ***Temporary Registers***
- ***Special Purpose Register***
- ***16 Bit Registers***

The 8085: CPU Internal Structure

Registers

- Six general purpose 8-bit registers: B, C, D, E, H, L
- They can also be combined as register pairs to perform 16-bit operations: BC, DE, HL
- Registers are programmable (data load, move, etc.)

Accumulator

- Single 8-bit register that is part of the ALU !
- Used for arithmetic / logic operations – the result is always stored in the accumulator.

The Flags register

S	Z		AC		P		CY

- *Indicate the result of condition tests.*
- *Conditional operations (IF / THEN) are executed based on the condition of these flag bits.*

- ***S-sign flag***
  - ***The sign flag is set if bit D7 of the accumulator is set after an arithmetic or logic operation.***
- ***Z-zero flag***
  - ***Set if the result of the ALU operation is 0. Otherwise is reset.***
- ***AC-Auxiliary Carry***
  - ***This flag is set when a carry is generated from bit D3 and passed to D4 . This flag is used only internally for BCD operations.***
- ***P-Parity flag***
  - ***After an ALU operation if the result has an even no of 1's the p-flag is set. Otherwise it is cleared. So, the flag can be used to indicate even parity.***
- ***CY-carry flag***
  - ***CY = carry is set when result generates a carry. Also a borrow flag.***

Question

If the 8085 adds 87H and 79H, specify the contents of the accumulator and the status of the S, Z, and CY flag?

PROGRAM COUNTER (PC) AND STACK POINTER (SP)

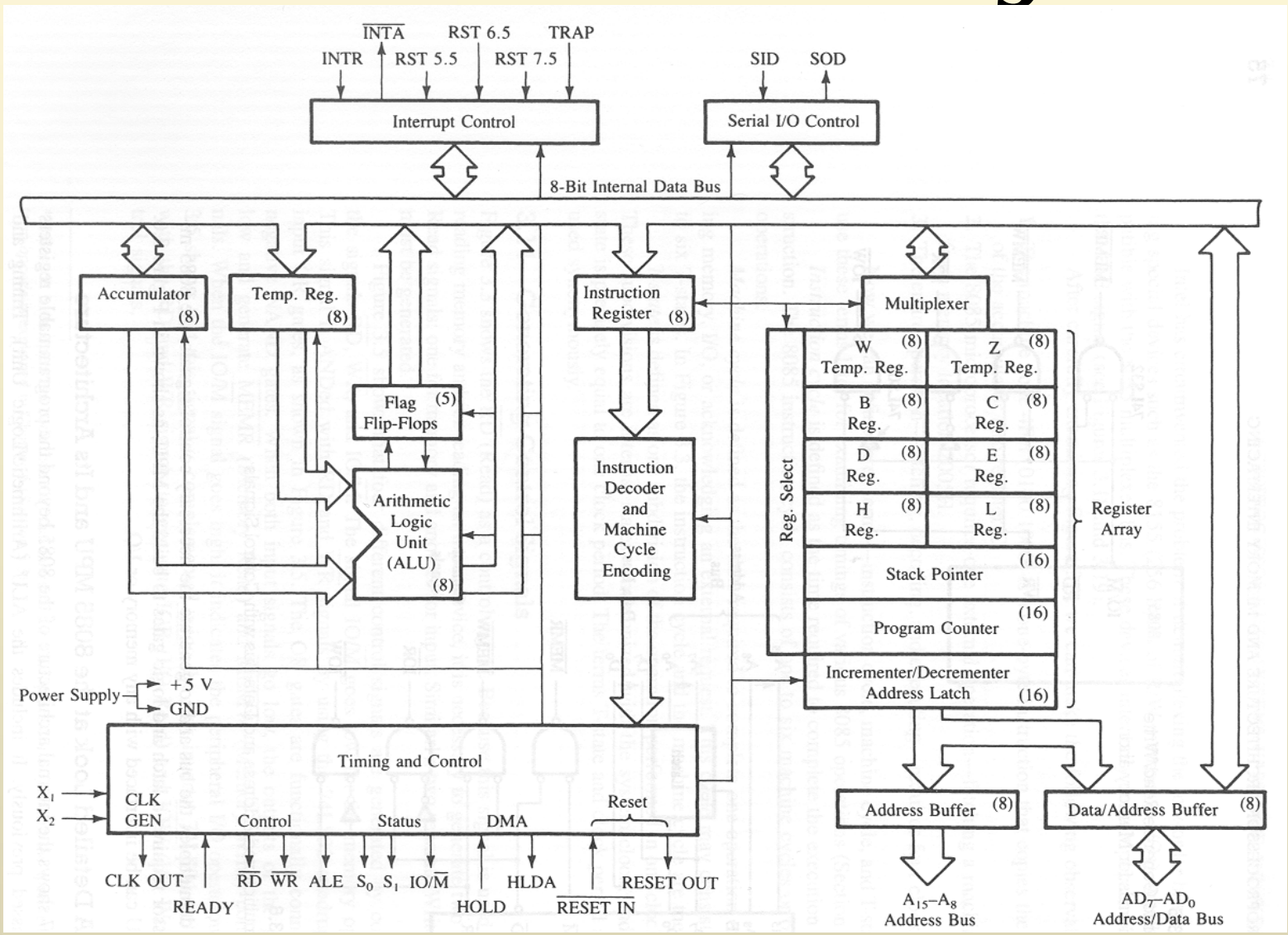
- **These are two 16-bit registers used to hold memory addresses.**
- **PC: Used to sequence the execution of instructions.**
  - **The function of the PC is to point to the memory address from which the next byte of the instruction is to be fetched.**
  - **When a byte (machine code) is being fetched, the program counter is incremented by one to point to the next memory location.**
- **SP:**
  - **It points to a memory location in R/W memory, called the stack.**
  - **The beginning of the stack is defined by loading a 16-bit address in the stack pointer.**
  - **The PC will automatically update when calling to /returning from Subroutines.**

The ALU

- ***In addition to the arithmetic & logic circuits, the ALU includes the accumulator, which is part of every arithmetic & logic operation.***

- ***Also, the ALU includes a temporary register used for holding data temporarily during the execution of the operation. This temporary register is not accessible by the programmer.***

8085 Functional Block Diagram



Functional Blocks

- ***Registers***
- ***ALU***
- ***Instruction Decoder***
- ***Address Buffer***
- ***Address/Data Buffer***
- ***Increment/ Decrement Address Latch***
- ***Serial I/O Control***
- ***Timing and control circuitry***
- ***Interrupt Control***

Instruction Decoder

- *This accepts a bit pattern from instruction register, decode it and gives the decoded information to control logic unit.*
- *It contains:*
  - *What operation to be performed?*
  - *Who will perform this?*
  - *How many bytes the instruction contains?*

Address Buffer/ Data Buffer

Address buffer:

- This is an 8 bits unidirectional buffer used for address lines.
- These are used to drive higher order address bus.

Address/ Data buffer:

- This is an 8 bits bidirectional buffer used for address and data lines.
- These are used to drive low order address and Data bus.

Increment/ decrement Address Latch

- *16 bits Register*
- *Used to increment and decrement address contents of PC, HL, BC, DE and SP.*

Serial IO

- The data transferred on data bus is parallel data but certain condition required serial data.
- 8085 uses SID and SOD pins for data under software control by serial I/O block.

Timing & Control Unit

- *Control all internal and external circuits.*
- *Operates with reference to clock signal.*
- *Accepts information from instruction decoder and generates micro steps.*
- *Synchronizes all data transfers.*

Interrupt Control

- Interrupts are the signals generated by external devices to request the microprocessor to perform a task. There are 5 interrupt signals: TRAP, RST 5.5, RST 6.5, RST 7.5 and INTR.

- Inform control logic to take action for valid interrupt request and acknowledge by INTA signal.

- Software Interrupt :RST0-RST7
- Hardware Interrupt: TRAP, RST 5.5, RST 6.5, RST 7.5 and INTR.