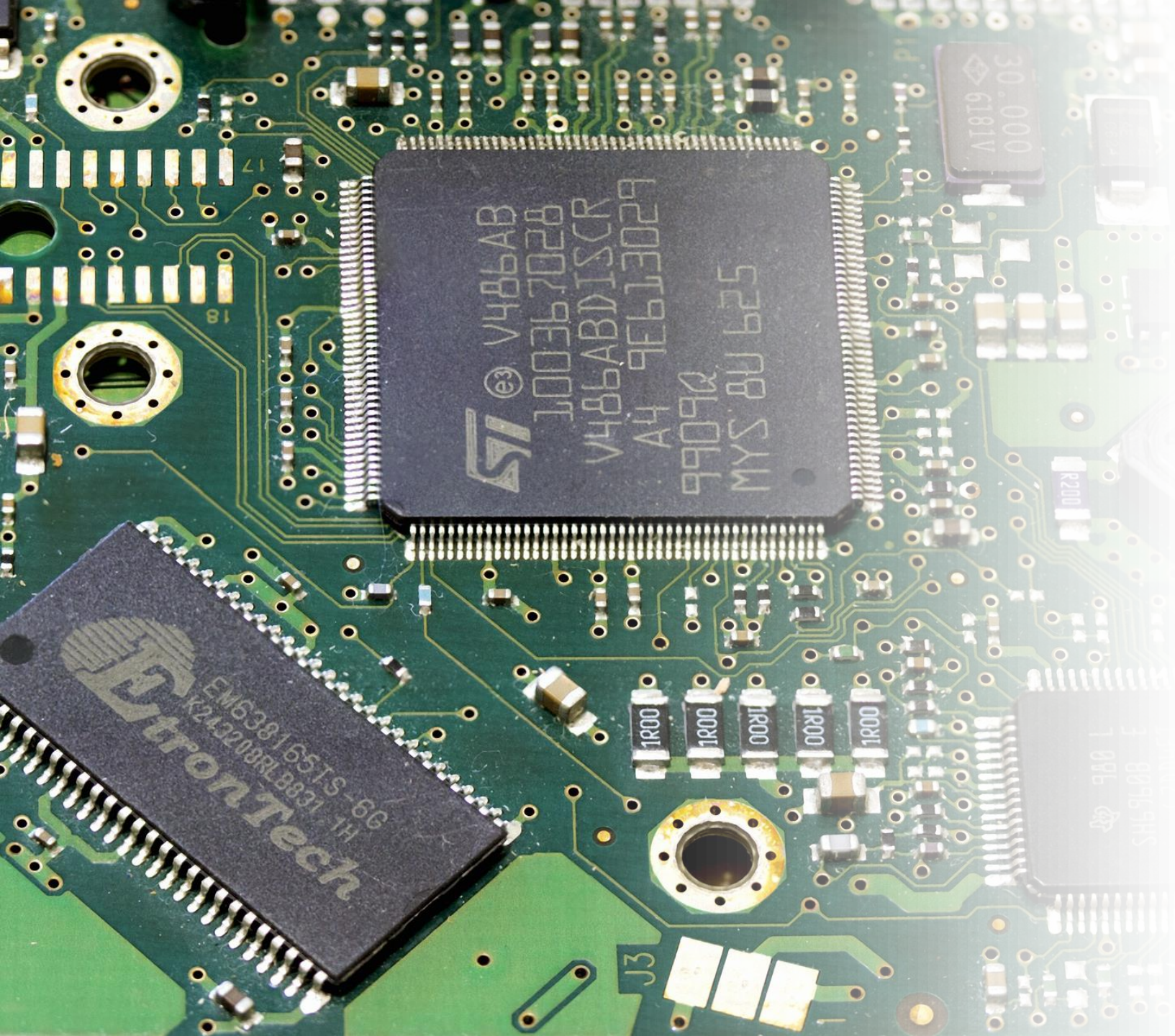

Digital Logic and System Design

10. Test & Validation

COL215, I Semester 2023-2024
Venue: LHC 111
'E' Slot: Tue, Wed, Fri 10:00-11:00

Instructor: Preeti Ranjan Panda
panda@cse.iitd.ac.in
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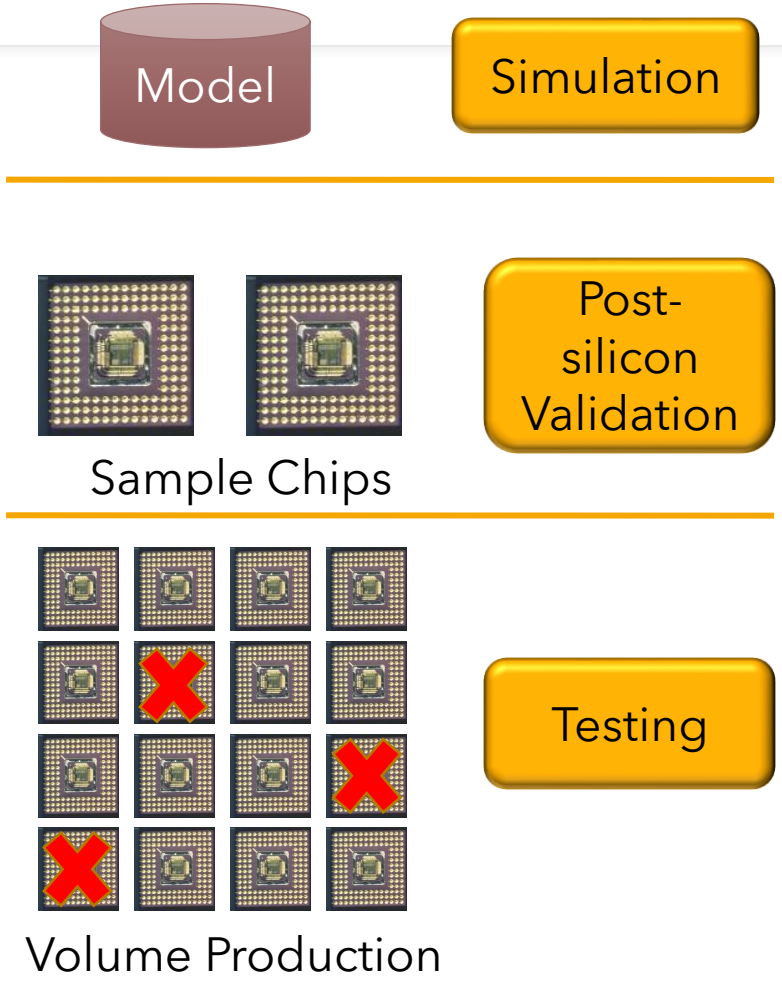
Dept. of Computer Science & Engg., IIT Delhi

Chip Verification Phases

- Simulation
  - On software model of chip
  - Different abstraction levels
  - Slow: small sub-system tests
- Post-silicon Validation
  - Validating sample chips in lab
  - Logical and Electrical Problems
  - Fast: real usage scenarios
- Testing
  - Manufacturing failures
  - Fast, but not much time per chip
  - Good/Bad decisions only

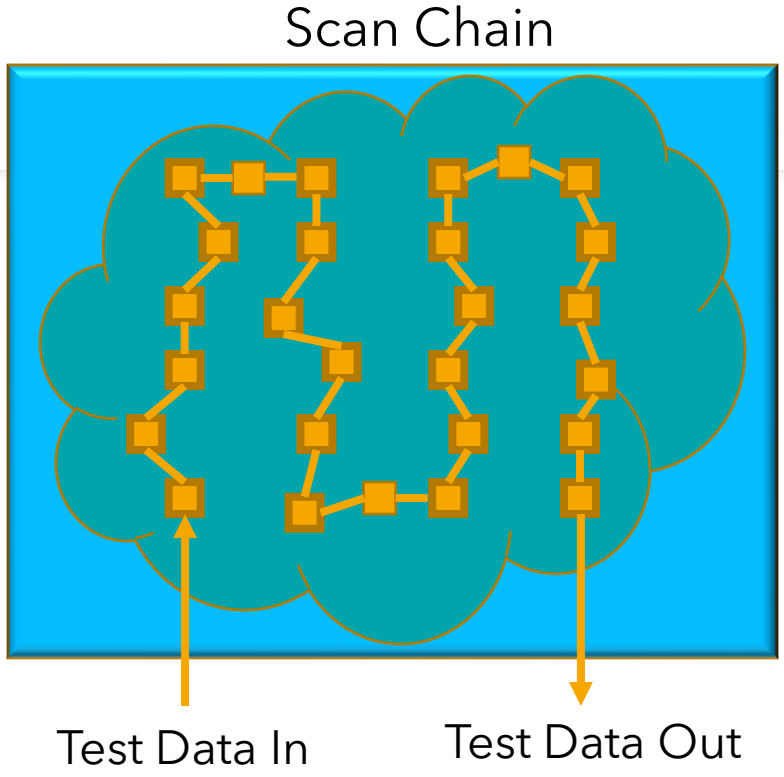


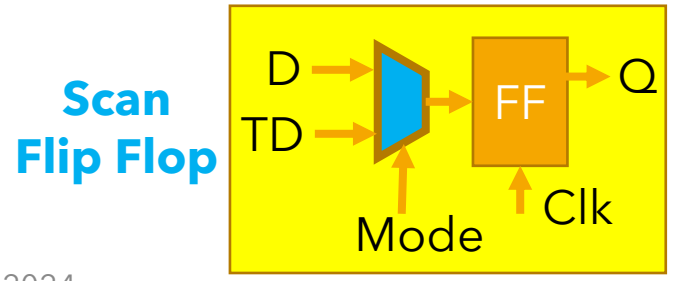
What if Bug is Found?

- If SEVERE (doesn't allow other validation to proceed)
  - RE-SPIN (Expensive!)
- If workaround exists (in software, etc.)
  - Proceed with other validation
- New revision only if certain threshold of bugs is crossed

How to test a chip?

- Examine internal memory (too large!)
- Collect all important memory elements (**flip flops**)
- Hook them together into a long chain
- Replace normal Flip Flop by **Scan Flip Flop**
  - Design-for-Test feature
  - Note: we are changing the original design!





Scan Chain

- NORMAL mode:
  - Disable chain
  - Execute
- TEST mode:
  - Enable chain
  - Send data IN/OUT