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| **Started on** | Saturday, 20 November 2021, 5:30 PM |
| **State** | Finished |
| **Completed on** | Saturday, 20 November 2021, 8:07 PM |
| **Time taken** | 2 hours 37 mins |
| **Grade** | **0.00** out of 100.00 |

**Question 1**

Complete

Not graded

Please carefully read the following statement: "I confirm that during this exam, I will neither give any help to other students nor receive any help from other students. I understand that providing or receiving an answer in this exam is academic misconduct for which I could be penalized as per the decision of the course instructor." Do you agree with this statement?

Select one:

- Yes (I agree with the above statement and would like to continue with this exam.)
- No (I do not agree with the above statement and would like to skip this exam.)

Your answer is correct.

The correct answer is: Yes (I agree with the above statement and would like to continue with this exam.)

**Question 2**

Not answered

Marked out of 8.00

Use Quine McCluskey method to minimize the following 5-variable function.

$Y = f(a,b,c,d,e) = \sum m(2, 3, 6, 19) + \sum d(7, 15, 23, 31)$

**Question 3**

Not answered

Marked out of 12.00

You need to design a 2-bit counter that counts in the sequence (2, 0, 1, 3) and raises a flag (i.e., outputs a bit 1) whenever the counter completes one cycle.

1. Draw the corresponding state diagram and state table. (4 Marks)
2. Derive the expression for the next states and the output considering that you can use only T flip-flops. (6 Marks)
3. Draw the circuit. (2 Marks)

**Question 4**

Not answered

Marked out of 8.00

Design a combinational module named EQ-COMP that takes two 2-bit numbers ($A_0$-$A_1$ and $B_0$-$B_1$) as inputs and generate an output – **eq** (equal).

**Question 5**

Not answered

Marked out of 7.00

Introduce another input **pre_eq** (all previous bits equal) and design a module named CASCADE-EQ-COMP to make the module cascadable for larger word lengths.

**Question 6**

Not answered

Marked out of 8.00

Write a VHDL behavioral description of the module CASCADE-EQ-COMP.

**Question 7**

Not answered

Marked out of 27.00

1. Write a VHDL structural description of a component named EQ-COMP16 that compares two 16-bit binary numbers to declare whether they are equal or not. Use CASCADE-EQ-COMP as a component. (12 Marks)
2. Assume a memory that stores 512 16-bit Integers. We need to count how many values are “0” in this list (Hex value 0000H). Write a VHDL description of a process to do that. Assume the needed components exist in the work library but clearly declare their interface through component declaration. (15 Marks)

**Question 8**

Not answered

Marked out of 12.00

Based on the Process described in the previous question, draw a state machine to implement the controller.

**Question 9**

Not answered

Marked out of 8.00

Map CASCADE-EQ-COMP to FPGA with 3-input LUTs. Show the number of LUTs required and the logic they implement.

**Question 10**

Not answered

Marked out of 10.00

Explain why the configuration bit file size depends only on the FPGA device on which the circuit is being implemented and is independent of the size and complexity of the circuit itself. (Max 100 words)

◄ Minor Exam Set-1 Solutions

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