Started on	Friday, 29 October 2021, 10:10 AM
State	Finished
Completed on	Friday, 29 October 2021, 10:14 AM
Time taken	4 mins 52 secs
Marks	1.00/1.00
Grade	**10.00** out of 10.00 (**100**%)

Question 1

Correct

Mark 1.00 out of 1.00

Consider the following VHDL description of an AND_OR gate:

```
entity AND_OR is
  port(a, b, c: in bit;
            y: out bit);
end AND_OR;
architecture beh of AND_OR is
signal d: bit;
begin
  d <= a AND b after 2 ns;
  y <= d OR c after 1 ns;
end beh;
```

Assume at time *t* = 0 ns, all input signals (*a*, *b*, and *c*) are "0" and simultaneously all change to "1" at 5 ns.

At what time, *y* would change to "1"?

Select one:

- 6 ns ✓
- 5 ns
- 8 ns
- between 5 ns and 6 ns
- None of the given options

Your answer is correct.

The correct answer is: 6 ns