2102-COL216 Quiz 3

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TOTAL POINTS

7 / 10

QUESTION 1

1 Read-Access Time 3 / 4

+ **0 pts** unattempted/incorrect
✓ + **1 pts** **Best Case**
✓ + **2 pts** **Worst Case**
+ **1 pts** Precise

QUESTION 2

2 Interrupts 0 / 2

✓ + **0 pts** **Incorrect**
+ **0 pts** Incomplete/Unattempted
+ **2 pts** Correct

QUESTION 3

3 Bus Transfer 4 / 4

✓ + **4 pts** **Correct**
+ **1 pts** Without brust transfer-with pipeline
+ **2 pts** With brust transfer- with pipeline
+ **1 pts** Ratio (with pipeline)
+ **0.5 pts** Without brust (without pipeline)
+ **1.5 pts** With brust (without pipeline)
+ **0.5 pts** Ratio (without pipeline)
+ **0 pts** Incorrect
+ **0 pts** Unattempted

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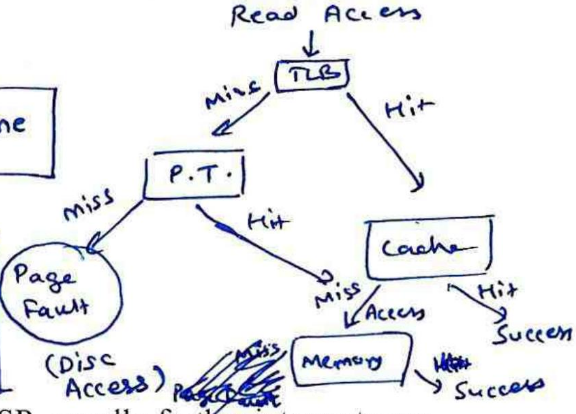
COL216 Computer Architecture **Quiz 3** **04.04.2022**

Note: Write answers in spaces provided, continue on reverse side if needed.

Note : Disc = Secondary Storage

Q 1. Consider a virtual memory system with the page table stored in physical memory. The system has one level physically addressed cache and a TLB. What would be the best case and worst-case timings for making a read access? Give answer in terms of access times of cache, TLB, main memory, secondary storage and any other relevant parameter.



Sol. BEST CASE : TLB Hit + Cache Hit

T_{best} = TLB Access Time + Cache Access Time

WORST CASE : TLB Miss + Page Table Miss

T_{worst} = TLB Access Time + Page Table Access Time + Disc Access Time

Q 2. In response to an interrupt, while transferring control to an ISR, usually further interrupts are disabled by the hardware. If the ISR wants to permit nested interrupts, it has to explicitly enable these. What could be the reason for this? Why not keep the interrupts enabled and leave these to be disabled by ISR if it does not want to permit nested interrupts?

Sol. Note that the interrupt service routine (ISR) is a function/routine which has been designed by the manufacturer. If the manufacterer intends for there to be nested interrupts, inside the ISR then the hardware can explicitly enable them. However, there can also be many unintentional interrupts like memory access interrupts, alignment exception, etc. If these nested interrupts occur inside the response to the interrupt, the response to these may interfere with response to the current interrupt and it may remain unresolved.

Also if same interrupt can be unintentionally raised in the ISR it could lead to an infinite loop/recursion.

Q 3. Consider a memory connected to a processor/cache through AMBA-Lite bus. The memory can supply the first word in 4 cycles and up to three subsequent words from consecutive addresses in one cycle each. Find the ratio of throughputs (words transferred per sec) for reading 16 word blocks using burst transfer and without burst transfer.

Sol. Without burst transfer

We would require 1 cycle for the address phase and 4 cycles for each of the words.

$\therefore$ Cycles reqd / word = 1+4 = 5

C_2 = Total no. of cycles = 5 X 16 = 80 cycles (for 16 words)

—— P.T.O ——

With Burst Transfer

With burst transfer, we require 1 cycle for the initial address phase 4 cycles for the 1st word and 1 for each of the other 3. So for each 4 word block we have,

$$\text{Cycles}/4 \text{ word block} = 1 + 4 + 3(1) = 8 \text{ cycles}.$$

$\therefore$ For 16 word blocks we would need

$$C_1 = \text{Total no. of cycles} = 8 \times 4 = 32 \text{ cycles}$$

$$\text{Ratio of throughputs} = \frac{C_2}{C_1} \quad (\text{No. of cycles ratio})$$

$$= \frac{80}{32} = \frac{5}{2} = 2.5$$

$\therefore$ For transfer with burst transfer we are able to get 2.5x throughput compared to without burst transfer.

NOTE: We have assumed that address phase takes 1 cycle for each word. If we pipeline the address phase then it would take only 1 cycle initially and would reduce the no. of cycles —

Without: Cycles / word = 4.

$$\therefore \text{No. of cycles } (C_2) = 1 + 4 \times 16 = 65$$

With: Cycles / 4 word block = 4 + 3 = 7

$$\therefore C_1 = 1 + 4 \times 7 = 29$$

$$\therefore \frac{C_2}{C_1} = \frac{65}{29} = 2.24$$ is the throughput ratio in this case.
