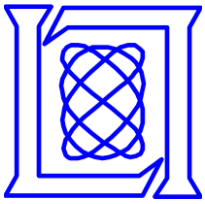
MIT LL 100 μA/μm^2 Superconductor Electronics Fabrication Process SFQ5eg

Design Guide

Revision 1.0 (Nov 2020)
Design Guide



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1. INTRODUCTION

About Revision 1

This document is Revision 1 of MIT Lincoln Laboratory's design guide intended for use by designers as a generic reference for MIT LL 100 µA/µm^2 fabrication processes. The currently offered SFQ3ee, SFQ4ee, and SFQ5ee processes differ in the number of superconducting layers, the minimum feature sizes, and other details given in the corresponding Design Rule documents. The present design guide is provided as an example SFQ process description that is based on the SFQ5ee process. However, it does not supersede and should not be viewed as a substitute for the currently active Design Rules for the MIT LL SFQ5ee Fabrication. Please contact Lincoln Laboratory for guidance if intending to prepare a chip design for fabrication in an actual technology.

About the SFQ5eg Process

This example MIT Lincoln Laboratory (MIT LL) fabrication process for superconductor electronics is a niobium-based integrated-circuit technology appropriate for RSFQ, RQL, ERSFQ, and other superconducting electronic circuits. It is based on Nb/Al-AlO_x/Nb tri-layer technology with a critical-current-density J_c of 100 µA/µm^2. It utilizes 248-nm photolithography and planarization with chemical-mechanical polishing (CMP) for wiring-layer feature sizes down to 350 nm and Josephson junction diameters down to 700 nm.

2. PROCESS GEOMETRY

Process Geometry Description

The MIT LL 100 μA/μm² SFQ5eg process cross section is given in Figure 1. The naming convention of the process is set according to the fabrication flow. There are nine superconducting layers: eight niobium wiring layers M0–M7 and one layer of high kinetic inductance (HKI) material, L0. There are two normal metal layers: layer R5 (Resistor) is for JJ shunting and available in either a standard or high-sheet-resistance (HSR) option, and layer M8 (Pad) is for chip contact metallization and chip packaging. Interconnects between all metal and resistor layers are formed by vias C0, C5, and I0–I7. All layer interconnects are etched vias filled with the niobium metal of the subsequent superconducting layer.

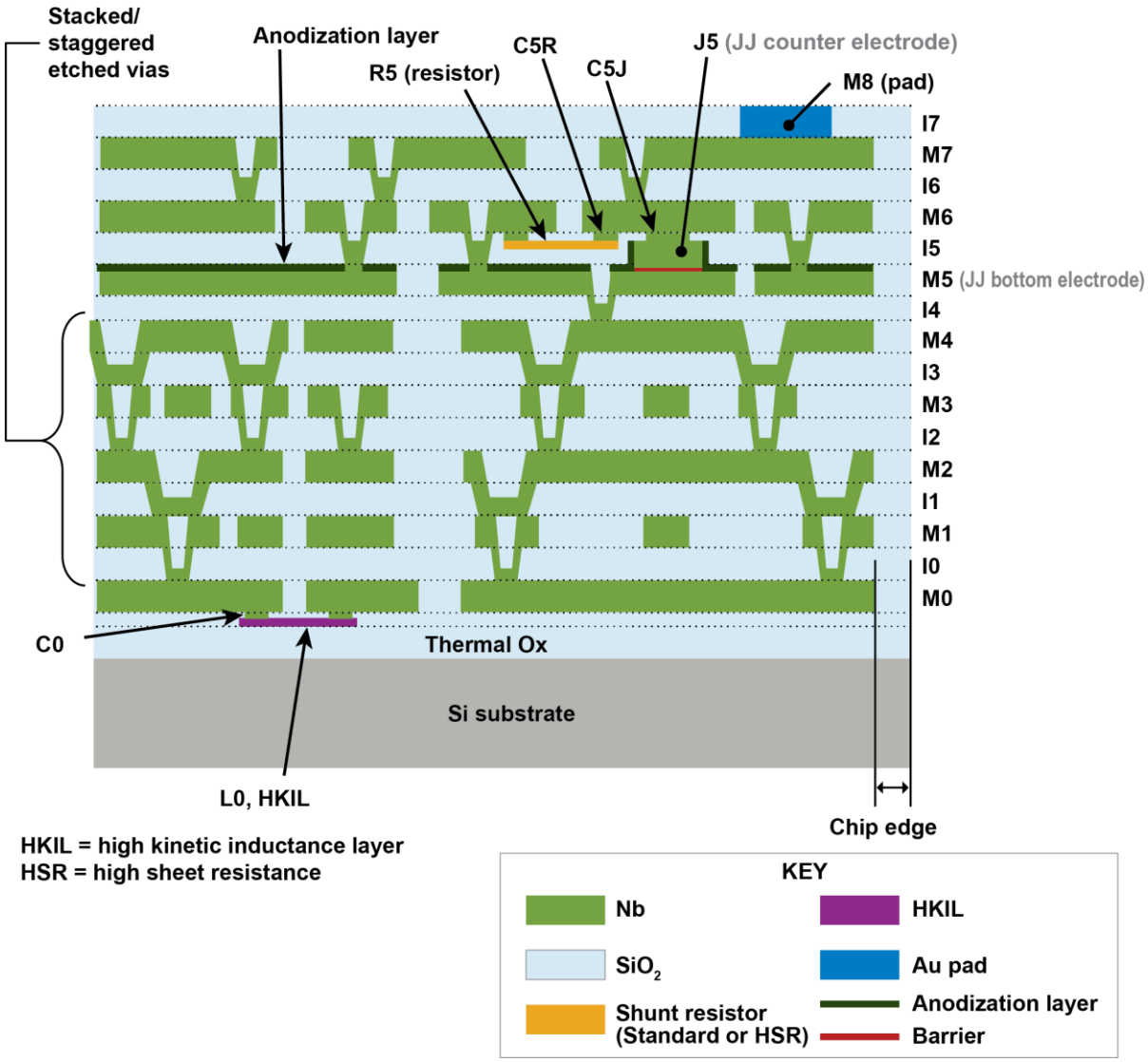

Figure 1. Cross section of the MIT LL 100 μA/μm² SFQ5eg process.

A cross section of the process layers near a Josephson junction is shown in Figure 2. Josephson junctions are formed between layers M5, the bottom electrode, and J5, the counter electrode. Wiring connections between counter electrodes are made on layer M6 with access to the counter electrodes through a contact via, C5J. The resistor layer R5 is placed beneath M6 for close proximity of shunting resistors to the JJs, and are accessed through contact vias C5R. Please note that resistor layer R5 is not planarized in the fabrication process.

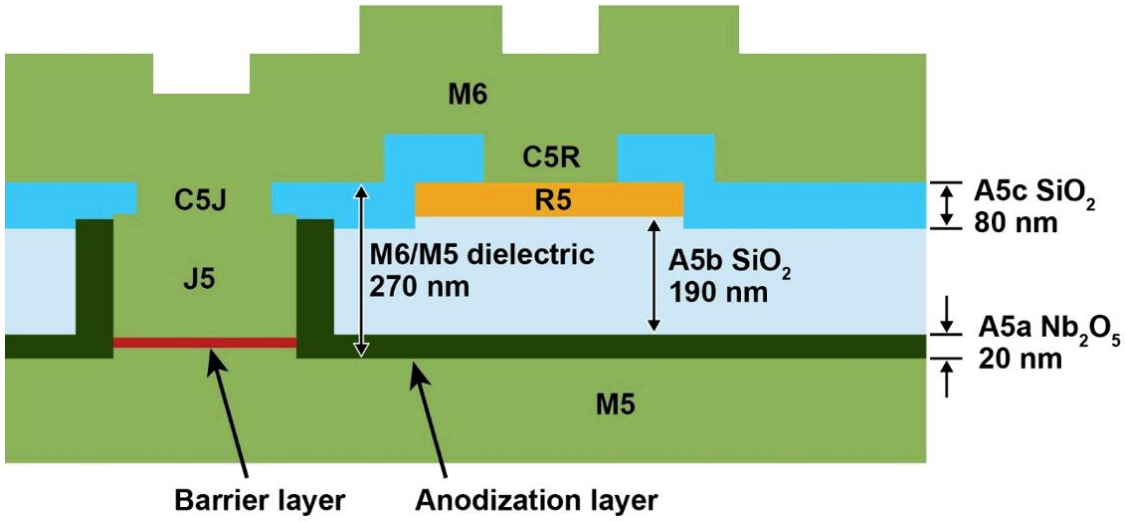

Figure 2. Cross section of the process layers near a Josephson junction, showing dielectric thicknesses of related layers.

Physical Layer Specifications

General Specifications

Specifications for both design and physical (superconducting, metal, and dielectric) layers are given Table 1 below, including materials, fabrication tolerances, thicknesses, and electrical properties. Design layers are drawn as part of circuit layout, and physical layers are formed during circuit fabrication.

Table 1. Specifications of Design and Physical Layers in the MIT LL 100 μA/μm² SFQ5eg

Layer Name	Material	Fabrication Tolerance (nm)	Thickness (nm)	Electrical Properties	Layer Type	
					Design	Physical
Therm Ox	SiO_2	–	500 ±10			√
L0	MoN_x	0 ±50	40 ±10	kinetic inductance, L_k = 8 ±1 pH/sq. I_c = 0.5 mA for 1.0- μm line width	√	√
AL0	SiO_2	–	130 ±10			√
C0		0 ±50		I_c = 0.5 mA for 1 μm x 1 μm via	√	
M0	Nb	0 ±50	200 ±10	I_c = 20 mA for 500-nm line width	√	√
A0	SiO_2	–	200 ±30			√

Layer Name	Material	Fabrication Tolerance (nm)	Thickness (nm)	Electrical Properties	Layer Type	
					Design	Physical
I0		**0 ±50**		I_c = 20 mA for 1.0-μm via, L_{via} = 0.24pH for 700 nm square via	√	
M1	**Nb**	**0 ±50**	**200 ±10**	I_c = 20 mA for 500-nm line width	√	√
A1	SiO_2	–	**200 ±30**			√
I1		**0 ±50**		I_c = 20 mA for 1.0-μm via, L_{via} = 0.24pH for 700 nm square via	√	
M2	**Nb**	**0 ±50**	**200 ±10**	I_c = 20 mA for 500-nm line width	√	√
A2	SiO_2	–	**200 ±30**			√
I2		**0 ±50**		I_c = 20 mA for 1.0-μm via, L_{via} = 0.24pH for 700 nm square via	√	
M3	**Nb**	**0 ±50**	**200 ±10**	I_c = 20 mA for 500-nm line width	√	√
A3	SiO_2	–	**200 ±30**			√
I3		**0 ±50**		I_c = 20 mA for 1.0-μm via, L_{via} = 0.24pH for 700 nm square via	√	
M4	**Nb**	**0 ±50**	**200 ±10**	I_c = 20 mA for 500-nm line width	√	√
A4	SiO_2	–	**200 ±30**		√	
I4		**–**		I_c = 20 mA for 1.0-μm via, L_{via} = 0.24pH for 700 nm square via	√	
M5	**Nb**	**0 ±50**	**150 ±10**	I_c = 15 mA for 500-nm line width	√	√
J5	**Nb**	**See Eq. 2**	**180 ±20**	J_c = 100 μA/μm²; specific capacitance Cs = 70 fF/μm²; I_cR_N = 1.6 mV, R_{sg}/R_N ≈ 10	√	√
A5a*	$NbAlO_x$	–	**20 ±5**			√
A5b*	SiO_2	–	**190 ±30**			√
R5	**–**	**0 ±50**	**40 ±10**	Sheet resistance options**: Standard R_s = 2.0 ±0.3 Ω/□, L_s = 1.13 pH/□ High R_s = 6.0 ±1.5 Ω/□, L_s ~ 1 pH/□	√	√
A5c*	SiO_2	–	**80 ±5**			√
C5J		**0 ±50**			√	
C5R		**0 ±50**			√	

Layer Name	Material	Fabrication Tolerance (nm)	Thickness (nm)	Electrical Properties	Layer Type	
					Design	Physical
I5		**0 ±50**		I_c = 20 mA for 1.0-μm via, L_{via} = 0.24pH for 700 nm square via	√	
M6	**Nb**	**0 ±50**	**200 ±10**	I_c = 20 mA for 500-nm line width	√	√
A6	SiO_2	–	**200 ±30**			√
I6		**0 ±50**		I_c = 20 mA for 1.0-μm via, L_{via} = 0.24pH for 700 nm square via	√	
M7	**Nb**	**0 ±50**	**200 ±10**	I_c = 20 mA for 500-nm line width	√	√
A7	SiO_2	–	**200 ±30**			√
I7		**0 ±50**		I_c = 0 (nonsuperconducting)	√	
M8	**Au/Pt/Ti**	**0 ±50**	**250 ±20**		√	√

Relative dielectric permittivity for all SiO_2 layers is 4.6±0.1.
Magnetic field penetration depth (aka London penetration depth) in Nb layers λ = 90 nm.
***The final thickness of SiO_2 dielectric between layers M5 and M6 is 250±30 nm. Total dielectric thickness (SiO_2 + anodization) between M5 and M6 thickness is 270±30 nm. The SiO_2 dielectric thickness between M5 and R5 layers is 190±20 nm.**
**** Two materials with different sheet resistance are available. For any give wafer, only one sheet resistance value is realized.**

We suggest using layer M4 as a ground plane under JJs. Other layers can be used for any type of passive transmission lines, e.g., layers M0 and M2 can be used for 50-Ω inverted microstrip lines, and layers M5, M6, and M7 for stripline and microstrip inductors. The measured inductances for these layers are given in Table 2. Process variations in the local dielectric thickness, metal thickness, and metal line width are expected to limit inductance variability to 7% (1 sigma). The use of other layers for inductors and transmission lines is possible. Please consult with MIT LL on the expected parameter distributions.

An example showing the relative relationship of a Josephson junction and associated shunt resistor, with related contacts and metal layers is shown in Figure 3. C5J contacts must be circularly shaped or reflect the symmetry of the selected junction shapes, and design rules presented in Section 4 below require that all C5J instances be fully surrounded by J5.

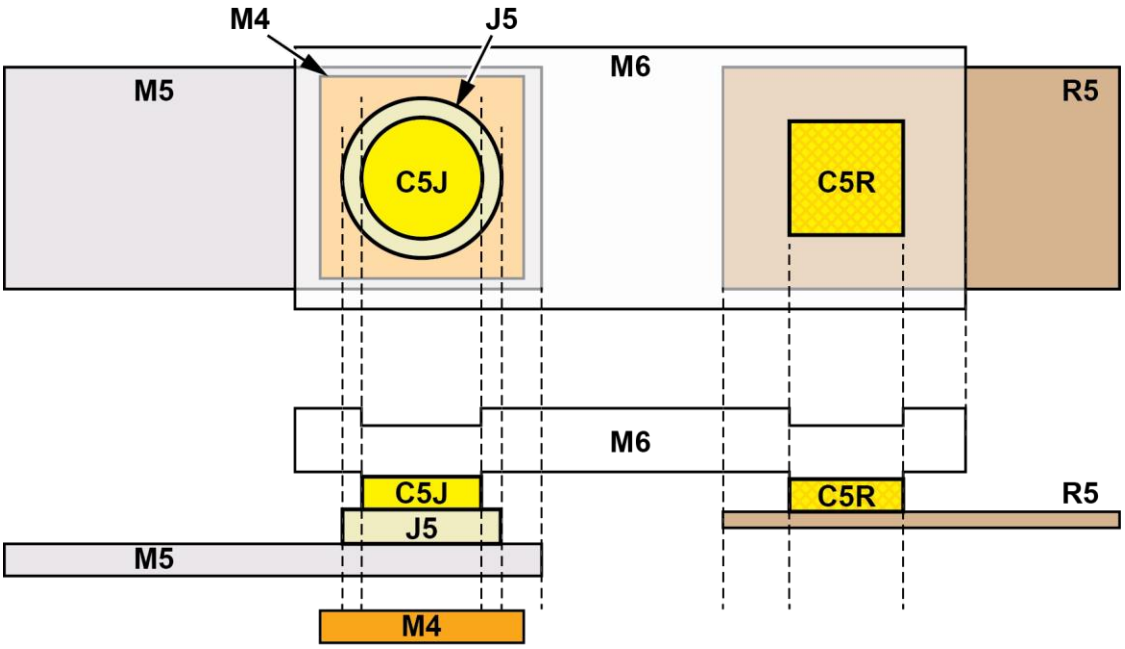

Figure 3. Top-down and cross-section view of a Josephson junction and related layers.

Josephson Junctions

For Josephson junctions we recommend "circular" shaped polygons with all vertices snapped to the grid and the maximum possible number of vertices consistent with the grid size. The polygons should have a high rotational symmetry (4th order or higher). The relationship between the design JJ diameter, d_d, and the resultant JJ diameter on wafers d_w is given by

$$d_w = (d_d^2 - d_c^2)^{1/2} + b, \text{ for } d_d > d_c \text{ and } \quad d_w = 0 \text{ otherwise}, \quad (1)$$

where d_c = 250 nm ± 10 nm and b = (-20 ± 50) nm [1],[2]. Inversion of (1) gives the design size as the function of the desired size on the wafer:

$$d_d = [(d_w - b)^2 + d_c^2)]^{1/2} \text{ for } d_d > d_c \quad (2)$$

Please note the sign convention for parameter b. It is negative when an object size on wafer is smaller than the drawn size. **This correction is expected to be done by circuit designers.**

The use of other shapes, e.g., square, is allowed. However, we cannot guarantee the linear scaling of I_c with the junction area, especially for small junction sizes, as the appropriate bias functions for other shapes are not known. It would then be the user's responsibility to establish them and make necessary adjustments to the design.

Resistors

For resistors, we recommend a layout style shown in Figure 4a, with the two resistor ends contacted by C5R satisfying design rule 52.3 (Section 4 below) requiring that C5R be surrounded by R5. In some cases, a more accurate resistor value can be obtained by using an alternative layout shown in Figure 4b, with the resistor length defined by C5R contacts.

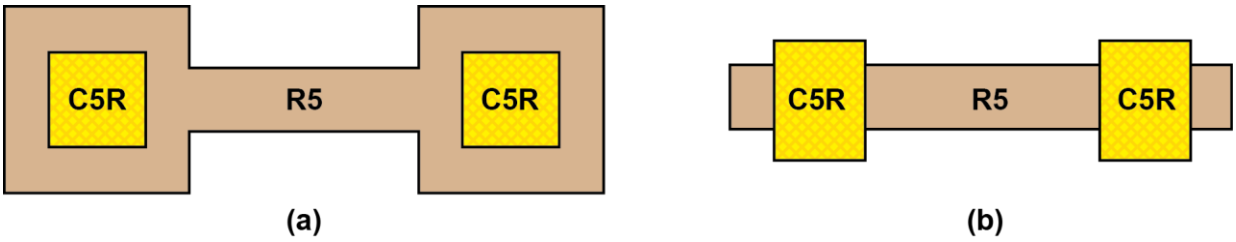

Figure 4(a). Standard resistor layout satisfying all design rules. 4(b) Alternative resistor layout with overlapping C5R contacts.

This alternative design is more compact, but violates design rule 52.3 and has been less thoroughly tested. Overlap of C5R and M5 edges is allowed in this case. *A DRC waiver subject to MIT LL approval may be obtained for this approach*. Please note that the resistor linewidth in the area of the C5R contact in Fig. 3 shrinks by ~50 nm. In either case, because physical resistor thickness is small (~40-nm) compared to M5 thickness (~150 nm), R5 crossing M5 edges is not recommended.

Vias

Vias are used to electrically connect metal layers as well as to provide connectivity to Josephson junctions and resistors. In the simplest case, vias connect two successive metal layers, M_i to M_{i+1} (I = 1, 2, … 8), and stacked vias are used to minimize area required.

Stacking minimium sized vias is not allowed on any sequential via levels, but is allowed on alternating via levels. For an example, a 0.7-μm I1 via cannot be stacked over an I0 via, but a 0.7-μm I2 via can be stacked over an I0 via.

Stacking of I6 vias on top of C5J contacts is allowed in cases when minimization of via inductance to a JJ is needed and such a stacking cannot be avoided. A design example is shown in Figure 5(a). Similarly, in some cases it may be necessary to minimize inductance of a resistor connection to a ground plane M7. In that case, I6 via overlap with C5R contact to a resistor as shown in Figure 5(b) is allowed.

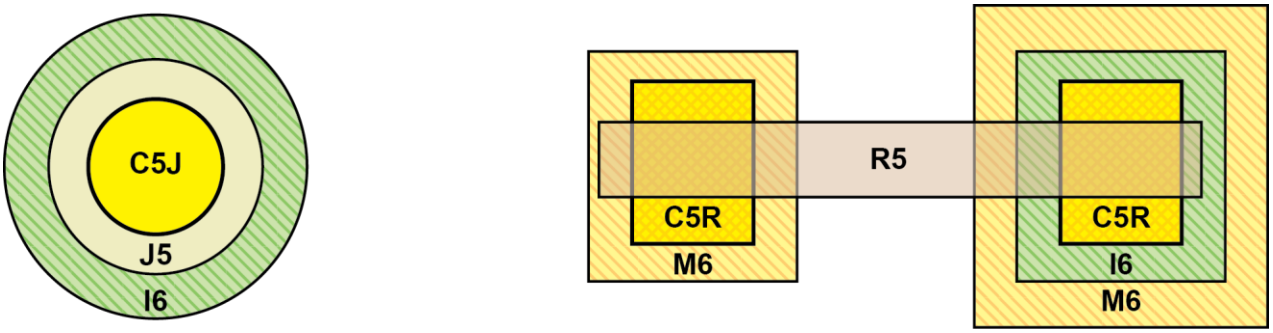

Figure 5(a). Overlapping I6 and C5J contacts on top of J5. 5(b) Overlapping I6 and C5R contacts on top of resistor R5.

Stacking of two vias on two sequential levels I_i and I_{i+1} (i = 0, 1, 2, 5, 6) is allowed **only if the upper via I_{i+1} completely surrounds via I_i by 0.3 µm** as shown in Figure 6. All via and metal surround rules given in Section 4 below apply. Stacking of three or more expanding vias is not allowed. The minimum distance between non-overlapping stacked vias should be 0.7 µm, e.*g*., an I1 via can be stacked on an I0 via with a 0.3-µm surround, and I3 via can be stacked on I2 via, but I2 min distance to I1 should be 0.7 µm. **Stacking with I4 is not allowed**.

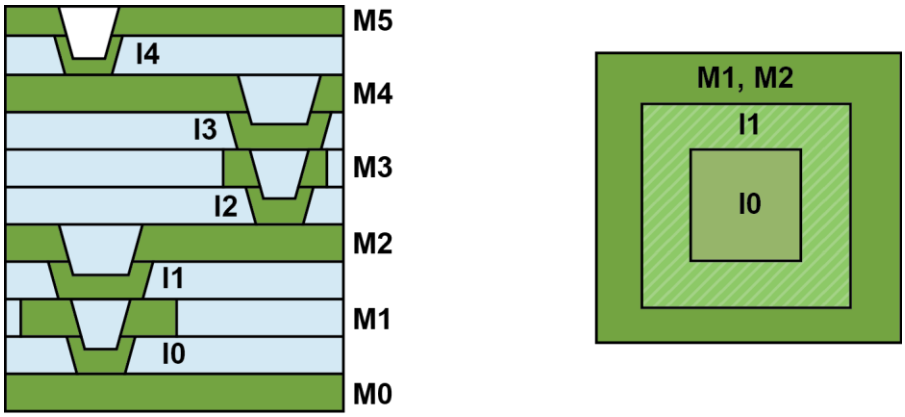

Figure 6(a). Two-via stacks connecting JJ base electrode M5 with M0. 6(b) Overlapping-I1-I0 two-via stack.

Wires

Note that the realized "electrical" feature sizes of wires may vary from (generally are smaller than) the "drawn" dimensions. The size change, if any, from the drawn structure to the actual (realized) electrical structure will be adjusted accordingly **during mask generation** if needed.

Please see model guide for recommended linewidth selection section for wires in contact with resistor. Critical currents of wires connected to resistors will be significantly reduced due to heating.

Inductances of Superconducting Layers

Typical inductances of various layer combinations are documented in this section. We will refer to microstrip and inverted microstrip line inductors using Signal-Ground notation, e.g., M6_M7 identifying signal layer, M6, followed by the ground plane layer, M7. Similarly, all stripline configurations will be referred to as Ground-Signal-Ground, e.g., M4_M6_M7 identifying the patterned signal line with width, *w,* on layer M6 sandwiched between two ground planes: M4 below it and M7 above it.

Inductances of the striplines and microstrip lines were measured using DC-SQUIDs. The experimental data available to date are summarized in Table 2 for 30 wafers from the SFQ5ee process measured between March 2016 and March 2017.

Inductors requiring tight tolerances should use larger geometries than the minimum layout rules. See Table 2 for standard deviation of select stripline and microstrip configurations; see model guide for further information on scaling of inductance with size.

Table 2. Mean inductance per unit length for microstrip (2 layers in combination) and stripline (3 layers in combination) configurations of straight-line inductors (based on SFQ5ee measurements).

Wiring Layer Combination	Width (µm)	Dielectric thickness (nm)	Mean Inductance per Length (pH/µm)	Standard Deviation (%)
M1_M0	0.35	200	0.566	5.7
M1_M0	0.5	200	0.457	4.6
M1_M0	0.7	200	0.367	3.8
M1_M0	1	200	0.290	4.1
M1_M0	2	200	0.179	3.9
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M0_M1_M2	0.35	200_200	0.478	8.8
M0_M1_M2	0.5	200_200	0.367	7.4
M0_M1_M2	0.7	200_200	0.285	7.0
M0_M1_M2	1	200_200	0.221	4.1
M0_M1_M2	2	200_200	0.118	8.5
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M2_M3_M4	0.25	200_200	0.597	12.6
M2_M3_M4	0.35	200_200	0.476	6.7
M2_M3_M4	0.5	200_200	0.367	6.5
M2_M3_M4	0.7	200_200	0.290	6.2
M2_M3_M4	1	200_200	0.218	6.0
M2_M3_M4	2	200_200	0.122	4.9
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M5_M4	0.35	200	0.684	4.2
M5_M4	0.5	200	0.531	2.4
M5_M4	0.7	200	0.422	7.3
M5_M4	1	200	0.345	1.7
M5_M4	2	200	0.205	2.0
M5_M4	4	200	0.116	2.6

Wiring Layer Combination	Width (µm)	Dielectric thickness (nm)	Mean Inductance per Length (pH/µm)	Standard Deviation (%)
M4_M5_M7	0.35	200_680	0.656	9.0
M4_M5_M7	0.5	200_680	0.493	2.8
M4_M5_M7	0.7	200_680	0.386	3.6
M4_M5_M7	1	200_680	0.304	2.3
M4_M5_M7	2	200_680	0.172	2.9
M4_M5_M7	4	200_680	0.091	2.2
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M6_M4	0.35	615	0.678	7.5
M6_M4	0.5	615	0.577	2.4
M6_M4	0.7	615	0.499	4.8
M6_M4	1	615	0.427	3.3
M6_M4	2	615	0.288	2.4
M6_M4	4	615	0.181	2.2
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M4_M6_M7	0.35	615_200	0.495	22.8
M4_M6_M7	0.5	615_200	0.354	15.3
M4_M6_M7	1	615_200	0.245	4.1
M4_M6_M7	2	615_200	0.147	2.0
M4_M6_M7	4	615_200	0.077	5.2
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M4_M7	0.35	1015	0.742	5.3
M4_M7	0.5	1015	0.639	9.1
M4_M7	0.7	1015	0.568	1.8
M4_M7	1	1015	0.474	11.4
M4_M7	1.4	1015	0.416	4.6

Wiring Layer Combination	Width (µm)	Dielectric thickness (nm)	Mean Inductance per Length (pH/µm)	Standard Deviation (%)
M5_M7	0.35	680	0.837	3.7
M5_M7	0.5	680	0.679	2.7
M5_M7	0.7	680	0.552	14.7
M5_M7	1	680	0.477	6.5
M5_M7	2	680	0.308	2.9
M5_M7	4	680	0.188	3.2
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M6_M7	0.35	200	0.520	11.3
M6_M7	0.5	200	0.417	3.6
M6_M7	0.7	200	0.347	7.5
M6_M7	1	200	0.277	4.3
M6_M7	2	200	0.167	5.4
M6_M7	4	200	0.096	6.3

3. DESIGN LAYERS

This section lists the available design layers in the SFQ5eg technology. Supported design layers in actual technologies (e.g.SFQ3ee, SFQ4ee, and SFQ5ee) will be either a subset or superset of this list. In addition to defining design layers, design purposes are also defined; the purpose definitions are listed in Table 3. The intention of design purposes is to define subsets of shapes on a design layer that serve particular functions. For example, the label purpose defines those objects on a layer that are used only for defining port names without corresponding to a polygon to be included in mask data on that layer. Although not all layer and purpose combinations may be strictly required, it is recommended to offer at least cursory support in a process design kit (PDK) for all layer-purpose combinations.

Design layers used for presently supported technology nodes are listed in Table 4. Table 4 also shows the mask GDS number, where applicable, that corresponds to the shapes associated with that design layer and its drawing purpose. A layer with a defined name and no mask layer number may be omitted from mask layer GDS generation, but has a required usage in design layout generation (usually to enable design rule checking or layout versus schematic checks). Although mask layer numbers are specified by MITLL, layout database layer numbers are not. The PDK developer is therefore free to adopt a layout database numbering convention that is suited to the vendor-specific needs of the layout editor supported by the PDK. It is therefore the burden of the PDK developer to ensure that translation of layout database information to mask layer GDS is handled correctly.

Table 3. Process Design Kit Layer Purposes

PDK Purpose	Description
drawing	Represents most design data; features on the drawing layer are directly used as inputs to the autogeneration routine to create mask data
fill	Dummy structure needed for uniform planarization and etch; features will be merged with those of drawing layer
net	Output layer in the layout extracted view that is generated by connectivity extraction tools
pin	Used for labeling that corresponds to subcircuit ports
label	Used for text labeling
blockage	Used for blocking for autorouting
nofill	Suppresses autogeneration of dummy fill patterns on the corresponding layer
text	Used for labeling nets that do not correspond to subcircuit ports; also used for other annotation purposes
autofill	Analogous to fill layer but used to indicate such shapes that are generated automatically during reticle planning by MIT LL
opc	Used for data that has undergone optical proximity correction during reticle planning by MIT LL
xpp	*Not implemented in design kit. Used to represent design data that are directly merged with the automatically generated mask data prior to final stream-out; no postprocessing will be applied.*
drcwaive	Used to create regions in which design rule checks on shapes on the corresponding layer are suppressed

Table 4. Design Layers for Presently Supported Technology Nodes

PDK Layer	Mask GDS No.	Layer Description
M0	1	Superconducting wiring; I_c = 20 mA for 500-nm line width
I0	2	Via connection between M0 and M1; I_c = 20 mA for 1.0-μm via
L0	3	High kinetic inductance layer for bias inductors; kinetic inductance per square, L_k = 8 ±1 pH/sq. I_c = 0.5 mA for 1.0-μm line width
C0	4	Via between L0 and M0, I_c = 0.5 mA for 1.0 μm x 1.0 μm via
M1	10	Superconducting wiring; I_c = 20 mA for 500-nm line width
I1	11	Via connection between M1 and M2; I_c = 20 mA for 1.0-μm via
M2	20	Superconducting wiring; I_c = 20 mA for 500-nm line width
I2	21	Via connection between M2 and M3; I_c = 20 mA for 1.0-μm via
M3	30	Superconducting wiring; I_c = 20 mA for 500-nm line width
I3	31	Via connection between M3 and M4; I_c = 20 mA for 1.0-μm via
M4	40	Superconducting wiring; I_c = 20 mA for 500-nm line width
I4	41	Via connection between M4 and M5; I_c = 20 mA for 1.0-μm via
M5	50	Josephson junction bottom electrode; I_c = 15 mA for 500- nm line width
J5	51	Josephson junction; J_c = 100 μA/μm²; specific capacitance Cs = 70 fF/μm²; I_cR_N = 1.6 mV, R_{sg}/R_N ≈ 10
R5	52	Resistor**, two options available: Sheet resistance Rs = 2.0 ±0.3 Ω/sq High sheet resistance Rs = 6.0 ±1.5 Ω/sq
	53	Reserved (previously used for C5; replaced by C5J and C5R)
I5	54	Via connection between M5 and M6; I_c = 20 mA for 1.0-μm via
C5J	55	Contact to Josephson Junction
C5R	56	Contact to Resistor
M6	60	Superconducting wiring; I_c = 20 mA for 500-nm line width
I6	61	Via connection between M6 and M7; I_c = 20 mA for 1.0-μm via
M7	70	Superconducting wiring; I_c = 20 mA for 500-nm line width
I7	71	Via connection between M7 and M8; I_c = 0 (nonsuperconducting)
M8	80	Contact metallization/underbump for chip packaging (wire bonding or flip chip bonding)
NOFILL	177	Flag to suppress automatic generation of fill structures
CE	180	Identifies no device zone around chip edges
TEXT	182	Text layer
DEVL		Flag device is inductor
DEVC		Flag device is capacitor

4. DESIGN RULES

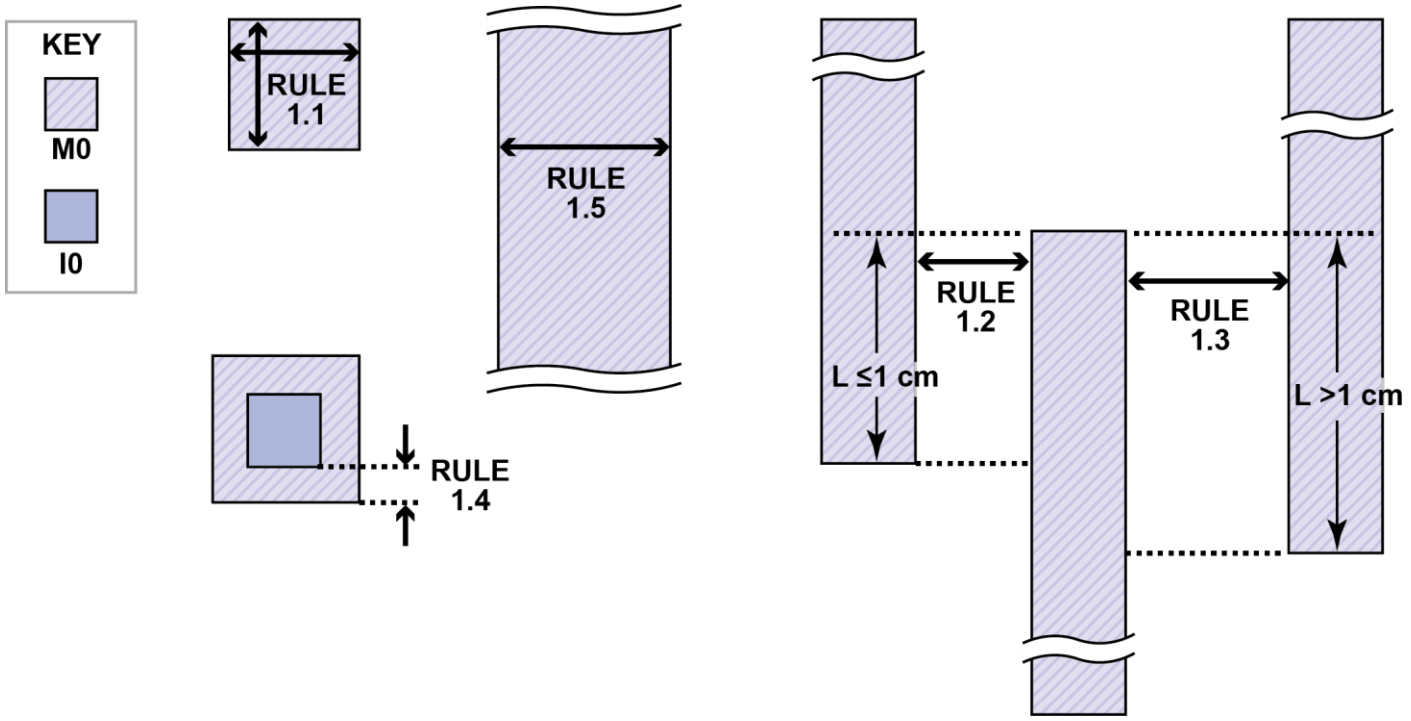
Definitions

	Term	Definition	Additional Notes
Descriptions	Flag	Logical layer used to control verification or autogeneration processing of a layout	
	Interacting	Overlapping or touching	If feature A overlaps or touches feature B, feature A is said to be *interacting* with feature B.
	Unrelated	Non-interacting	If feature A is non-interacting with feature B, feature A is said to be *unrelated* to feature B.
	Common	Interacting plurally	If feature A interacts with both feature B and feature C, feature A is said to be *common* to feature B and feature C.

	Term	Definition	Additional Notes
Rule Types	"D" Rule	Density	"D" as a prefix to a rule number denotes a density requirement, applied after generation of fill patterns by MIT LL
	"W" Rule	Warning	"W" as a prefix to a number denotes an important warning that a designer must consider on a case-by-case basis during the design process. It is not binned with the set of recommended rules.

1 Metal 0 Layer (M0)

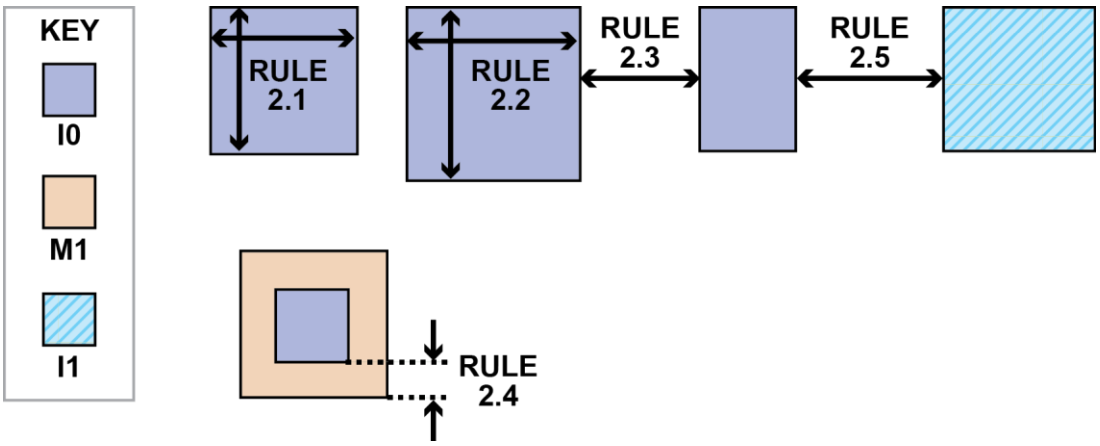
Rule	Description	Value
1.1	M0 min size	0.5 µm
1.2	M0 to M0 min space for L ≤ 1 cm (L = length of gap between two adjacent M0 features)	0.5 µm
1.3	M0 to M0 min space for L > 1 cm	1.0 µm
1.4	M0 min surround of I0	0.30 µm
1.5	M0 max width (except for pads)	20.0 µm
D1.1	M0 min density (any 200 µm x 200 µm box)	15%
D1.2	M0 max local density (any 200 µm x 200 µm box)	85%
D1.3	M0 max global density (5 mm x 5 mm chip)	80%



2 Via between M0 and M1 (I0)

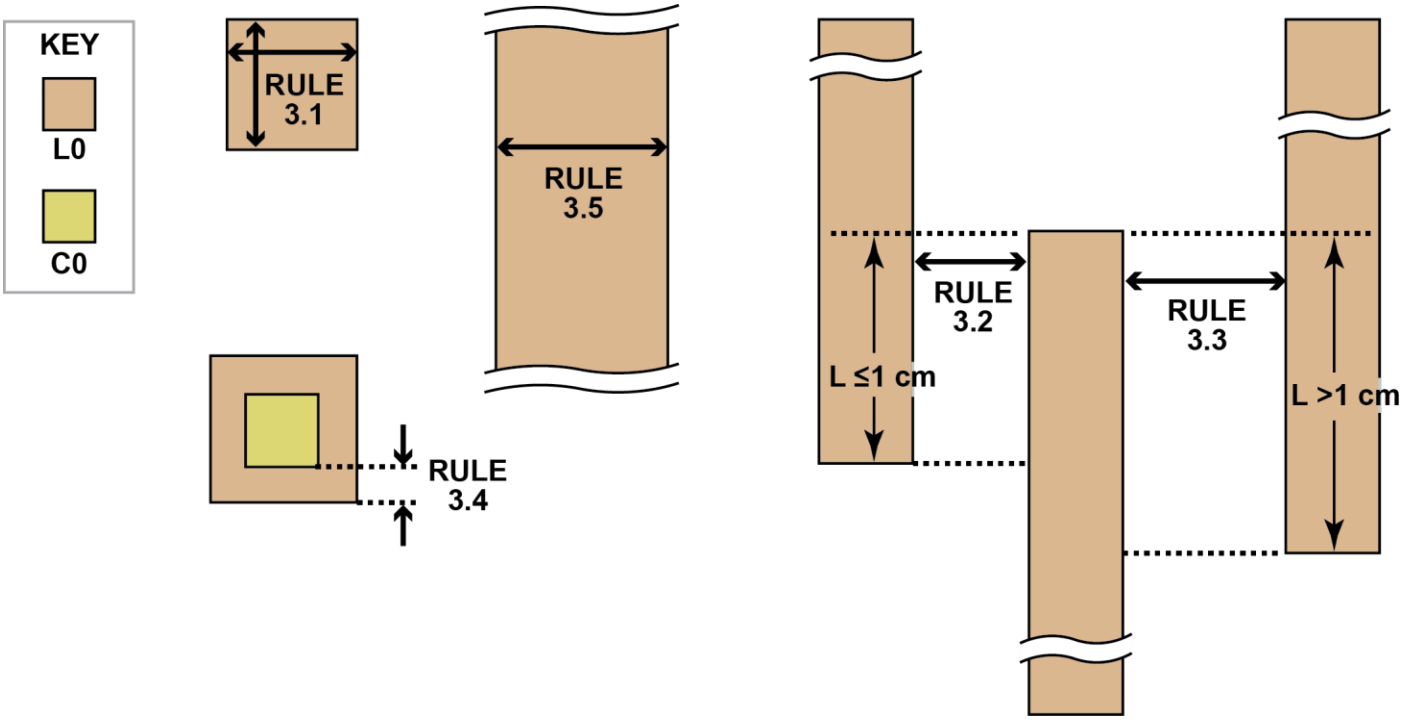
Rule	Description	Value
2.1	I0 min size	0.6 µm
2.2	I0 max size	1.2 µm
2.3	I0 to I0 min space (on the same node)	0.7 µm
2.4	I0 min surround by M1	0.30 µm
2.5	I0 to non-overlapping I1 min space	0.7 µm
2.6	I0 partial overlap with I1	prohibited
D2.1	I0 min density (any 200 µm x 200 µm box)	0%
D2.2	I0 max local density (any 200 µm x 200 µm box)	25%
D2.3	I0 max global density (5 mm x 5 mm chip)	25%

I0 via can be square or rectangular.



3 High Kinetic Inductance Layer (L0)

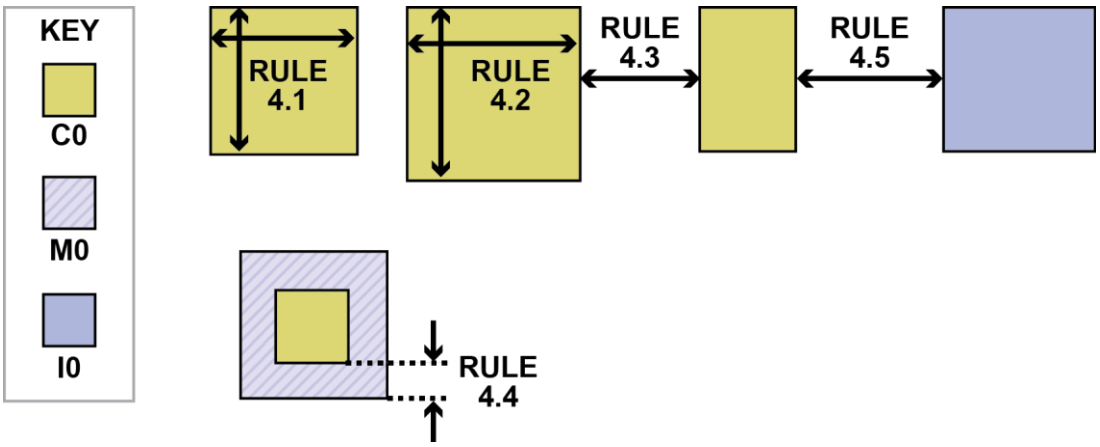
Rule	Description	Value
3.1	L0 min size	2.0 μm
3.2	L0 to L0 min space for length L ≤1 cm (L = length of gap between two adjacent L0 features)	0.7 μm
3.3	L0 to L0 min space for length L >1 cm	1.0 μm
3.4	L0 surround of C0	0.35 μm
3.5	L0 width size	20 μm
D3.1	L0 min density (any 200 μm x 200 μm box)	0%
D3.2	L0 max local density (any 200 μm x 200 μm box)	85%
D3.3	L0 max global density (5 mm x 5 mm chip)	80%



4 Contact 0 Layer (C0)

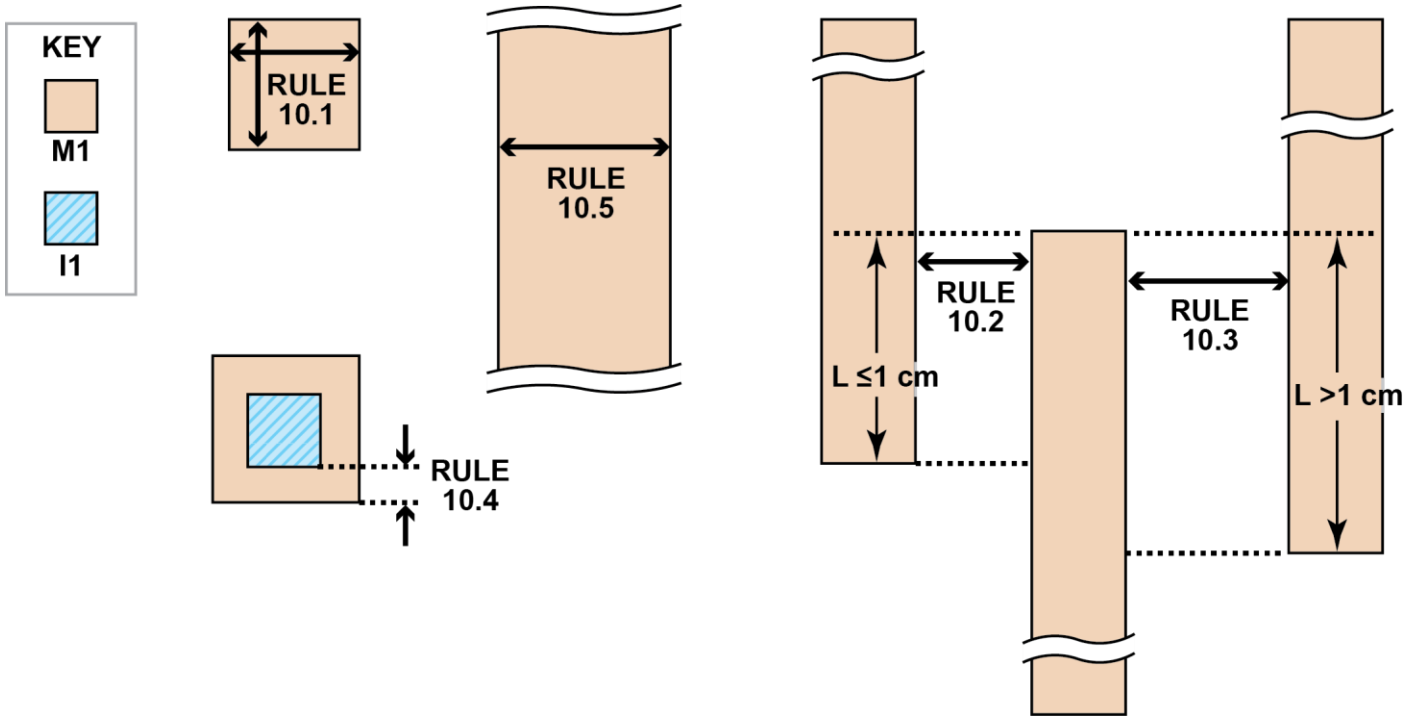
Rule	Description	Value
4.1	C0 min size	0.7 µm
4.2	C0 max size	1.0 µm
4.3	C0 to C0 min space (on the same node)	0.7 µm
4.4	C0 min surround by M0	0.35 µm
4.5	C0 to I0 min space	0.7 µm
D4.1	C0 min density (any 200 µm x 200 µm box)	0%
D4.2	C0 max local density (any 200 µm x 200 µm box)	25%
D4.3	C0 max global density (5 mm x 5 mm chip)	25%

C0 via can be square or rectangular.



10 Metal 1 Layer (M1)

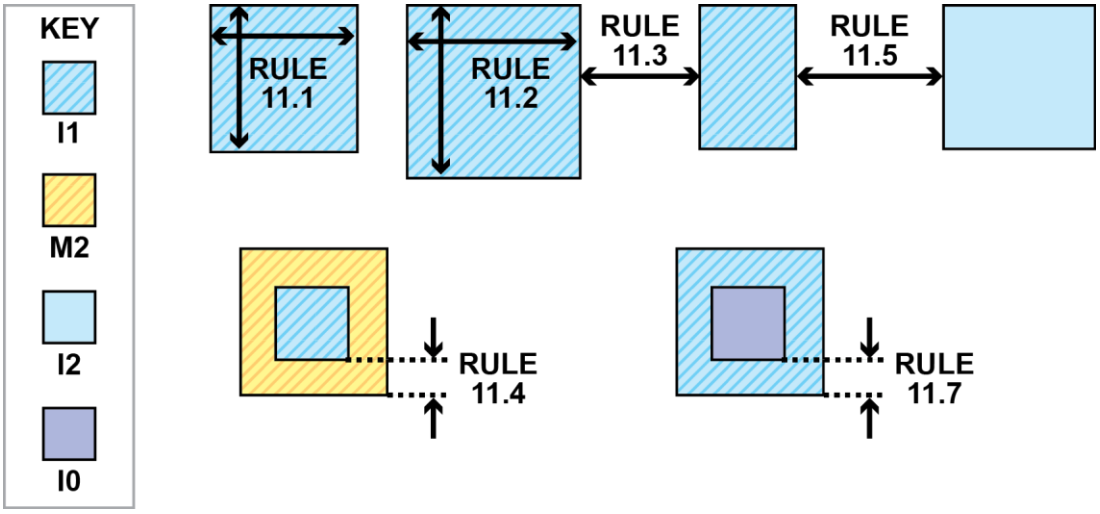
Rule	Description	Value
10.1	M1 min size	0.5 µm
10.2	M1 to M1 min space for L ≤ 1 cm (L = length of gap between two adjacent M1 features)	0.5 µm
10.3	M1 to M1 min space for L > 1 cm	1.0 µm
10.4	M1 min surround of I1	0.30 µm
10.5	M1 max width (except for pads)	20.0 µm
D10.1	M1 min density (any 200 µm x 200 µm box)	15%
D10.2	M1 max local density (any 200 µm x 200 µm box)	85%
D10.3	M1 max global density (5 mm x 5 mm chip)	80%



11 Via between M1 and M2 (I1)

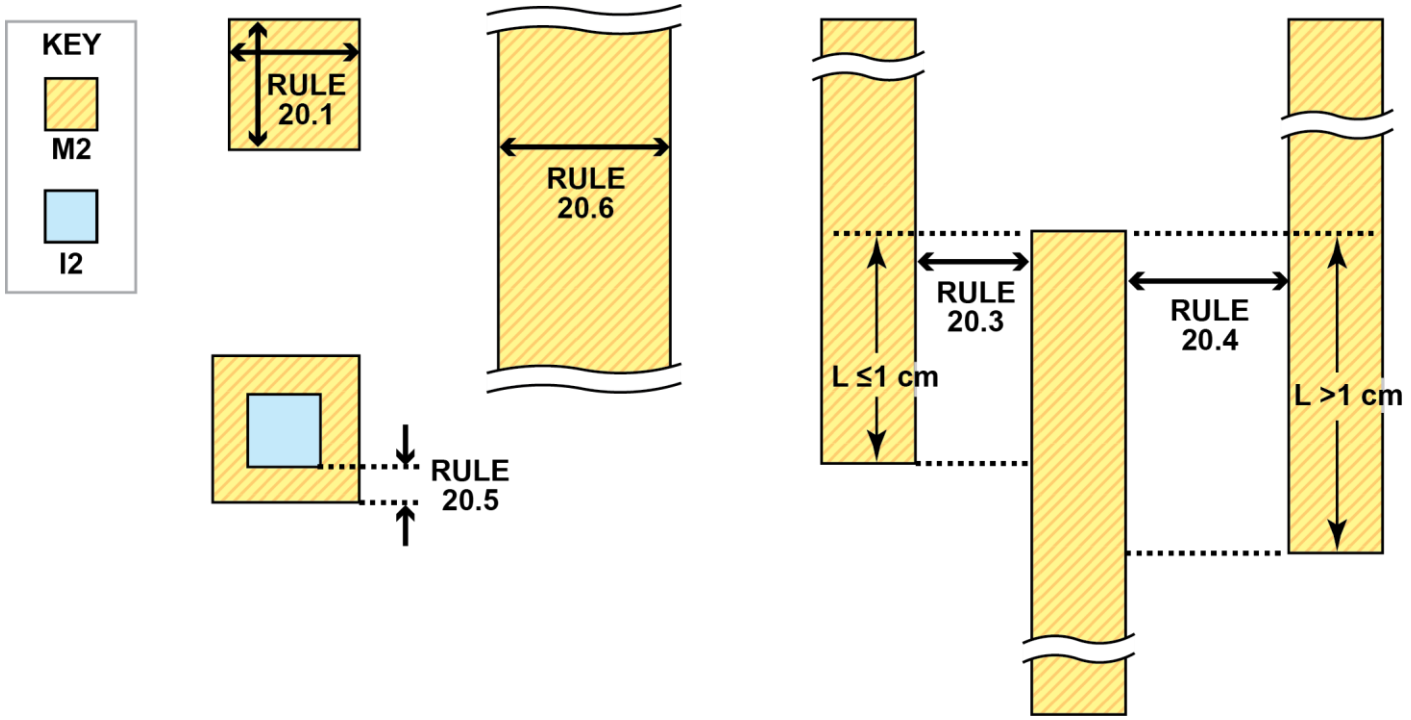
Rule	Description	Value (μm)
11.1	I1 min size	0.6 μm
11.2	I1 max size	1.2 μm
11.3	I1 to I1 min space (on the same node)	0.7 μm
11.4	I1 min surround by M2	0.30 μm
11.5	I1 to non-overlapping I2 min space	0.7 μm
11.6	I1 partial overlap with I2	prohibited
11.7	I1 via stacked on I0, min surround of I0*	0.3 μm
D11.1	I1 min density (any 200 μm x 200 μm box)	0%
D11.2	I1 max local density (any 200 μm x 200 μm box)	25%
D11.3	I1 max global density (5 mm x 5 mm chip)	25%

I1 via can be square or rectangular.
*See Section 2 “Vias” for special requirements for stacking two expanding vias



20 Metal 2 Layer (M2)

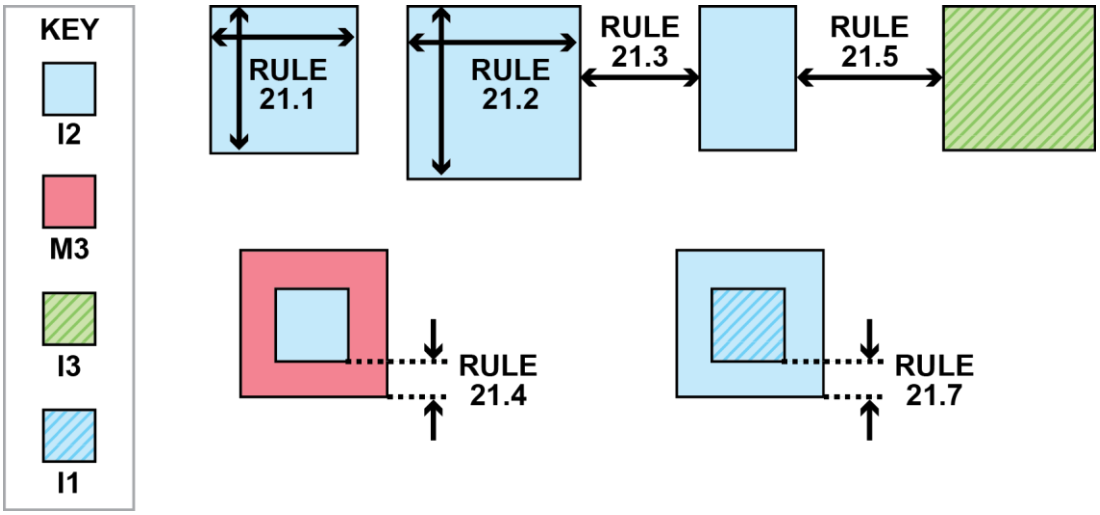
Rule	Description	Value
20.1	M2 min size	0.35 μm
20.2	M2 min size for inductors	0.5 μm
20.3	M2 to M2 min space for L ≤ 1 cm (L = length of gap between two adjacent M2 features)	0.5 μm
20.4	M2 to M2 min space for L > 1 cm	1.0 μm
20.5	M2 min surround of I2	0.30 μm
20.6	M2 max width (except for pads)	20.0 μm
D20.1	M2 min density (any 200 μm x 200 μm box)	15%
D20.2	M2 max local density (any 200 μm x 200 μm box)	85%
D20.3	M2 max global density (5 mm x 5 mm chip)	80%



21 Via between M2 and M3 (I2)

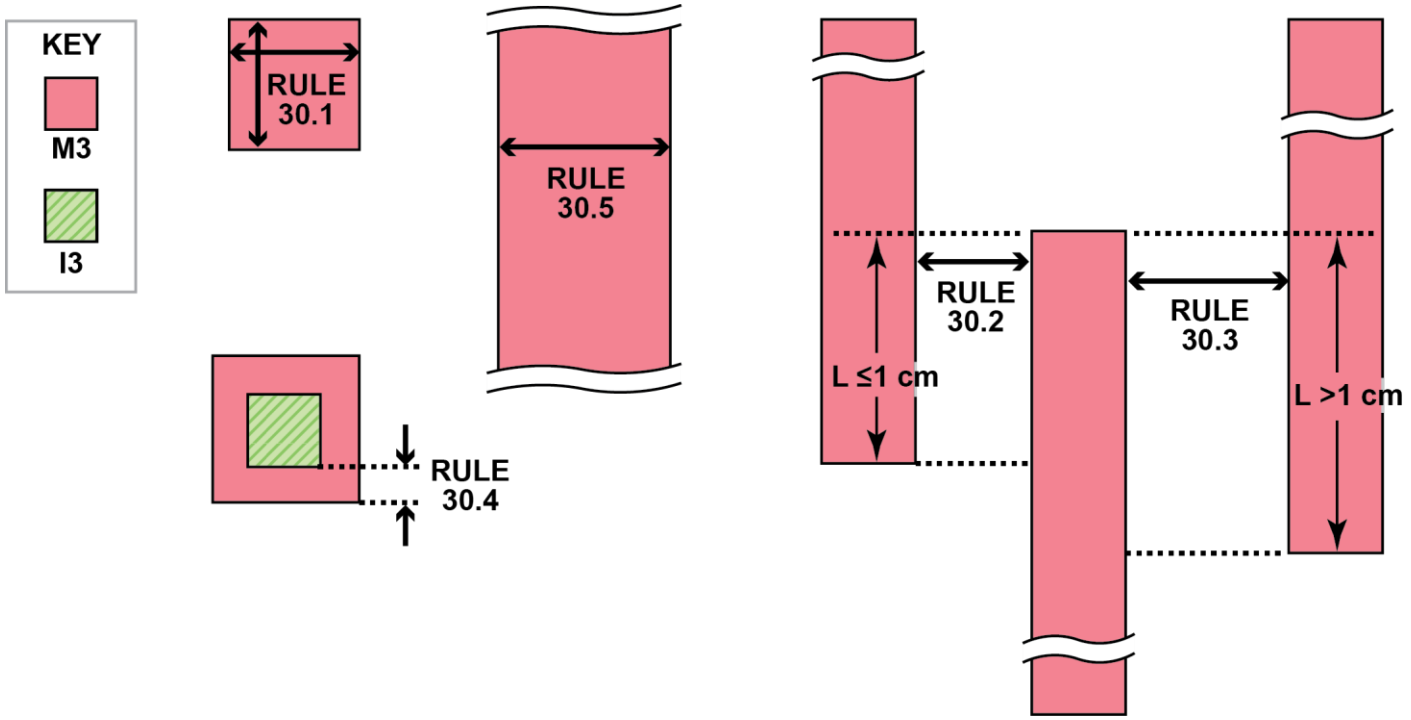
Rule	Description	Value
21.1	I2 min size	0.6 μm
21.2	I2 max size	1.2 μm
21.3	I2 to I2 min space (on the same node)	0.7 μm
21.4	I2 min surround by M3	0.30 μm
21.5	I2 to non-overlapping I3 min space	0.7 μm
21.6	I2 partial overlap with I3	prohibited
21.7	I2 via stacked on I1, min surround of I1*	0.3 μm
D21.1	I2 min density (any 200 μm x 200 μm box)	0%
D21.2	I2 max local density (any 200 μm x 200 μm box)	25%
D21.3	I2 max global density (5 mm x 5 mm chip)	25%

I2 via can be square or rectangular.
*See Section 2 "Vias" for special requirements for stacking two expanding vias



30 Metal 3 Layer (M3)

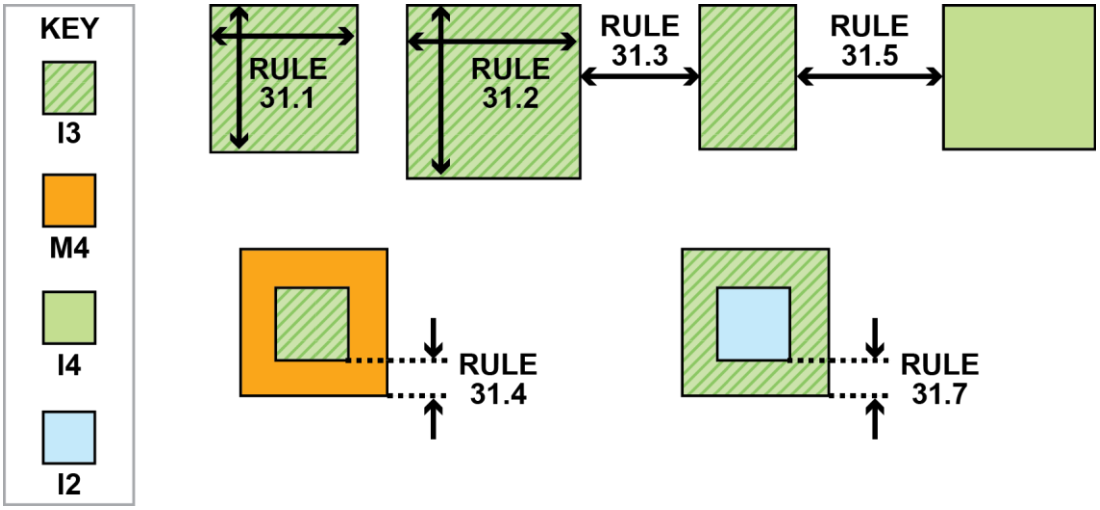
Rule	Description	Value
30.1	M3 min size	0.35 μm
30.2	M3 to M3 min space for L ≤ 1 cm (L = length of gap between two adjacent M3 features)	0.5 μm
30.3	M3 to M3 min space for L > 1 cm	1.0 μm
30.4	M3 min surround of I3	0.30 μm
30.5	M3 max width (except for pads)	20.0 μm
30.6	M3 min size for inductors	0.5 μm
D30.1	M3 min density (any 200 μm x 200 μm box)	15%
D30.2	M3 max local density (any 200 μm x 200 μm box)	85%
D30.3	M3 max global density (5 mm x 5 mm chip)	80%



31 Via between M3 and M4 (I3)

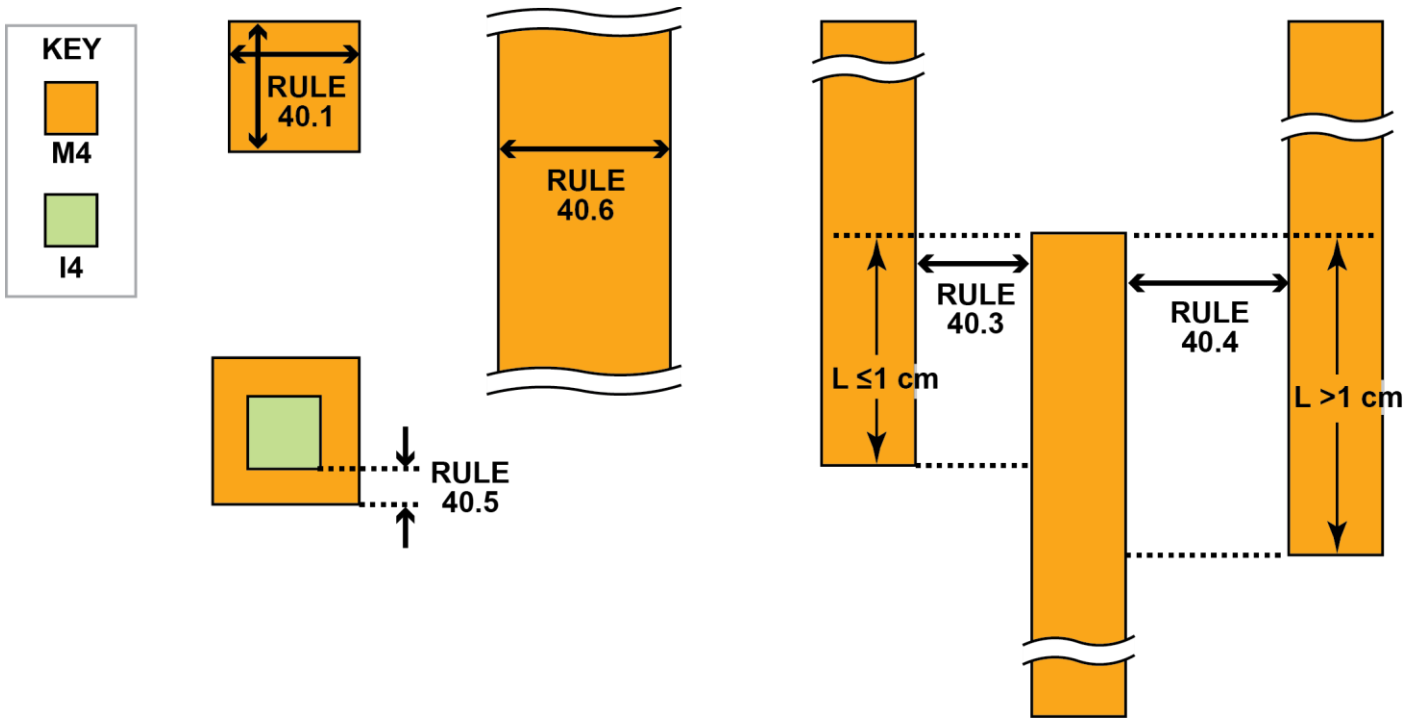
Rule	Description	Value
31.1	I3 min size	0.6 μm
31.2	I3 max size	1.2 μm
31.3	I3 to I3 min space (on the same node)	0.7 μm
31.4	I3 min surround by M4	0.30 μm
31.5	I3 to non-overlapping I4 min space	0.7 μm
31.6	I3 partial overlap with I4	prohibited
31.7	I3 via stacked on I2, min surround of I2*	0.3 μm
D31.1	I3 min density (any 200 μm x 200 μm box)	0%
D31.2	I3 max local density (any 200 μm x 200 μm box)	25%
D31.3	I3 max global density (5 mm x 5 mm chip)	25%

I3 via can be square or rectangular.
*See Section 2 "Vias" for special requirements for stacking two expanding vias



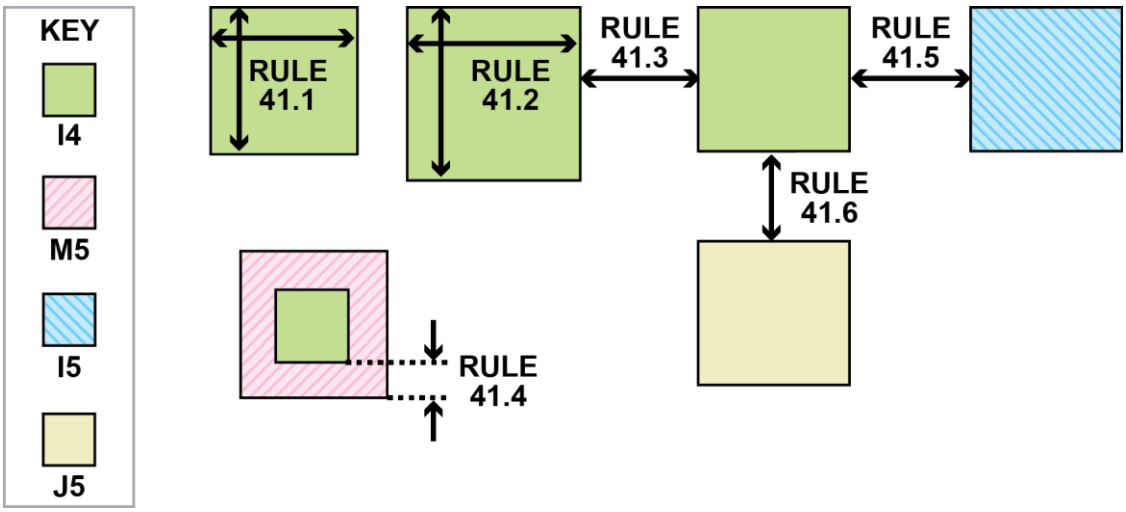
40 Metal 4 Layer (M4)

Rule	Description	Value
40.1	M4 min size	0.35 μm
40.2	M4 min size for inductors	0.5 μm
40.3	M4 to M4 min space for L ≤ 1 cm (L = length of gap between two adjacent M4 features)	0.5 μm
40.4	M4 to M4 min space for L > 1 cm	1.0 μm
40.5	M4 min surround of I4	0.30 μm
40.6	M4 max width (except for pads)	20.0 μm
D40.1	M4 min density (any 200 μm x 200 μm box)	15%
D40.2	M4 recommended min density (any 200 μm x 200 μm box)	35%
D40.3	M4 max local density (any 200 μm x 200 μm box)	85%
D40.4	M4 max global density (5 mm x 5 mm chip)	80%



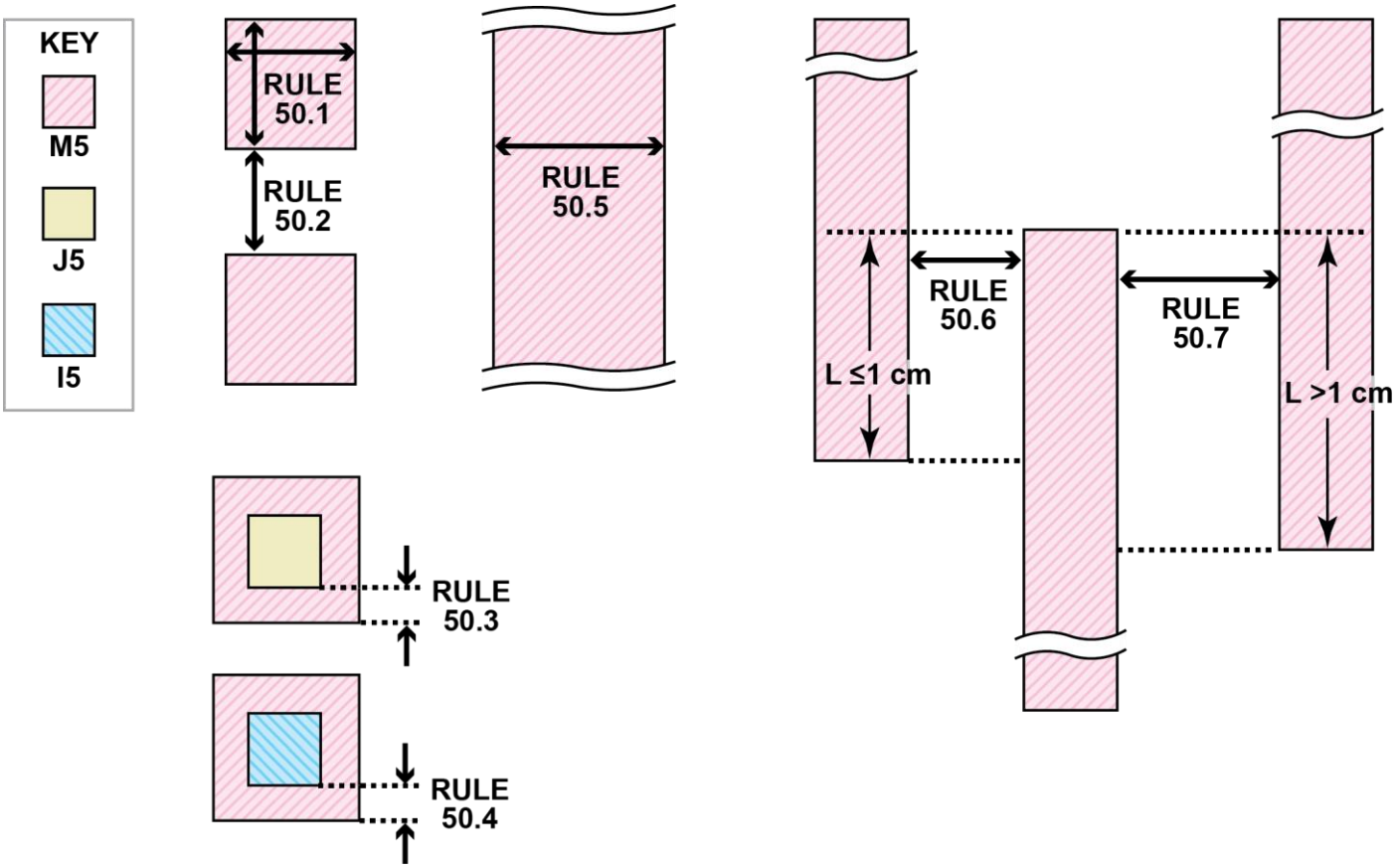
41 Via between M4 and M5 (I4)

Rule	Description	Value
41.1	I4 min size	0.8 µm
41.2	I4 max size	1.2 µm
41.3	I4 to I4 min space (the same node)	1.0 µm
41.4	I4 min surround by M5	0.30 µm
41.5	I4 to I5 min space	1.0 µm
41.6	I4 to J5 min space	1.4 µm
41.7	I4 square shape	required
41.8	Stacking of I4 on I3	prohibited
D41.1	I4 min density (any 200 µm x 200 µm box)	0%
D41.2	I4 via recommended density (any 200 µm x 200 µm box)	N/A
D41.3	I4 max local density (any 200 µm x 200 µm box)	25%
D41.4	I4 max global density (5 mm x 5 mm chip)	25%



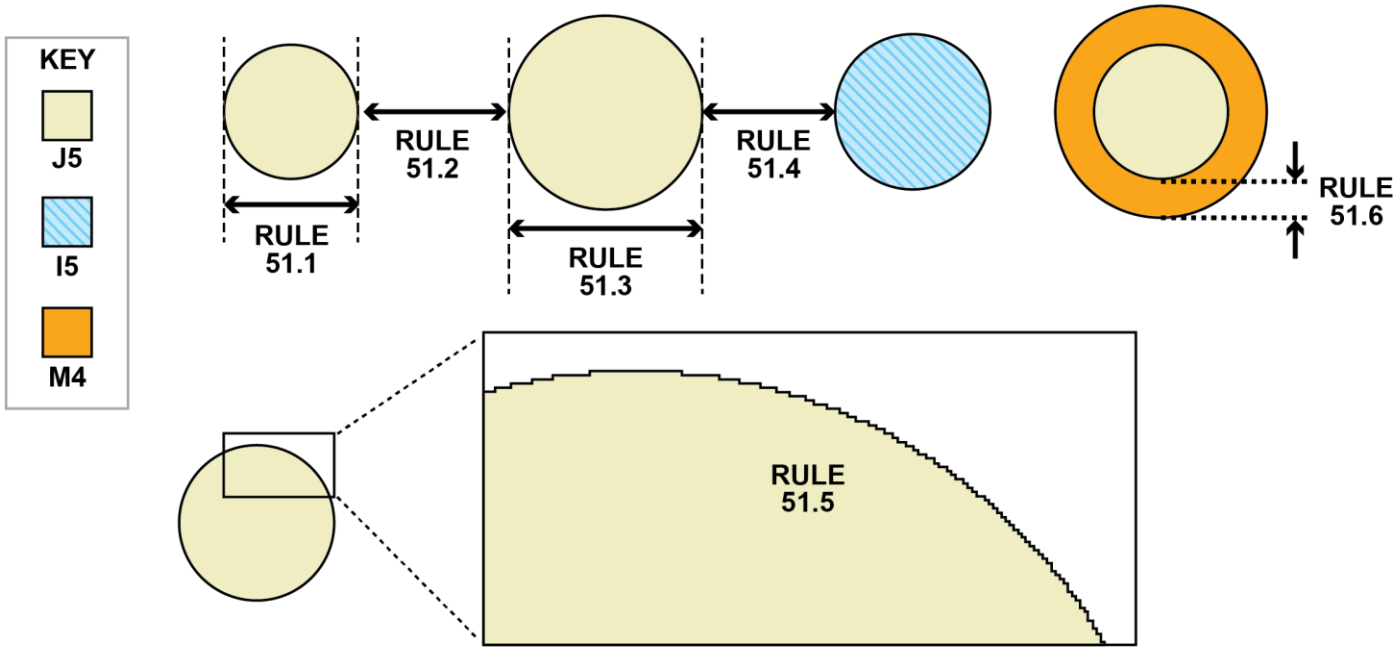
50 Metal 5 Josephson Junction Bottom Electrode Layer (M5)

Rule	Description	Value
50.1	M5 min size	0.7 µm
50.2	M5 to M5 min spacing	1.0 µm
50.3	M5 min surround of J5	0.5 µm
50.4	M5 min surround of I5	0.5 µm
50.5	M5 max width (except for pads)	20.0 µm
50.6	M5 min space if there are no M6 or R5 crossing over (overlapping) the space for L ≤ 1 cm (L = length of gap between two adjacent M5 features)	0.8 µm
50.7	M5 min space if there is no M6 or R5 crossing over (overlapping) the space for L > 1 cm	1.0 µm
D50.1	M5 min density (any 200 µm x 200 µm box)	15%
D50.2	M5 recommended min density (any 200 µm x 200 µm box)	35%
D50.3	M5 max local density (any 200 µm x 200 µm box)	85%
D50.4	M5 max global density (5 mm x 5 mm chip)	75%



51 Josephson Junction Counter Electrode Layer (J5)

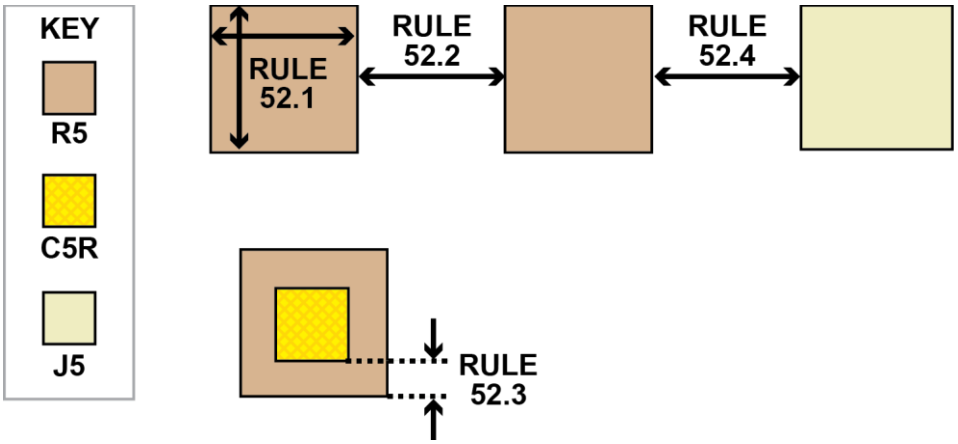
Rule	Description	Value
51.1	J5 min size (diameter if drawn as circle)	0.7 μm
51.2	J5 to J5 min space (on the same M5)	1.1 μm
51.3	J5 max size	3.0 μm
51.4	J5 min space to I5	0.7 μm
51.5	"circular" Manhattan-shape (only supported JJ shape)	Required
51.6	J5 min overlap by M4	0.5 μm
51.7	J5 min surround of C5J	0.1 μm
51.8	J5 min distance to contact (wire bonding) pads	20 μm
D51.1	J5 min density (any 200 μm x 200 μm box)	2%
D51.2	J5 recommended min density (any 200 μm x 200 μm box)	5%
D51.3	J5 max local density (any 200 μm x 200 μm box)	20%
D51.4	J5 max global density (5 mm x 5 mm chip)	20%



52 Lateral Resistor Layer (R5)

Rule	Description	Value
52.1	R5 min size	0.5 μm
52.2	R5 to R5 min space	0.5 μm
52.3	R5 min surround of C5R**	0.25 μm
52.4	R5 to J5 min space	0.4 μm
D52.1	R5 min density (any 200 μm x 200 μm box)	0%
D52.2	R5 max local density (any 200 μm x 200 μm box)	25%
D52.3	R5 max global density (5 mm x 5 mm chip)	25%

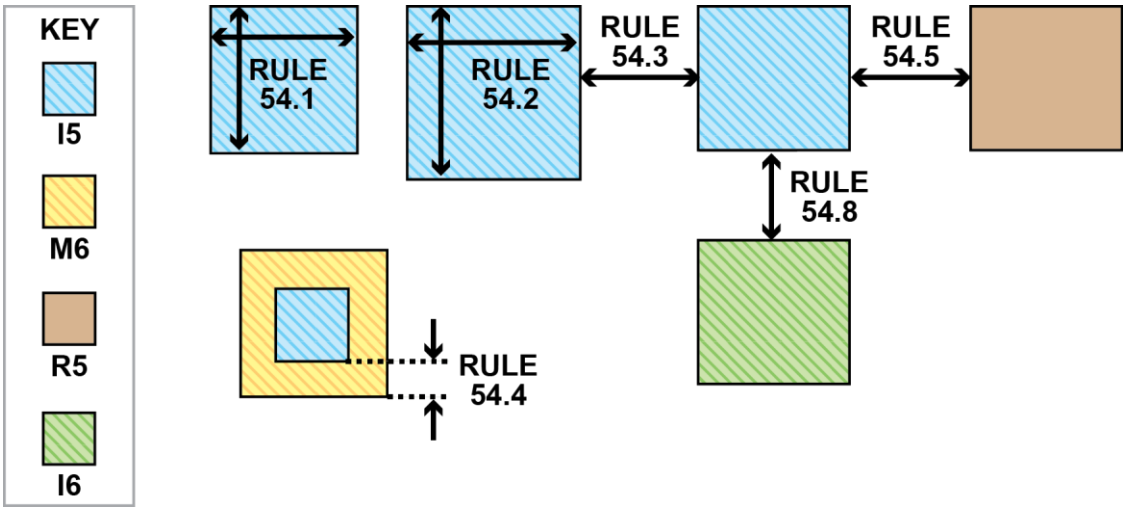
**See Section 2 “Resistors” for alternative resistor layout



54 Via Between Metal 5 and Metal 6 (I5)

Rule	Description	Value (µm)
54.1	I5 min size	0.7
54.2	I5 max size	1.2
54.3	I5 to I5 min space	0.7
54.4	I5 min surround by M6	0.35
54.5	I5 min space to R5	0.5
54.6	I5 overlap of R5	prohibited
54.7	I5 partial overlap with I6	prohibited
54.8	I5 to non-overlapping I6 min space	1.0
54.9	I5 stacking on I4	prohibited
D54.1	I5 min density (any 200 µm x 200 µm box)	0%
D54.2	I5 max local density (any 200 µm x 200 µm box)	25%
D54.3	I5 max global density (5 mm x 5 mm chip)	25%

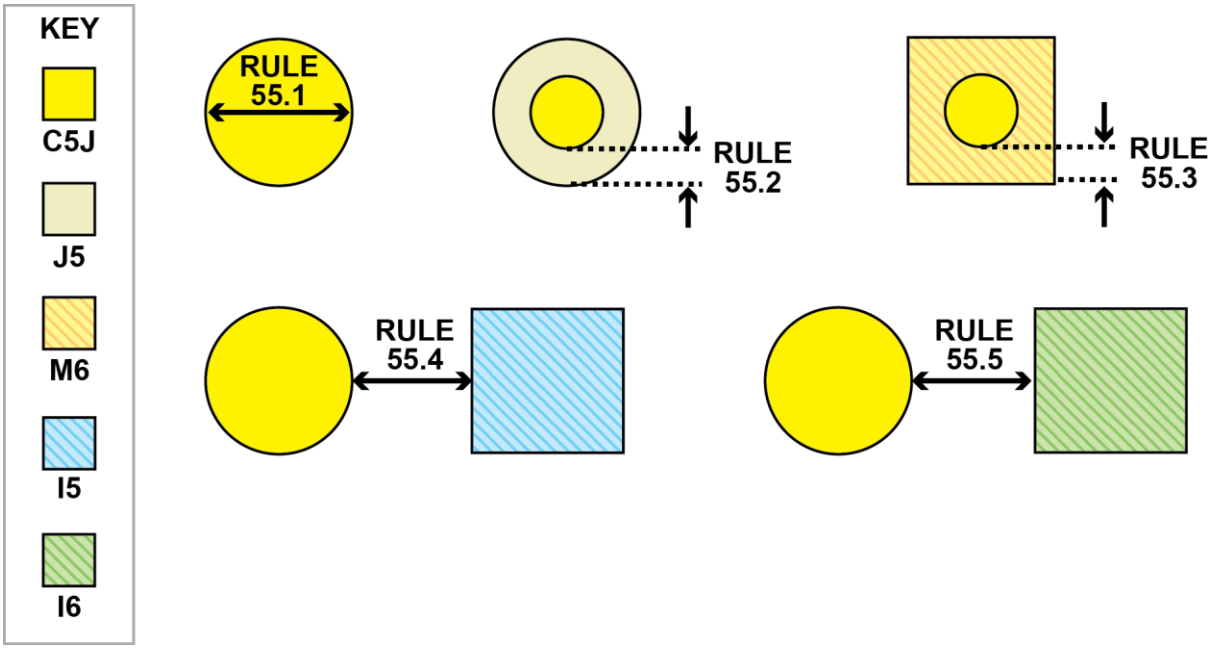
I5 via can be square or rectangular.



55 ContactLayer to J5 (C5J)

Rule	Description	Value
55.1	C5J min size	0.5 μm
55.2	C5J min surround by J5	0.1 μm
55.3	C5J min surround by M6	0.35 μm
55.4	C5J min space to I5 (on the same node)	0.5 μm
55.5	C5J to non-overlapping I6 min space	0.5 μm

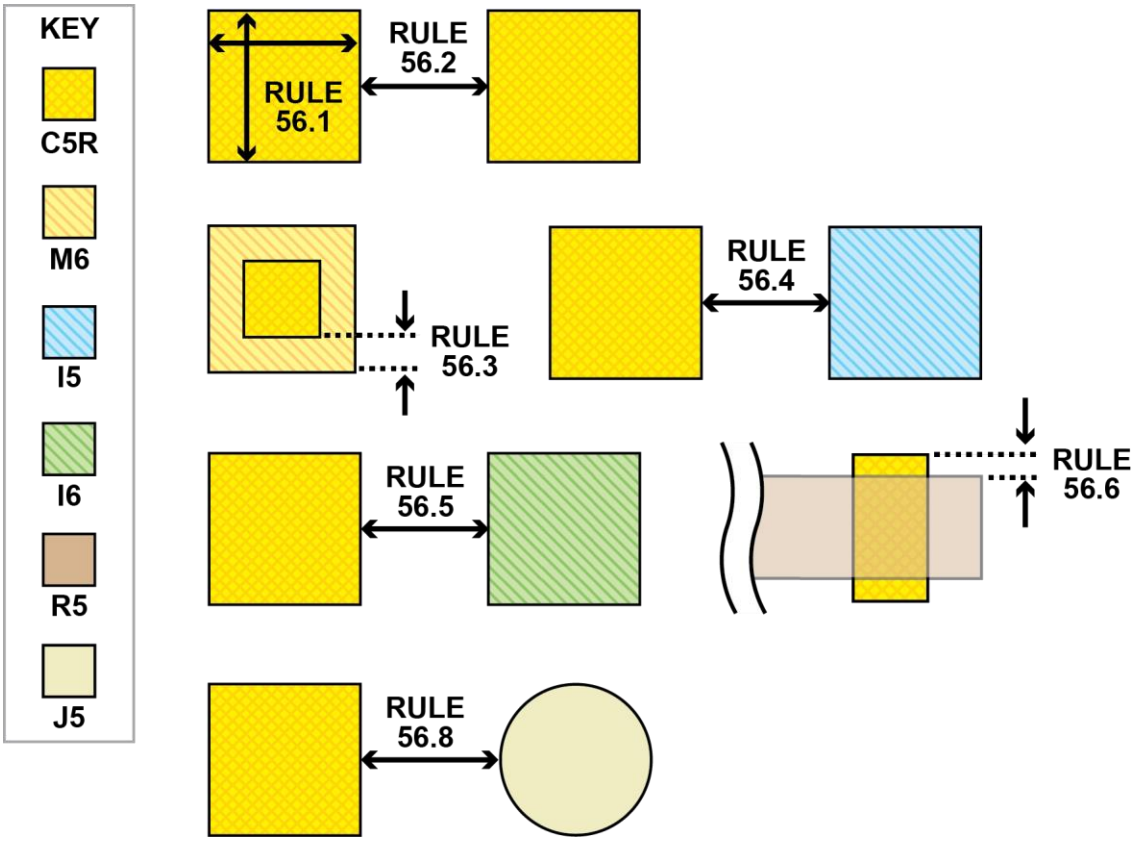
C5J contact must correspond to the shape of J5.
**See Section 2 "Vias" for discussion of overlapping I6 and C5J



56 Contact Layer to R5 (C5R)

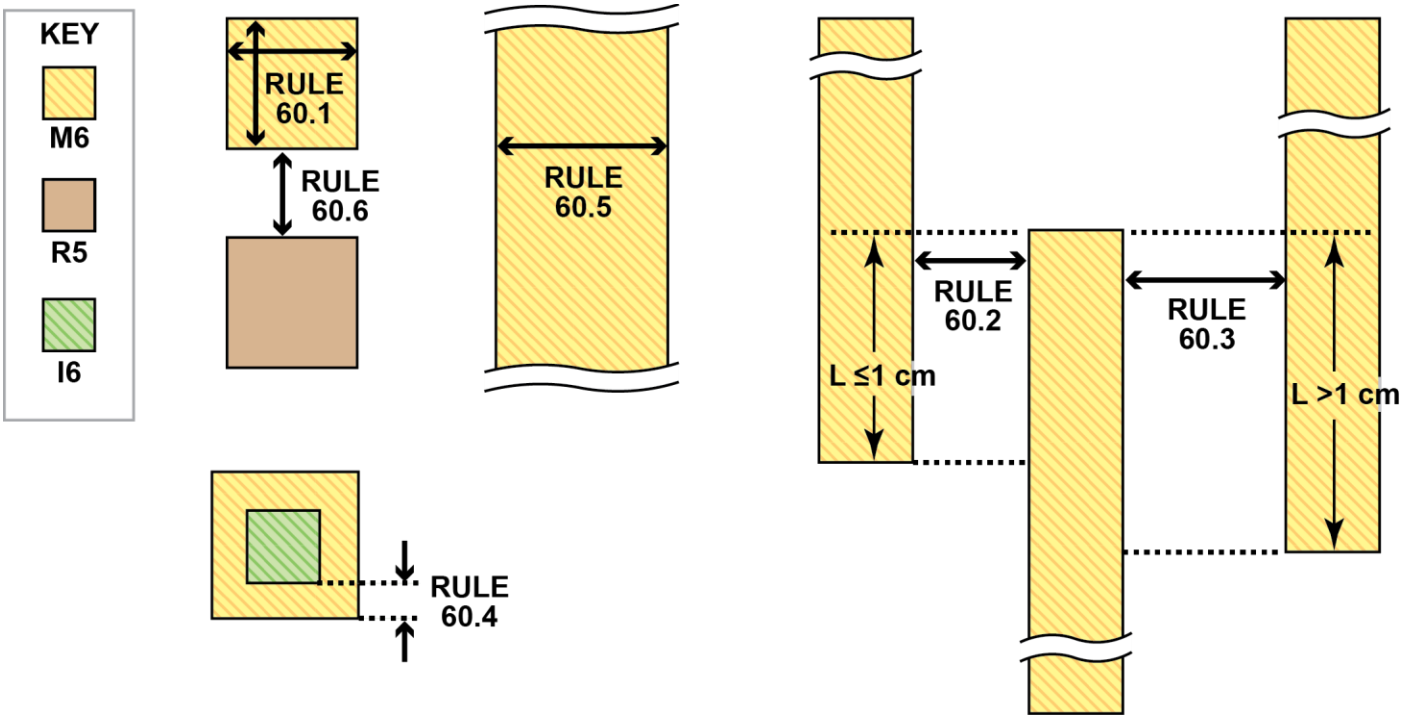
Rule	Description	Value
56.1	C5R min size	0.5 μm
56.2	C5R to C5R min space	0.7 μm
56.3	C5R min surround by M6	0.35 μm
56.4	C5R min space to I5 (on the same node)	0.5 μm
56.5	C5R to non-overlapping I6 min space**	0.5 μm
56.6	C5R max surround of R5 on a side (only for alternative resistor design, see Sec. 2)	0.05 μm
56.7	C5R overlap of M5 edges	Prohibited
56.8	C5R min space to J5	0.5 μm

C5R contact can be square or rectangular.
**See Section 2 "Vias" for discussion of overlapping I6 and C5R



60 Metal 6 Layer (M6)

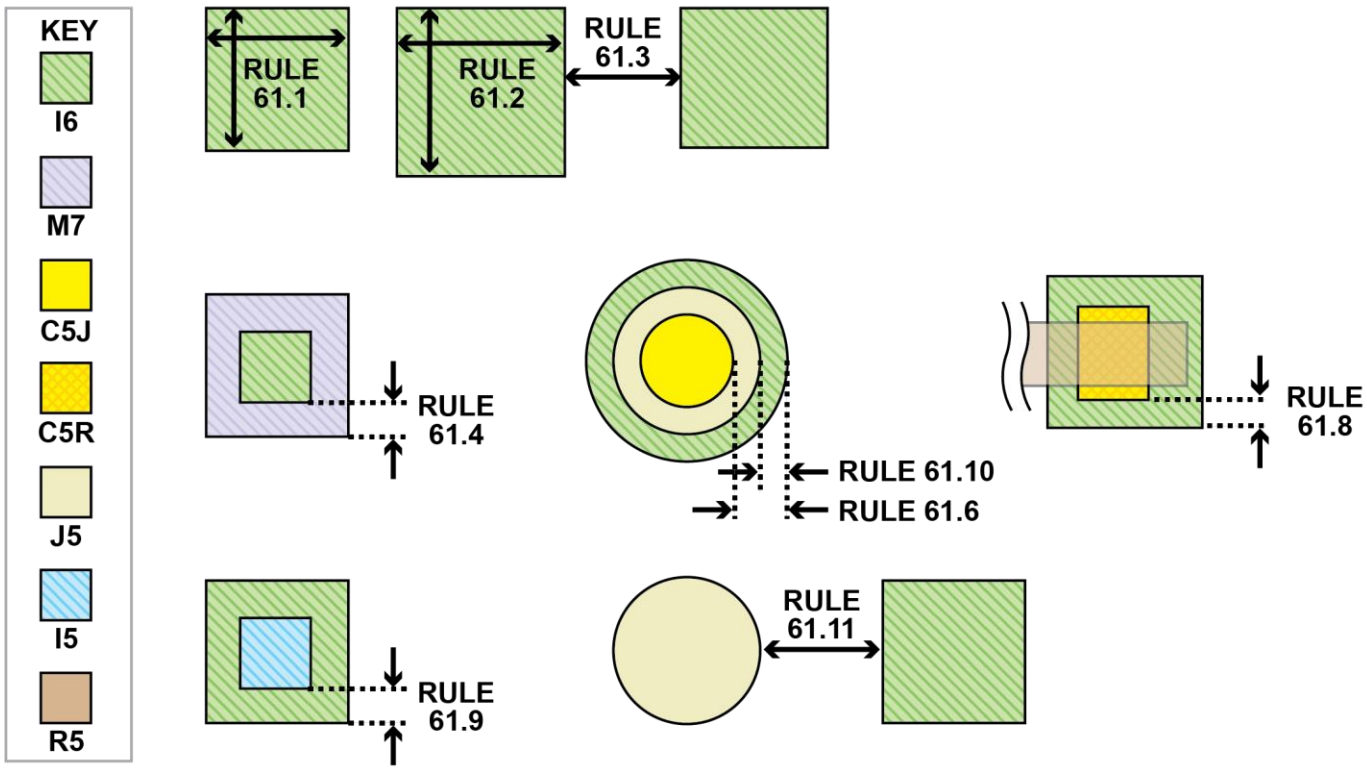
Rule	Description	Value
60.1	M6 min size	0.5 μm
60.2	M6 to M6 min space for L ≤ 1 cm (L = length of gap between two adjacent M6 features)	0.7 μm
60.3	M6 to M6 min space for L > 1 cm	1.0 μm
60.4	M6 min surround of I6	0.35 μm
60.5	M6 max width (except for pads)	20.0 μm
60.6	M6 space to unrelated R5	0.7 μm
D60.1	M6 min density (any 200 μm x 200 μm box)	15%
D60.2	M6 recommended min density (any 200 μm x 200 μm box)	35%
D60.3	M6 max local density (any 200 μm x 200 μm box)	85%
D60.4	M6 max global density (5 mm x 5 mm chip)	80%



61 Via between M6 and M7 (I6)

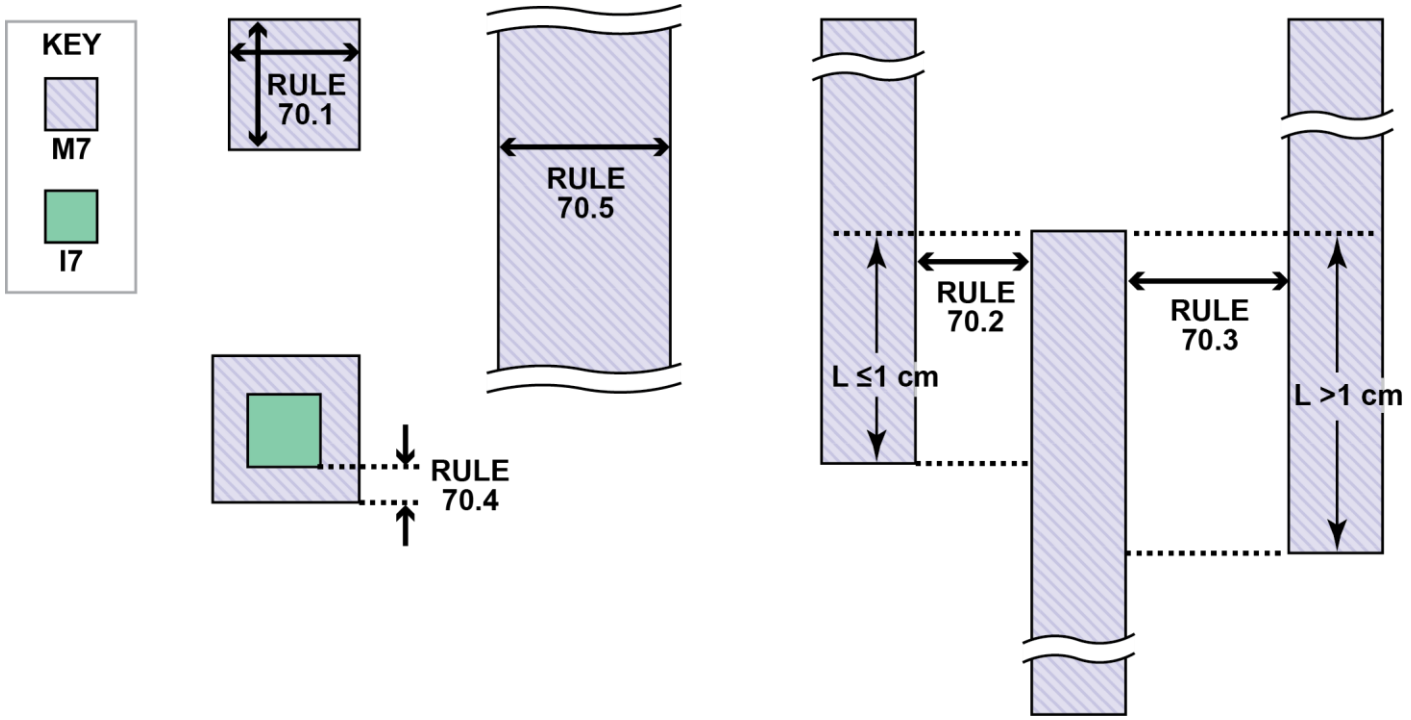
Rule	Description	Value
61.1	I6 min size	0.7 µm
61.2	I6 max size	2.0 µm
61.3	I6 to I6 min space	0.7 µm
61.4	I6 min surround by M7	0.35 µm
61.5	I6 stacking on C5J on J5 is allowed as an exception	
61.6	I6 min surround of C5J over J5	0.30 µm
61.7	I6 stacking on C5R on R5 is allowed as an exception	
61.8	I6 min surround of C5R over R5 per side	0.30 µm
61.9	I6 via stacked on I5, min surround of I5*	0.30 µm
61.10	I6 min surround of J5	0.20 µm
61.11	I6 min space to non-overlapping J5	0.40 µm

I6 via can be square, rectangular, or circular.
*See Section 2 "Vias" for special requirements for stacking two expanding vias



70 Metal 7 Sky Plane Layer (M7)

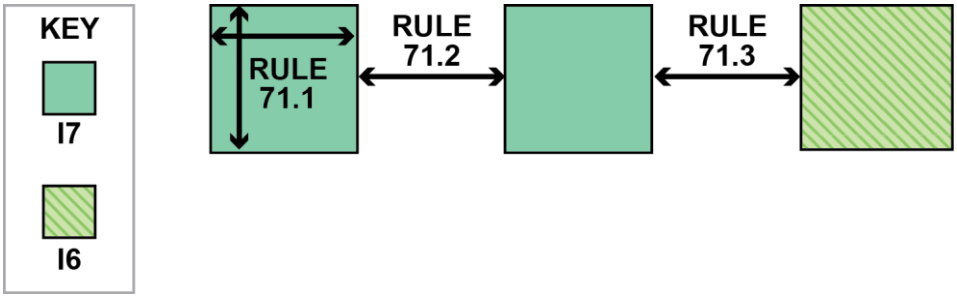
Rule	Description	Value
70.1	M7 min size	0.5 μm
70.2	M7 to M7 min space for L ≤ 1 cm (L = length of gap between two adjacent M7 features)	0.7 μm
70.3	M7 to M7 min space for L > 1 cm	1.0 μm
70.4	M7 min surround of I7	3.0 μm
70.5	M7 max width (except for pads)	20.0 μm
D70.1	M7 min density (any 200 μm x 200 μm box)	0%
D70.2	M7 recommended min density (any 200 μm x 200 μm box)	35%
D70.3	M7 max local density (any 200 μm x 200 μm box)	85%
D70.4	M7 max global density (5 mm x 5 mm chip)	80%



71 Via in Chip Passivation (I7)

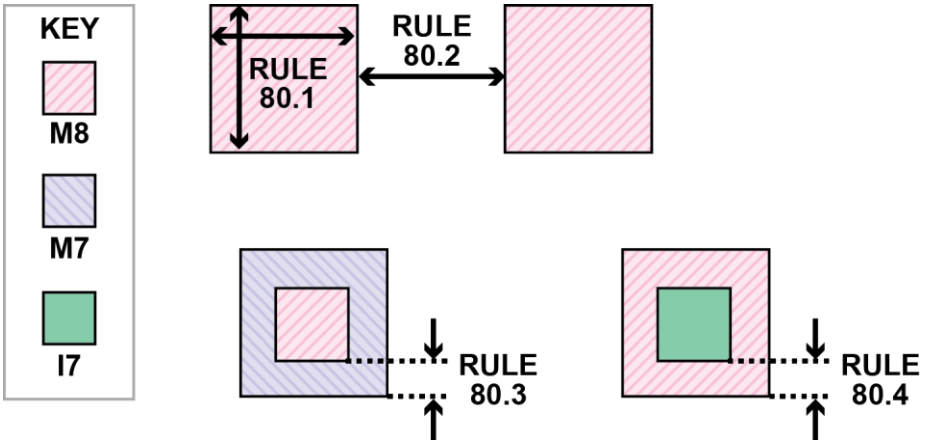
Rule	Description	Value
71.1	I7 min size	5.0 μm
71.2	I7 to I7 min space	3.0 μm
71.3	I7 to non-overlapping I6 min space*	1.0 μm
D71.1	I7 max global density (5 mm x 5 mm chip)	25%

I7 via can be square or rectangular.
*See Section 2 "Vias" for special requirements for stacking two expanding vias



80 Metal 8 Pad Layer (M8)

Rule	Description	Value
80.1	M8 min size	10.0 µm
80.2	M8 to M8 min space	10.0 µm
80.3	M8 min surround by M7	3.0 µm
80.4	M8 surround of I7	3.0 µm

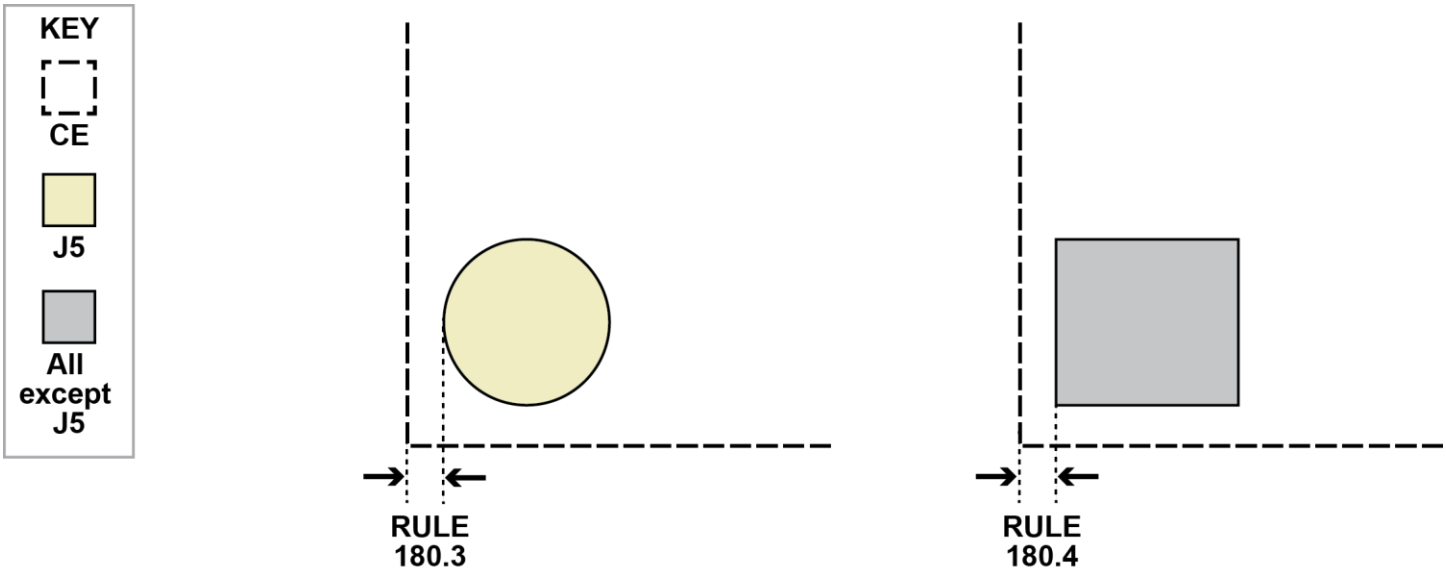


177 NOFILL

NOFILL suppresses automatic fill generation on all mask layers. In regions not covered by **NOFILL**, fill structures are automatically generated by MIT LL to force compliance with layer density rules. When **NOFILL** is used, the designer takes responsibility for all layer density specifications in that region of use. Designs that use **NOFILL** must meet all density constraints after application of the automatic fill generation routine. Each metal, M0, M1, …. may individually have fill blocked in a region with M0 nofill, M1 nofill, etc.

180 Chip Edge Layer (CE)

Rule	Description	Value
180.1	One CE shape must surround all design shapes	Required
180.2	CE must be a rectangle	Required
180.3	CE min extension beyond J5	160 µm
180.4	CE min extension beyond all design shapes except J5	150 µm



182 TEXT

191 Flag Inductor (DEVL)

DEVL indicates the device is an inductor for verification and simulation.

192 Flag Inductor (DEVC)

DEVC indicates the device is a capacitor for verification and simulation.

5. THERMAL DESIGN RULES

Many SFQ circuits use resistors and resistive dividers for distributing DC bias currents and RF impedance matching. These resistors are in direct contact with superconducting wiring in M6 layers through C5R vias. Heat dissipated in the resistors increases the local temperature and decreases the critical current of superconducting wires and JJs, which in extreme cases can turn the junctions and wires into the normal state. This should be avoided by a proper sizing of the resistors, vias, and wires, and proper spacing of high-current-carrying resistors and other circuit elements sensitive to temperature increase. Thermal constraints for the maximum sustainable current though a contact from C5R to R5 depends on width, absolute maximum values are given in Table 5 below. Resistor contacts should be sized such that some margin is allowed for the design current to be safely supplied through the resistor contact.

Table 5. Thermal Design Requirements

Rule	R_s = 2 Ω/□	R_s = 6 Ω/□
Maximum current per width of C5R-R5 contact (chip submerged in liquid helium)	2 mA/μm	0.6 mA/μm

6. DEVICE MODELS

The following subcircuit model and model card, provided in Cadence Spectre format, may be used to simulate JJ devices in the SFQ5eg process. This model corresponds to J_C=100 uA/μm² and I_{crit}=0.0001 A.

```
subckt model_jj (TOP BOTTOM)
        parameters ic_v=0 ic_phase=0 mfactor=1 d=700n
        parameters process_bias_cons1=0.250
        parameters process_bias_cons2=0.020
        parameters dw=pow(((d/1e-6)*(d/1e-6)-process_bias_cons1*process_bias_cons1),1/2)-process_bias_cons2
        parameters area_calc=3.141593*(dw/2.000)*(dw/2.000)
        J0 (TOP BOTTOM) jj_wr_rp area=area_calc ic_v=ic_v ic_phase=ic_phase mfactor=mfactor
ends

model jj_wr_rp jj
        +ic_v=0          ic_phase=0       pijj=0
        +cct=1           tsfactor=0.2     rtype=1
        +area=1          icrit=0.0001      cap=7e-14
        +vgap=0.0028     delv=8e-05       rsub=75
        +rnorm=4.25      vshunt=0          icfct=0.785398
        +vdpbak=50100        enable_dcres=1    version=1.7
```

7. LAYOUT ACCEPTANCE REQUIREMENTS

Use of SFQ5eg Design Rules and Acceptance Requirements

The requirements outlined in this section are for purposes of example only. All designs to be submitted for fabrication must be designed and submitted according to the process-specific design rules and requirements provided for the target technology.

Design Grid

Most layers require shapes to be drawn on a 50 nm grid, as shown in Table 6. Grid checks are of particular importance for design signoff and should be incorporated into routine DRC checking.

Table 6. Layer-by-Layer Grid Requirements

Layer Name	GDSII Layer	Grid Size (nm)
M0	1	50
I0	2	50
L0	3	50
C0	4	50
M1	10	50
I1	11	50
M2	20	50
I2	21	50
M3	30	50
I3	31	50
M4	40	50
I4	41	50
M5	50	50
J5	51	50
R5	52	50
I5	54	50
C5J	55	50
C5R	56	50
M6	60	50
I6	61	50
M7	70	50

Layer Name	GDSII Layer	Grid Size (nm)
I7	71	50
M8	80	500
NOFILL	177	100
CE	180	50
TEXT	182	

Layout Database Format

GDSII is the required format for all layout submissions. A list of GDSII layer numbers is included in Table 6.

Mask Preparation Procedure

The designs should be arranged onto 5-mm by 5-mm chips. All circuit structures should be at least 150 µm away from the border of the 5-mm chip. The delivered chip sizes for the process are 5000 µm by 5000 µm ±20 µm, and 10150 µm by 10150 µm ±20 µm. The maximum possible chip size is 20450 µm x 20450 µm. Please coordinate with MIT LL to determine the chip size and how many chips can be made available for your designs.

Fill will be generated by MIT LL on all layers to aid in the CMP and other processing steps. Designers may use their own fill structures inside the circuits in order to reach the layer densities specified in Section 4 density rules. MIT LL-added fill is no closer than 6 µm to the circuit traces. It is recommended to use "no fill" regions (GDS #177), if necessary, to mark active parts of the circuit where an external (MIT LL) fill is not desired. We recommend that at least one dimension (width or length) of a "no fill" region not exceed 200 µm. Since we cannot fill in within the no-fill zones, we require generating the "internal" fill inside the active circuit area to maintain a uniform metal and Josephson junction densities specified in Section 4 density rules. We strongly recommend maintaining a uniform density of JJs in the circuits and place "dummy" (unconnected) junctions (M4/M5/J5) in the sparse areas. It is recommended to keep the average distance between JJs to about 5-6 µm. The "dummy" junctions used in the internal fill structures do not need to have a C5J contact. The fill junctions can be circular, rectangular, of square. We presently target a metal density on J5 layer of about 6%. "Dummy" junction structures can also be used to generate the required densities.

The minimum metal density on metal layers, except L0, J5 and R5, must be 15%. If any metal layer is not used in the active part of the circuit (a no-fill zone), please generate an internal fill to provide a minimum metal density of at least 15%. We presently target a metal density on all wiring layers of ~ 35%. The average metal density on each layer must not exceed 80% to prevent potential issues with CMP dielectric planarization and robust end-point detection during metal etching. Metal with widths exceeding 20 µm should be slotted to meet density requirements.

In some cases a large ground plane may be required. Please note that, in general, a dielectric thickness on top of metal plates larger than ~ 100 µm x 100 µm may deviate (be larger) from the thicknesses specified in the design rules. The difference may reach ~ 10%. In cases of large ground planes with a low density of moats we do not recommend placing dielectric-thickness-sensitive structures (*e.g.*, inductors and capacitors) near the edges (within ~ 10 µm) of these ground planes.

Contact Information

Contributor contact information must accompany all submissions to allow follow-up as required.

Disclaimer

MIT LL reserves the right to modify the Design Guide at any time. Designs must be made compliant with all design rules.

8. REFERENCES

[1] S.K. Tolpygo, V. Bolkhovsky, T. Weir, L.M. Johnson, W.D. Oliver, and M.A. Gouker, "Deep sub-micron stud-via technology of superconductor VLSI circuits," Supercond. Sci. Technol., vol. 27, 025016, 2014. Doi: 10.1088/0953-2048/27/2/025016

[2] S.K. Tolpygo, V. Bolkhovsky, T. Weir, L.M. Johnson, M.A. Gouker, and W.D. Oliver, "Fabrication and properties of fully-planarized, deep-submicron Nb/Al-AlOx/Nb Josephson junctions for VLSI circuits," IEEE Trans. Appl. Supercond., vol. 25, no. 3, , June 2015. Doi: 10.1109/TASC.2014.2374

9. REVISION HISTORY

Rev. 1 (Nov 2020)

Initial revision, based primarily on the SFQ5ee process