PAPER • OPEN ACCESS

Evaluation of flux trapping moat position on AQFP cell performance

To cite this article: Coenrad J Fourie et al 2021 J. Phys.: Conf. Ser. 1975 012027

View the <u>article online</u> for updates and enhancements.



Fundamentals of Electrochemistry: Basic Theory and Kinetic Methods Instructed by: Dr. James Noël Sun, Sept 19 & Mon, Sept 20 at 12h–15h ET

Register early and save!



1975 (2021) 012027

doi:10.1088/1742-6596/1975/1/012027

Evaluation of flux trapping moat position on AQFP cell performance

Coenrad J Fourie¹, Naoki Takeuchi², Kyle Jackman¹ and Nobuyuki Yoshikawa³

E-mail: coenrad@sun.ac.za

Abstract. With recent advances in InductEx and the TetraHenry numerical engine, it is now possible to analyze the coupling of trapped flux in moats to superconductor circuit structures. Here we show the analysis of moat position in the layout of an adiabatic quantum-flux-parametron (AQFP) buffer cell on the coupling to critical inductors such as the load inductor. This inductor is often carefully laid out to balance current flow and cancel out stray coupling between clock and dc current excitation lines. We investigate the effect of trapped flux that couples asymmetrically to the circuit—either due to the moat position and shape or due to only one of a symmetrical duo of moats being filled with a trapped fluxon—on circuit operating margin and performance. We conclude with suggestions on moat placement to reduce the chances of circuit failure when fluxons are trapped in the moats.

1. Introduction

Flux trapping in type-II superconductor thin films, such as the ground planes of niobium-based integrated circuits, has long been known to degrade circuit operating margins [1]. Moats are used as low energy flux trapping locations [2] to lower the probality of Pearl vortex formation [3] in critical circuit structures such as Josephson junctions.

SQUID microscope imaging of fluxons trapped in thin films and moats [4, 5, 6, 7] has helped superconductor integrated circuit designers understand how fluxons are attracted to moats.

Recently, new methods were developed to analyse the coupling of fluxons in superconducting holes to superconducting structures in a circuit layout [8, 9] and incorporated in InductEx [10] and TetraHenry [11]. The phase-based circuit simulator JoSIM [12] was also developed to simulate the compact simulation models of trapped fluxons in superconductor circuit simulations. The extraction tools, compact simulation models and JoSIM engine were validated through experimental investigation of SQUIDs coupled to different moat configurations [13].

With the tools validated, investigations were done on the coupling between fluxons in different moats and SQUID loop inductors [14], and it was shown that fluxons trapped in moats induce currents in superconductor circuit loops that alter Josephson junction bias points and can significantly degrade the operational margins of such circuits.

¹Department of Electrical and Electronic Engineering, Stellenbosch University, Banghoek Road, Stellenbosch 7600, South Africa

²Institute of Advanced Sciences, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan

³Department of Electrical and Computer Engineering, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan

Content from this work may be used under the terms of the Creative Commons Attribution 3.0 licence. Any further distribution of this work must maintain attribution to the author(s) and the title of the work, journal citation and DOI.

1975 (2021) 012027

doi:10.1088/1742-6596/1975/1/012027

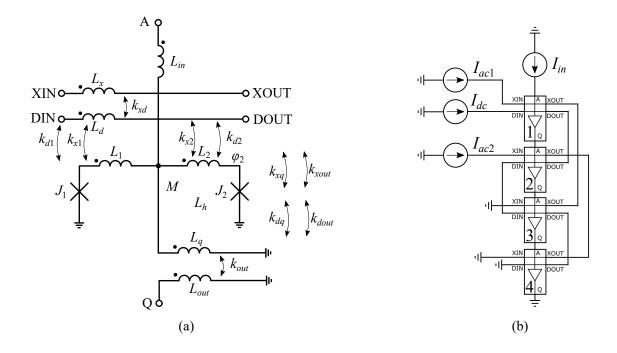


Figure 1. AQFP buffer cell (a) schematic and (b) simulation test circuit.

In this work we investigate the effects of fluxons trapped in moats near adiabatic quantum-flux-parametron (AQFP) cells on circuit operation, and draw conclusions the effectiveness of several moat configurations.

2. Adiabatic Quantum Flux Parametron test circuit

2.1. AQFP buffer simulation

For this investigation we analysed a standard AQFP buffer cell [15], for which the circuit schematic is shown in Figure 1(a). A cascaded test circuit was created for simulation, as shown in Figure 1(b), with ac clock sources, a dc bias and input signal applied. The second cell (labelled "2") is subjected to flux trapping in moats.

The AQFP buffer cell layout is taken from the cell library for the $10\,\mathrm{kA\,cm^{-2}}$ high-speed standard process provided by the National Institute of Advanced Industrial Science and Technology (AIST) in Japan, as presented in [16]. Several most layout configurations were implemented, labelled from A1 to I2 as shown in Figure 2.

Circuit parameters are extracted from the layout with InductEx to account for all significant mutual inductance (the layout marked for extraction in InductEx is shown in Figure 4), and simulation was done with JoSIM [12] because it allows phase-based simulation that is a requirement for compact models that include fluxons on moats. The simulation results for the A circuit are shown in Figure 3(a) for no fluxons in any moat, and in Figure 3(b) when there are three fluxons (oriented upwards from the chip surface) in moat A2. The nominal circuit, without any fluxons in moats, acts as a buffer chain that propagates high inputs from input current I_{in} to the output of each buffer at I_{Q1} to I_{Q4} . With three fluxons trapped in moat A2, buffer 2 fails to produce sufficient output current to drive buffer 3, so that the outputs of buffers 3 and 4 remain low.

1975 (2021) 012027

doi:10.1088/1742-6596/1975/1/012027

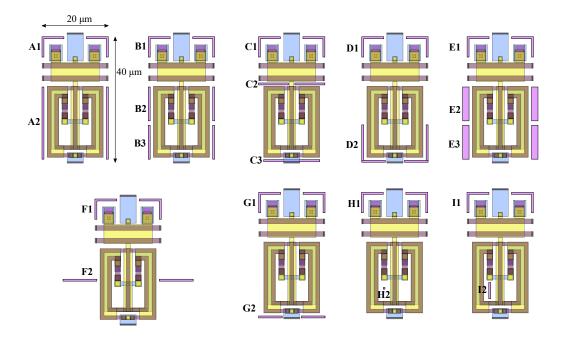


Figure 2. AQFP buffer cell layout with various ground plane moat options, labelled from A1 to I2.

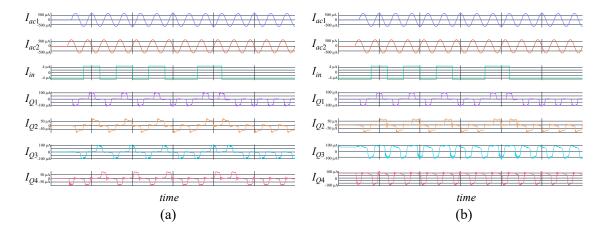


Figure 3. JoSIM simulation result of AQFP buffer chain with (a) no fluxons in any moat showing correct operation and (b) three fluxons in moat A2 of buffer 2 showing failure to switch buffers 3 and 4.

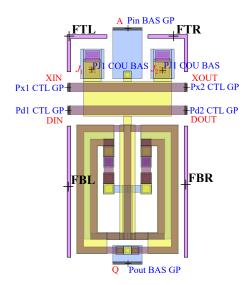
2.2. AQFP buffer layout and InductEx model

The AQFP buffer layout for the AIST HSTP process is shown in Figure 4, labelled for inductance extraction with InductEx. Moats are included in the extraction with "F" labels in every moat.

The moats under investigation are shown in Figure 2. Due to symmetry, we only consider moats to the left of each layout. Moats A1 and A2 represent the typical configuration. Here we also investigated shorter moats B2 and B3 parallel to the output transformer and moats C2 and C3 that try to limit the asymmetry with the output transformer. Moat D2 is an attempt to lessen the asymmetry of B2, moats E2 and E3 are wider to increase moat inductance and reduce the amplitude of the circulating current due to a trapped fluxon, moat F2 is perpendicular to the

1975 (2021) 012027

doi:10.1088/1742-6596/1975/1/012027



- 6.2e+12
- 2e+12
- 1e+12
- 2e+12
- 1e+12
- 2e+11
- 2e+11
- 2e+11
- 2e+10
- 2e

Figure 4. AQFP buffer layout marked for parameter extraction with InductEx.

Figure 5. InductEx model of the AQFP buffer cell with current distribution generated by a positively oriented fluxon in moat A2.

output transformer to reduce the distance that circulating current flows parallel to the output transformer, and moat G2 is an attempt to reduce the asymmetry with the output transformer. Finally, moat H2 mimics a Pearl vortex inside the output transformer coil, while I2 examines the result of a moat inside the output transformer coil.

3. Simulation results

Rather than examine the change in bias margins for the AQFP buffer cell as a function of the number of fluxons in each moat, we measured the current in the main branches of the AQFP buffer cell when exactly one fluxon of either positive or negative orientation is added to one moat at a time. This provides information on the sensitivity of branch currents to fluxons in the moats. The results are shown in Table 1

We also measured the number of fluxons in each moat that causes the simulation to fail. The lower the number of fluxons for circuit failure, the more sensitive the circuit is to the specific moat. Results are shown in Table 2.

4. Discussion on moat design and placement

We note that moats A1 to I1 protect the Josephson junctions and couple weakly to L_1 , L_2 , L_q and L_{out} .

Moats A2, B2, B3, D2 and G2 couple asymmetrically to L_q and L_{out} and induce significant currents in L_q even when one fluxon is trapped in the moat.

The perpendicular moat F2 exhibits low coupling, and a fishbone structure of parallel moats is thus a good design choice, at the expense of decreased placement density for cells.

Thicker moats E2 and E3 reduce coupling to the circuit with a low area cost, and are preferable to A2 or B2 and B3.

Finally, moats C2, C3, H2 and I2 guarantee circuit failure with one trapped fluxon. From the results for these moats, we can define a fluxon exclusion zone that covers the output transformer $(L_q \text{ and } L_{out})$ and the gap between this transformer and L_1 and L_2 . No moats are allowed in this zone, and Pearl vortex formation must be prevented with nearby moats.

1975 (2021) 012027

doi:10.1088/1742-6596/1975/1/012027

Table 1. Static currents in AQFP buffer cell (with dc bias current applied).

Moat		+9	Φ_0		$-\Phi_0$					
	I_{J1} (μ A)	I_{J2} (μ A)	I_Q (μA)	I_{out} (μA)	I_{J1} (μ A)	I_{J2} (μ A)	I_Q (μA)	I_{out} (μ A)		
A1I1	-49.98	+49.77	-1.68	-0.61	-49.91	+49.99	+0.53	+0.17		
A2	-49.97	+49.82	-1.20	-6.25	-49.54	+50.00	-0.29	+5.74		
B2	-49.90	+49.78	-1.44	-5.84	-49.04	+49.94	-0.23	+5.30		
В3	-49.99	+49.93	-0.85	-6.59	-49.74	+50.00	-0.36	+6.11		
C2	-39.77	+42.66	-10.52	-5.42	-29.94	+20.07	-31.78	+3.79		
C3	-31.78	+41.30	-1.14	+25.91	-42.65	+35.33	-1.60	-26.41		
D2	-49.99	+49.91	-0.91	-6.38	-49.65	+49.99	-0.22	+5.91		
E2	-49.96	+49.77	-1.26	-4.73	-49.95	+49.94	-0.24	+4.29		
E3	-49.98	+49.92	-0.80	-5.33	-49.63	+50.00	-0.32	+4.97		
F2	-49.72	+50.00	-0.36	-2.66	-50.00	+49.89	-0.96	-3.18		
G2	-49.99	+49.78	-1.15	-5.54	-49.62	+49.98	-0.13	+4.99		
H2	-45.97	+42.23	-2.96	+22.71	-42.28	+45.96	+1.58	-23.27		
I2	+19.36	+13.42	-13.92	-1.20	-13.38	-19.86	+12.93	+0.78		

Table 2. Number of fluxons an a moat that causes circuit failure for AQFP buffer.

Moat	A1I1	A2	B2	В3	C2	C3	D2	E2	E3	F2	G2	H2	I2
$+\Phi_0$	+5	+3	+3	+3	+1	+1	-3	+4	+4	+6	+4	+1	+1
$-\Phi_0$	-7	-3	-3	-3	-1	-1	-3	-4	-4	-6	-3	-1	-1

5. Conclusion

We investigated the effects of fluxons in moats on an AQFP buffer cell, and found that moats that couple asymmetrically to the output transformer significantly disturb circuit operation.

Wider moats (covering more surface area) reduce such coupling, and where space is avialable, moats perpendicular to the sides of the transformer coil perform even better. We also showed that flux trapping inside the transformer coil will destroy circuit operation.

Finally it may be worth considering different designs for the output transformer to enable better symmetry to moats while retaining the necessary low coupling from this transformer to other inductors in the circuit.

Acknowledgments

The research is based upon work supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via the U.S. Army Research Office grant W911NF-17-1-0120.

References

- [1] Narayana S, Polyakov Y A and Semenov V K 2009 IEEE Trans. Appl. Supercond. 19 640–643 ISSN 1558-2515
- [2] Semenov V K and Khapaev M M 2016 IEEE Trans. Appl. Supercond. 26 1-10 ISSN 2378-7074
- [3] Pearl J 1964 Appl. Phys. Lett. $\mathbf{5}$ 65–66
- [4] Jeffery M, Van Duzer T, Kirtley J R and Ketchen M B 1995 Appl. Phys. Lett. 67 1769–1771

1975 (2021) 012027

doi:10.1088/1742-6596/1975/1/012027

- [5] Tanaka K, Morooka T, Odawara A, Chinone K, Mawatari Y and Koyanagi M 2000 Appl. Phys. Lett. 77 1677–1679
- [6] Suzuki K, Hosomizu R, Adachi S, Kawabe U and Tanabe K 2003 Phys. C 392-396 1446 1450 ISSN 0921-4534
- [7] Suzuki K, Suzuki H, Adachi S, Utagawa T, Kawabe U and Tanabe K 2002 Phys. C $\bf 378\text{-}381$ 1301 1305 ISSN 0921-4534
- [8] Fourie C J and Jackman K 2019 IEEE Trans. Appl. Supercond. 29 1301004
- [9] Jackman K and Fourie C J 2017 IEEE Trans. Appl. Supercond. 27 1300105
- [10] Fourie C J 2015 IEEE Trans. Appl. Supercond. 25 1300209
- [11] Jackman K and Fourie C J 2016 IEEE Trans. Appl. Supercond. 26 1–5
- [12] Delport J A, Jackman K, l Roux P and Fourie C J 2019 IEEE Trans. Appl. Supercond. 29 1300905
- [13] Jackman K and Fourie C J 2020 Supercond. Sci. Technol. 33 105001
- [14] Fourie C J and Jackman K submitted for publication IEEE Trans. Appl. Supercond.
- [15] Takeuchi N, Suzuki H, Fourie C J and Yoshikawa N submitted for publication, arXiv:200911018 IEEE Trans. Appl. Supercond.
- [16] Takeuchi N, Nagasawa S, China F, Ando T, Hidaka M, Yamanashi Y and Yoshikawa N 2017 Superconductor Science and Technology 30 035002