

Influence of Magnetic Flux Trapped in Moats on Superconducting Integrated Circuit Operation

Yuki Yamanashi , Member, IEEE, Hibiki Imai, and Nobuyuki Yoshikawa , Member, IEEE

Abstract—The influence of a trapped flux quantum in a superconducting ground plane hole, called a moat, on superconducting circuit operation was analyzed. We devised a calculation model to estimate the magnetic flux threading a signal line of a superconducting integrated circuit by the trapped flux quantum in a moat placed near the signal line, by using a conventional inductance extraction tool. Assuming one flux quantum trapped in the moat, the dependence of the magnetic flux threading the signal line on the distance between the moat and the signal line were calculated. We measured the flux linkage by measuring the modulation of the I - V characteristic of a dc-SQUID with a moat near the SQUID implemented by using the 2.5 kA/cm^2 Nb standard process. The measured flux linkage agrees well with the analysis results using the devised calculation model. When the distance between the $1 \mu\text{m} \times 10 \mu\text{m}$ moat and the SQUID, the signal line size of which corresponds to the typical inductance of an adiabatic flux quantum parametron (AQFP) is $1 \mu\text{m}$ and one flux quantum is trapped in the moat, the measured magnetic flux linkage threads the signal line was approximately 1.2% of the flux quantum. This flux linkage induces approximately 4% deterioration of the device margin of the AQFP. The devised calculation model and experimental results provide useful information for designing highly integrated future superconducting integrated circuits.

Index Terms—Flux trapping, moat, single-flux-quantum (SFQ) circuit, quantum flux parametron (QFP).

I. INTRODUCTION

SUPERCONDUCTING circuits can perform logic operations with extremely high energy efficiency compared to semiconductor CMOS integrated circuits [1], [2]. However, because superconducting circuits such as the single-flux-quantum (SFQ) circuit [3], [4] and its modified versions [5]–[9], use the magnetic flux quantum as the information carrier, superconducting circuits are sensitive to external magnetic flux. Magnetic flux trapped inside the superconducting circuit affects the circuit operation [10].

To prevent the influence of undesired magnetic flux trapping, holes in the ground plane of the superconducting circuit, called moats, have been used [11], [12]. By trapping the

magnetic flux quanta in moats that are distant from a critical part of the superconducting circuit, the influence of the trapped magnetic flux can be avoided. So far, the optimum shape and placement of the moats have been experimentally investigated [10], [13]–[19]. Material suitable for the superconducting ground plane has been investigated to efficiently trap the flux quantum in the moat [20]. How the moat attracts the magnetic flux has been theoretically and numerically analyzed [21], [22]. In the previous studies, the influence of the flux quanta trapped in moats on superconducting circuit operation have been ignored. However, to build highly-integrated superconducting circuits by using more advanced fabrication processes, the influence of trapped flux quanta in moats on circuit operation should be of concern because the distance between signal lines and moats can be short. Investigation of the influence of a trapped flux quantum in a moat is also important for high-sensitivity superconducting circuits that use magnetic coupling, such as reciprocal quantum logic [8] and quantum flux parametron (QFP) circuits [9], [23]. Moreover, this investigation is important to determine the practical integration limit of the superconducting circuits.

In this study, a calculation model that estimates the magnetic flux threading signal lines in the superconducting circuit by the trapped flux quantum in the moat from the circuit layout was investigated. Magnetic flux threading signal lines was measured by using a dc-SQUID that has a moat near the signal line. The influence of the trapped flux quantum in the moat on the operation of adiabatic QFP (AQFP) was investigated.

II. NUMERICAL ANALYSIS

The influence of the flux quantum trapped in the moat on the superconducting circuit operation can be estimated by calculating the magnetic flux threading a signal line in the circuit, assuming the existence of a moat where the flux quantum is trapped. To analyze the magnetic flux threading a signal line numerically using conventional electromagnetic analysis, we devised a calculation model. Fig. 1(a) shows the layout, cross-sectional view, and superconducting current distribution caused by the flux trapping in a moat around the moat when one flux quantum is trapped in the moat. Fig. 1(b) shows the layout and cross section of the calculation model corresponding to the layout shown in Fig. 1(a). As shown in Fig. 1(a), the superconducting current in the surface of the ground plane, caused by the trapped flux quantum in the moat, exponentially decays as a function of distance from the edge of the moat according to the London equations [24], [25]. Magnetic flux threading the signal

Manuscript received January 30, 2018; revised April 10, 2018; accepted April 27, 2018. Date of publication May 15, 2018; date of current version June 14, 2018. This work was supported in part by JSPS KAKENHI under Grant JP26220904 and in part by the auspices of the MEXT Program for Promoting the Reform of National Universities. This paper was recommended by Associate Editor R. Cristiano. (Corresponding author: Yuki Yamanashi.)

The authors are with the Department of Electrical and Computer Engineering, Yokohama National University, Yokohama 240-8501, Japan (e-mail: yamanashi-yuki-kr@ynu.ac.jp; imai-hibiki-gk@ynu.jp; nyoshi@ynu.ac.jp).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TASC.2018.2836971

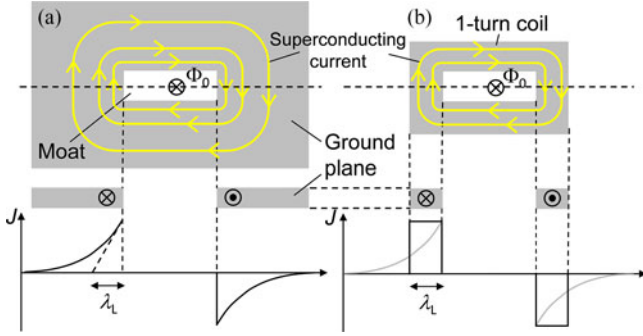


Fig. 1. Layouts and cross sections of (a) a practical moat and (b) our calculation model. Superconducting current distributions (J) along the horizontal dashed line are also shown. λ_L is the London penetration depth of the superconducting ground plane.

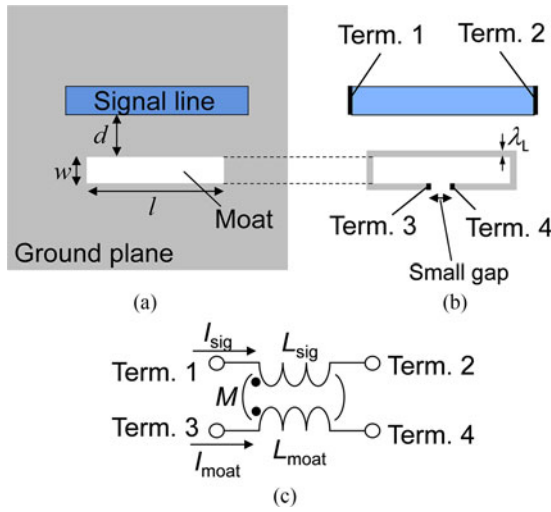


Fig. 2. (a) Layout under analysis, (b) the corresponding calculation model, and (c) the equivalent circuit of the calculation model.

line of the superconducting circuit that is placed near the moat can be determined by calculating the magnetic field distribution around the moat. However, applying the current distribution with exponential decay as shown in Fig. 1(a), in a conventional electromagnetic analysis tool is difficult. In our calculation model, the uniform superconducting current is applied to a one-turn superconducting coil with the width of London penetration of the superconducting penetration depth λ_L by changing λ_L of the one-turn superconducting coil in the electromagnetic calculation.

Fig. 2 shows the layout we analyzed, the corresponding calculation model, and the equivalent circuit of the calculation model. In this analysis, we assumed the use of the National Institute of Advanced Industrial Science and Technology (AIST) 2.5 kA/cm² Nb standard process 2 (AIST-STP2) with four superconducting layers including the ground plane [26], [27]. In this fabrication process, λ_L of each superconducting layer is approximately 80 nm. By making a small gap in the one-turn superconducting coil that has the width of λ_L of the ground plane and the same thickness as the ground plane, the uniform superconducting current can be applied by connecting a current

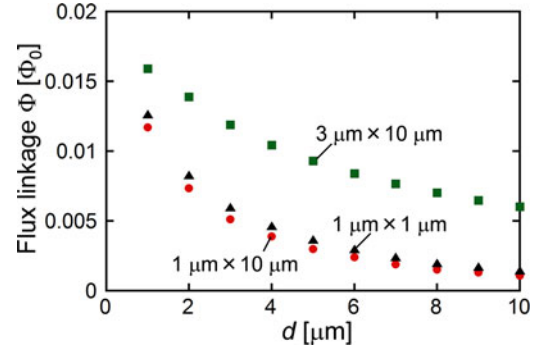


Fig. 3. Calculated dependence of the magnetic flux threading the signal line on the distance between the signal line and the moat d . Flux linkage Φ is normalized by the flux quantum Φ_0 .

source to terminals 3 and 4 in Fig. 2(b) in the electromagnetic analysis tool. The electromagnetic distribution near the surface of the superconductor can be approximated with high accuracy by using this model [28].

Assuming one flux quantum is trapped in the moat with width w and length l , the current I_{moat} flowing in L_{moat} , which is the inductance between terminals 3 and 4 in Fig. 2(b), is represented by

$$I_{\text{moat}} = \frac{\Phi_0}{L_{\text{moat}}} \quad (1)$$

where Φ_0 is the flux quantum. Hence, the flux linkage Φ threading L_{sig} , the inductance of the signal line, can be calculated using mutual inductance between L_{sig} and L_{moat} , M as

$$\Phi = M I_{\text{moat}} = \frac{M}{L_{\text{moat}}} \Phi_0. \quad (2)$$

By substituting L_{moat} and M calculated by the inductance extraction tool into (2), the flux linkage Φ can be calculated. Though magnetic flux threading the signal line by the flux quanta trapped in moats can be calculated by using the latest version of the InductEX software [29], [30], flux linkage can be calculated using a conventional inductance extraction tool such as FastHenry [31] by our calculation model.

We calculated dependence of flux linkage Φ on distance d between the signal line and moats with sizes of $1 \mu\text{m}$ (width) $\times 1 \mu\text{m}$ (length), $1 \mu\text{m} \times 10 \mu\text{m}$, and $3 \mu\text{m} \times 10 \mu\text{m}$ assuming one flux quantum is trapped in moats of various sizes. A $1.2 \mu\text{m} \times 13.2 \mu\text{m}$ signal line composed of the counter (COU) layer of the AIST-STP2 was assumed in our calculation. Therefore, the thickness of the superconducting and insulating layers of the circuits was set to be those of the AIST-STP2. The width and length of the signal line is the typical size of an output inductor of the AQFP buffer cell [32]. We set the small gap between terminals 3 and 4 to be $0.1 \mu\text{m}$. The London penetration depth of the one-turn superconducting coil was set to be $1 \mu\text{m}$ to apply uniform current to the one-turn coil.

We calculated the magnetic flux threading the signal line using this calculation model and the inductance extraction tool InductEX [30]. Fig. 3 shows the calculated dependence of the magnetic flux threading the signal line on the distance between

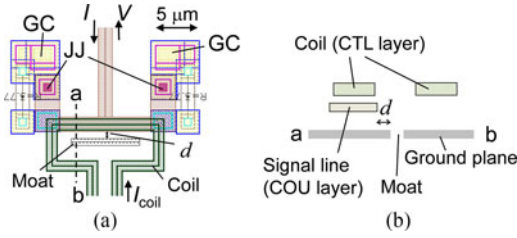


Fig. 4. (a) Layout of a test circuit and (b) its cross section along the vertical dashed line. GC represents the ground contact that connects JJ to the ground plane. Because the ground plane is placed in all area shown in the layout except the area labeled as “moat,” the moat with the size of $1 \mu\text{m} \times 10 \mu\text{m}$ was implemented. The size of the signal line is $1.2 \mu\text{m} \times 12.3 \mu\text{m}$, which is the typical size of the output inductance of the AQFP. Many test circuits with various moat sizes and d values were prepared.

the moat and the signal line. The calculated results indicate that the use of a thin and long moat is effective for reducing the influence of the flux quantum trapped in the moat.

III. EXPERIMENTAL

We experimentally evaluated the magnetic flux threading the signal line when one flux quantum is trapped in the moat. Fig. 4 shows the layout of the test circuit implemented by AIST-STP2 [26], [27]. The dc-SQUID, which was composed of two Josephson junctions (JJs) with a critical current of $200 \mu\text{A}$, was used to measure the flux linkage. The SQUID loop was composed of two JJs, the signal line implemented by the COU layer with size $1.2 \mu\text{m} \times 13.2 \mu\text{m}$, two ground contacts (GCs), and the ground plane. Rectangle-shaped moats of various sizes were placed near the dc-SQUID signal line at distances of $1 \mu\text{m}$, $2 \mu\text{m}$, and $3 \mu\text{m}$. In the measurement sequence, test chips were cooled to 4.2 K in liquid helium. To trap the flux quantum in the moat, an on-chip coil was used. During the chip cooling process, the appropriate dc current was supplied to the on-chip coil composed of the control (CTL) layer. After cooling, the dc current was switched OFF and the I - V characteristic of the dc-SQUID was measured. To repeat the I - V measurements, we employed an on-chip heating technique [33]. By applying a dc voltage of 4 V to the on-chip 50Ω resistor to warm the chip and break its superconductivity, the trapped flux quantum could be removed. The I - V characteristic of the dc-SQUID was measured after turning OFF the dc voltage and the measurement was repeated ten times by repeating this cycle. We compared the I - V characteristics of the dc-SQUID with and without flux trapping in the moat and measured the shift in threshold current (ΔI_{th}). The threshold current was obtained by measuring the minimum applied current value, when the dc-SQUID switches to the finite voltage state using a source meter and a nanovoltmeter.

Fig. 5 shows the dependence of ΔI_{th} of the dc-SQUID with a moat size of $1 \mu\text{m} \times 1 \mu\text{m}$.

Fig. 5 shows the step-shaped ΔI_{th} characteristic. This means we can control the number of flux quanta trapped in the moat by adjusting the dc current applied to the on-chip coil (I_{coil}). In this case, we employed an I_{coil} of 0.4 mA to ensure the trapping of one flux quantum. By measuring ΔI_{th} and the periodicity of the threshold characteristic of the dc-SQUID, we estimated the magnetic flux threading the signal line of the dc-SQUID.

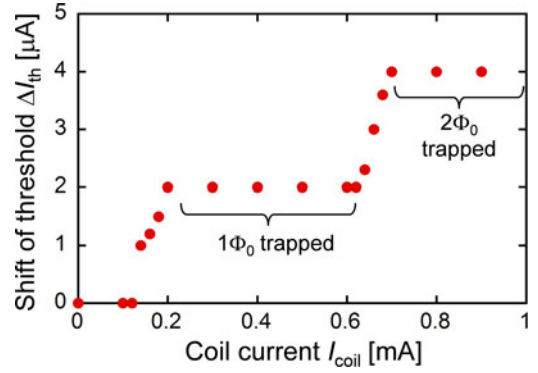


Fig. 5. Example of measured dependence of threshold current shift ΔI_{th} on a dc current applied to the on-chip coil. Measured ΔI_{th} is the average value of 10 measurements.

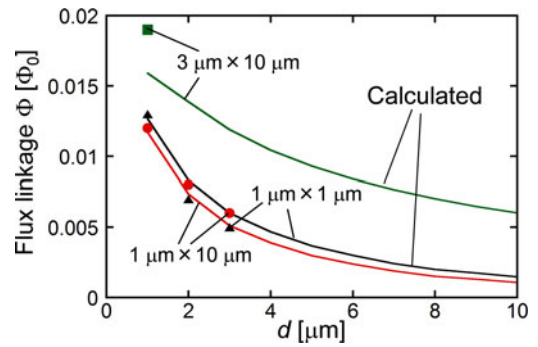


Fig. 6. Dependencies of calculated flux linkage on d for various moat sizes. Squares, triangles, and dots represent the measured flux linkage. Lines correspond to the calculated flux linkage mentioned in Section II and already reported in Fig. 3. Flux linkage Φ is normalized by the flux quantum Φ_0 .

IV. RESULTS AND DISCUSSION

Fig. 6 shows the measured dependencies of the magnetic flux threading the SQUID loop on the distance d between the SQUID and the moat. The calculated dependencies mentioned in Section II are also shown in Fig. 6. Measured results agree well with the calculated results. The discrepancy between the measured and analyzed result is large in the case of the $3 \mu\text{m} \times 10 \mu\text{m}$ moat. This is thought to be caused by the lack of contribution of the magnetic field induced by the superconducting current in the small-gap region in the numerical analysis. When one flux quantum is trapped in the $1 \mu\text{m} \times 10 \mu\text{m}$ moat, which is the typical moat size of the SFQ cell library [34], distant from the signal line by $1 \mu\text{m}$, magnetic flux threading the signal line is approximately 1.2% of the flux quantum.

To estimate influence of the trapped flux quantum in the moat, we simulated the circuit operation of AQFP using the analog circuit simulator JSIM [35]. Fig. 7 shows the equivalent circuit of the AQFP buffer cell. The critical currents of the JJs of the AQFP buffer cell are $50 \mu\text{A}$. Output inductance L_{out} of the AQFP buffer cell was 27.9 pH , which corresponds to the inductance of the $1.2 \mu\text{m} \times 13.2 \mu\text{m}$ COU layer. We evaluated the device margin of the JJs of the AQFP buffer cell assuming 1.2% of flux quantum threading the output inductance L_{out} . Fig. 8 shows the simulated dependence of the JJ device margin of the AQFP cell, which corresponds to tolerate the change of

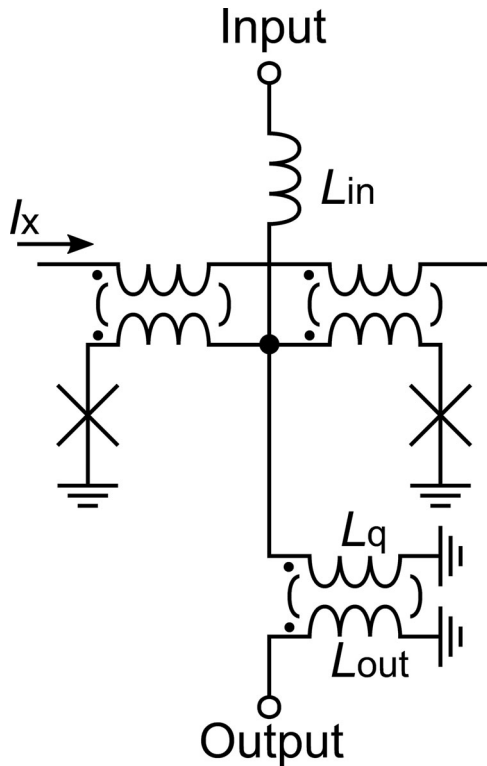


Fig. 7. Equivalent circuit of the AQFP buffer cell. $L_{out} = 27.9$ pH and $I_C = 50$ μ A.

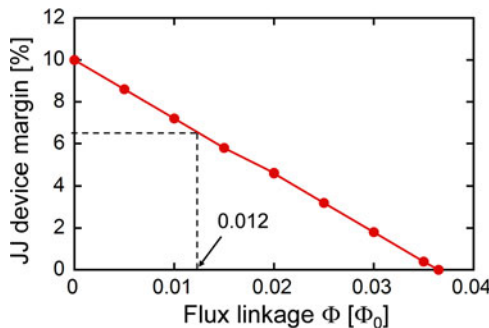


Fig. 8. Dependence of the JJ device margin of the AQFP buffer cell on the magnetic flux threading the output inductance (L_{out}) of the cell.

the critical current of the JJ on the magnetic flux threading the output inductance. When the 1.2% of flux quantum threads the output inductance, the JJ device margin of the AQFP buffer deteriorates to 6.3%, whereas the JJ device margin is 10% when no magnetic flux threads. The existence of 3.5% of the flux quantum is critical for the operation of the AQFP circuit. These results provide a useful design guideline of the moat for not only large-scale AQFP circuits, but also for future superconducting circuits with high integration level.

V. CONCLUSION

We investigated the influence of magnetic flux trapped in a moat on the operation of superconducting circuits. To estimate the influence of the trapped flux quantum, we devised a

calculation model in which conventional inductance extraction tools can be used. We quantitatively measured the magnetic flux threading a signal line in superconducting circuits, caused by the magnetic flux trapped in the moat placed near the signal line. The measured flux linkage agreed well with the analysis results using the calculation model. We estimated the reduction in the device margin of the AQFP buffer for a typical moat size with distance from the signal line.

ACKNOWLEDGMENT

The authors would like to thank Prof. C. J. Fourie for fruitful discussions and providing support for inductance calculation. The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of AIST with the standard process 2 (STP2). The AIST-STP2 is based on the Nb circuit fabrication process developed in ISTE.

REFERENCES

- [1] D. S. Holmes, A. L. Ripple, and M. A. Manheimer, "Energy-efficient superconducting computing—power budgets and requirements," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, Jun. 2013, Art. no. 1701610.
- [2] M. A. Manheimer, "Cryogenic computing complexity program: Phase 1 introduction," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, Jun. 2015, Art. no. 1301704.
- [3] K. Nakajima, H. Mizusawa, H. Sugahara, and Y. Sawada, "Phase mode Josephson computer system" *IEEE Trans. Appl. Supercond.*, vol. 1, no. 2, pp. 29–36, Mar. 1991.
- [4] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz clock-frequency digital systems," *IEEE Trans. Appl. Supercond.*, vol. 1, no. 1, pp. 3–28, Mar. 1991.
- [5] Y. Yamanashi, T. Nishigai, and N. Yoshikawa, "Study of LR-Loading technique for low-power single flux quantum circuits" *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 150–153, Jun. 2007.
- [6] O. A. Mukhanov, "Energy-Efficient single flux quantum technology," *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 760–769, Jun. 2011.
- [7] D. E. Kirichenko, S. Sarwana, and A. F. Kirichenko, "Zero static power dissipation biasing of RSFQ circuits" *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 776–779, Jun. 2011.
- [8] Q. P. Herr, A. Y. Herr, O. T. Oberg, and A. G. Ioannidis, "Ultra-low-power superconductor logic," *J. Appl. Phys.*, vol. 109, no. 10, May 2011, Art. no. 103903.
- [9] N. Takeuchi, D. Ozawa, Y. Yamanashi, and N. Yoshikawa, "An adiabatic quantum flux parametron as an ultra-low-power logic device," *Supercond. Sci. Technol.*, vol. 26, no. 3, Jan. 2013, Art. no. 035010.
- [10] R. P. Robertazzi, I. Siddiqi, and O. Mukhanov, "Flux trapping experiments in single flux quantum shift registers," *IEEE Trans. Appl. Supercond.*, vol. 7, no. 2, pp. 3164–3167, Jun. 1997.
- [11] S. Berman and T. Gheewala, "Moat-guarded Josephson SQUIDS," *IEEE Trans. Magn.*, vol. 19, no. 3, pp. 1160–1164, May 1983.
- [12] M. Jeffery, T. Van Duzer, J. R. Kirtley, and M. B. Ketchen, "Magnetic imaging of moat-guarded superconducting electronics circuits," *Appl. Phys. Lett.*, vol. 67, no. 12, pp. 1769–1771, Sep. 1995.
- [13] K. Suzuki, R. Hosomizu, S. Adachi, U. Kawabe, and K. Tanabe, "Investigation of flux trapping into moats with various moat depths by a scanning SQUID microscope," *Phys. C*, vol. 392–396, pp. 1446–1450, Oct. 2003.
- [14] Y. Polyakov, S. Narayana, and V. K. Semenov, "Flux trapping in superconducting circuits," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 520–525, Jun. 2007.
- [15] S. Narayana, Y. A. Polyakov, and V. K. Semenov, "Evaluation of flux trapping in superconducting circuits," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 640–643, Jun. 2009.
- [16] B. Ebert, T. Ortlev, and F. H. Uhlmann, "Experimental study of the effect of flux trapping on the operation of RSFQ circuits," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 607–610, Jun. 2009.
- [17] K. Fujiwara et al., "Research on effective moat configuration for Nb multi-layer device structure," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 603–606, Jun. 2009.

- [18] Q. P. Herr *et al.*, “Reproducible operating margins on a 72800-device digital superconducting chip,” *Supercond. Sci. Technol.*, vol. 28, no. 12, Dec. 2015, Art. no. 124003.
- [19] V. K. Semenov, Y. A. Polyakov, and S. K. Tolpygo, “AC-Biased shift registers as fabrication process benchmark circuits and flux trapping diagnostic tool,” *IEEE Trans. Appl. Supercond.*, vol. 27, no. 4, Jun. 2017, Art. no. 1301409.
- [20] N. Mitamura, N. Naito, H. Akaike, and A. Fujimaki, “Suppression of magnetic flux trapping by moats formed in NbN ground planes,” *Appl. Phys. Exp.*, vol. 4, no. 1, Dec. 2011, Art. no. 013102.
- [21] V. K. Semenov and M. M. Khapaev, “How moats protect superconductor films from flux trapping,” *IEEE Trans. Appl. Supercond.*, vol. 26, no. 3, Apr. 2016, Art. no. 1300710.
- [22] M. Inoue, S. Mizoguchi, and A. Fujimaki, “Study on the force and potential for the vortex motion around the concave film edge by the numerical calculation,” *IEEE Trans. Appl. Supercond.*, vol. 27, no. 4, Jun. 2017, Art. no. 1501004.
- [23] M. Hosoya *et al.*, “Quantum flux parametron: A single quantum flux device for Josephson supercomputer,” *IEEE Trans. Appl. Supercond.*, vol. 1, no. 2, pp. 77–89, Jun. 1991.
- [24] F. London and H. London, “The electromagnetic equations of the superconductor,” *Proc. Roy. Soc. A*, vol. 149, no. 866, pp. 71–88, Mar. 1935.
- [25] J. Pearl, “Current distribution in superconducting films carrying quantized fluxoids,” *Appl. Phys. Lett.*, vol. 5, no. 4, pp. 65–66, Aug. 1964.
- [26] S. Nagasawa, Y. Hashimoto, H. Numata, and S. Tahara, “A 380 ps, 9.5 mW Josephson 4-Kbit RAM operated at a high bit yield,” *IEEE Trans. Appl. Supercond.*, vol. 5, no. 2, pp. 2447–2452, Jun. 1995.
- [27] M. Hidaka, S. Nagasawa, T. Satoh, K. Hinode, and Y. Kitagawa, “Current status and future prospect of the Nb-based fabrication process for single flux quantum circuits,” *Supercond. Sci. Technol.*, vol. 19, no. 3, pp. S138–S142, Feb. 2006.
- [28] N. Takeuchi, Y. Yamanashi, Y. Saito, and N. Yoshikawa, “3D simulation of superconducting microwave devices with an electromagnetic-field simulator,” *Phys. C*, vol. 496, no. 15–19, pp. 1662–1665, Oct. 2009.
- [29] K. Jackman and C. J. Fourie, “Flux trapping analysis in superconducting circuits” *IEEE Trans. Appl. Supercond.*, vol. 27, no. 4 Jun. 2017, Art. no. 1300105.
- [30] C. J. Fourie, O. Wetzstein, T. Orllepp, and J. Kunert, “Three-dimensional multi-terminal superconductive integrated circuit inductance extraction,” *Supercond. Sci. Technol.*, vol. 24, no. 12, Nov. 2011, Art. no. 125015.
- [31] M. Kamon, M. J. Tsuk, and J. K. White, “FASTHENRY: A multipole-accelerated 3-D inductance extraction program,” *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 9, pp. 1750–1758, Sep. 1994.
- [32] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, “Adiabatic quantum-flux-parametron cell library adopting minimalist design,” *J. Appl. Phys.*, vol. 117, no. 17, May 2015, Art. no. 173912.
- [33] K. Gotoh, N. Fujimaki, T. Imamura, S. Hasuo, and A. Shibatomi, “A method of detrapping magnetic flux in a SQUID sensor using an integrated thin-film heater,” *IEICE Trans. Electron.*, vol. E74-C, no. 7, pp. 2029–2035, Jul. 1991.
- [34] H. Akaike *et al.*, “Design of single flux quantum cells for a 10-Nb-layer process,” *Phys. C*, vol. 496, no. 15–20, pp. 1670–1673, Oct. 2009.
- [35] E. S. Fang and T. Van Duzer, “A Josephson integrated circuit simulator (JSIM) for superconductive electronics application,” in *Proc. Ext. Abstr. 2nd Int. Supercond. Electron. Conf.*, 1989, pp. 407–410.

Yuki Yamanashi received the B.E., M.E., and Ph.D. degrees in electrical and computer engineering from Yokohama National University, Yokohama, Japan, in 2003, 2005, and 2007, respectively.

From 2007 to 2012, he was with the Interdisciplinary Research Center, Yokohama National University. Since 2012, he has been with the Department of Electrical and Computer Engineering, Yokohama National University. His research interests include superconductive circuit design and its applications.

Dr. Yamanashi is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Japan Society of Applied Physics, the Institute of Electrical Engineering of Japan, and Cryogenics and Superconductivity Society of Japan.

Hibiki Imai received the B.E. and M.E. degrees from Yokohama National University, Yokohama, Japan, in 2015 and 2017, respectively.

Since 2017, he has been with Tokyo Electron Ltd., Tokyo, Japan.

Nobuyuki Yoshikawa received the B.E., M.E., and Ph.D. degrees in electrical and computer engineering from Yokohama National University, Yokohama, Japan, in 1984, 1986, and 1989, respectively.

Since 1989, he has been with the Department of Electrical and Computer Engineering, Yokohama National University, where he is currently a Professor. His research interests include superconductive devices and their application in digital and analog circuits. He is also interested in single-electron-tunneling devices, quantum computing devices, and cryo-CMOS devices.

Prof. Yoshikawa is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Japan Society of Applied Physics, and the Institute of Electrical Engineering of Japan.