Adiabatic Quantum-Flux-Parametron: A Tutorial Review

Article *in* IEICE Transactions on Electronics · January 2022

DOI: 10.1587/transele.2021SEP0003

CITATIONS
14

READS
356

5 authors, including:

Christopher Lawrence Ayala
Yokohama National University
48 PUBLICATIONS **696** CITATIONS
SEE PROFILE

Hideo Suzuki
Yokohama National University
73 PUBLICATIONS **553** CITATIONS
SEE PROFILE

Nobuyuki Yoshikawa
Yokohama National University
406 PUBLICATIONS **4,946** CITATIONS
SEE PROFILE

IEICE TRANSACTIONS

on Electronics

DOI:10.1587/transele.2021SEP0003

Publicized:2022/01/19

A PUBLICATION OF THE ELECTRONICS SOCIETY

The Institute of Electronics, Information and Communication Engineers

Kikai-Shinko-Kaikan Bldg., 5-8, Shibakoen 3chome, Minato-ku, TOKYO, 105-0011 JAPAN

INVITED PAPER

Adiabatic Quantum-Flux-Parametron: A Tutorial Review

Naoki TAKEUCHI[†,††a)], ***Member***, **Taiki YAMAE**[†††,††††], **Student *Member***, **Christopher L. AYALA**[††], **Hideo SUZUKI**[††], **and Nobuyuki YOSHIKAWA**[††,†††], ***Members***

SUMMARY The adiabatic quantum-flux-parametron (AQFP) is an energy-efficient superconductor logic element based on the quantum flux parametron. AQFP circuits can operate with energy dissipation near the thermodynamic and quantum limits by maximizing the energy efficiency of adiabatic switching. We have established the design methodology for AQFP logic and developed various energy-efficient systems using AQFP logic, such as a low-power microprocessor, reversible computer, single-photon image sensor, and stochastic electronics. We have thus demonstrated the feasibility of the wide application of AQFP logic in future information and communications technology. In this paper, we present a tutorial review on AQFP logic to provide insights into AQFP circuit technology as an introduction to this research field. We describe the historical background, operating principle, design methodology, and recent progress of AQFP logic.

key words: *QFP, adiabatic logic, low-power, energy-efficient, superconductor digital electronics.*

1. Introduction

The spread of new technologies such as social networking services (SNS), artificial intelligence (AI), and the Internet of things (IoT) has led to a dramatic increase in electricity demand for information and communications technology (ICT), which is expected to reach 20% of global electricity demand by 2030 [1]. This trend indicates that a future information society, such as Society 5.0, where AI and IoT are fully exploited to collect and process huge amounts of data, will require extremely energy-efficient electronics for ICT. Therefore, many types of energy-efficient superconductor logic families have been proposed in the last decade [2–7], which have the potential to operate with less power dissipation than state-of-the-art semiconductor circuits and save energy for data processing. Furthermore, several research groups have reported successful demonstrations of large-scale, energy-efficient superconductor digital circuits [8–10], which indicates the high robustness, as well as the high energy efficiency, of superconductor logic families. Note that these demonstrations were supported by recent advances in fabrication technology for superconductor integrated circuits [11–13].

In this paper, we report a tutorial review on the adiabatic quantum-flux-parametron (AQFP) [5], which is an energy-efficient superconductor logic element based on the quantum flux parametron (QFP) [14, 15]. AQFP circuits can operate with energy dissipation near the thermodynamic and quantum limits [16] due to the energy-efficient switching process, adiabatic switching [17, 18]. We describe the historical background, operating principle, design methodology, and recent progress of AQFP logic to provide insights into AQFP circuit technology, especially for students and those who are new to this research field.

2. Historical Background

The research background of the QFP and AQFP is closely associated with the study of information thermodynamics, such as reversible computing [19, 20]. Since Landauer's discussion on the relation between logical and thermodynamic reversibility in 1961 [21], many researchers have discussed the minimum energy dissipation in computing and the possibility of computers that can operate in a thermodynamically reversible manner (i.e., without energy dissipation). In 1970, Keys and Landauer showed that the logic state of a physical device can be switched without energy dissipation by gradually changing the potential energy shape from a single well to a double well [17], whereas the reset process dissipates some amount of energy. We refer to this switching process as adiabatic switching, referencing the terminology in adiabatic complementary metal–oxide–semiconductor (CMOS) logic [18]. In 1977, Likharev invented a superconductor device that operates via adiabatic switching, the parametric quantron (PQ) [22]. The PQ is an rf superconducting quantum interference device (SQUID) in which the critical current of the Josephson junction is modulated by applying a magnetic flux so that the potential energy shape changes

†The author is with the Research Center for Emerging Computing Technologies, the National Institute of Advanced Industrial Science and Technology (AIST), 1-1-1 Umezono, Tsukuba 305-8568, Japan.
††The authors are with the Institute of Advanced Sciences, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan.
†††The authors are with the Department of Electrical and Computer Engineering, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan.
††††The author is a Research Fellow of Japan Society for the Promotion of Science, 5-3-1 Kojimachi, Chiyoda, Tokyo 102-0083, Japan.
a)E-mail: n-takeuchi@aist.go.jp

gradually. Likharev explored reversible computing based on the PQ [23], but PQ-based circuits have never been demonstrated, for several reasons [24].

Later, Goto invented a more practical adiabatic superconductor device, the QFP [14], inspired by his own previous invention, the parametron [25]. The QFP is an rf SQUID with the Josephson junction replaced with a dc SQUID, the critical current of which can be modulated by a smaller control current than is necessary for the direct modulation of a Josephson junction. Interestingly, Likharev also proposed a similar device as a modified PQ around the same time [26]. In 1986, a five-year national project exploring the possibility of QFP-based computers, "GOTO Quantum Magneto Flux Logic [27]," started in Japan, sponsored by the ERATO program of the Research Development Corporation of Japan (JRDC). This project was led by Goto and achieved many important results [15], such as the demonstration of basic QFP circuits (e.g., shift registers [28, 29] and analog-to-digital converters [30, 31]) and studies on QFP-based reversible computing [32]. Following this project, Hitachi, Ltd. and other research groups continued research on QFP circuits [33–37]. However, in the 90s, rapid single-flux-quantum (RSFQ) logic [38] attracted more attention and became the mainstream of superconductor electronics because of its ultra-high operating speed [39].

In the 2000s, energy became the key limiter of computer performance [40–42], and energy efficiency has been the most important metric in computer design. Also, the increasing power demand for ICT indicates the need for low-power computing, as mentioned in the introduction. Therefore, we revived the QFP and proposed an energy-efficient QFP, the AQFP [5], which is designed to maximize the energy efficiency of adiabatic switching by using optimized circuit parameters and advanced fabrication processes. We have established the design methodology for AQFP logic and recently succeeded in demonstrating a 4-bit microprocessor [10]. We have also developed various systems by exploiting the physical features of the AQFP, such as reversible computers [43, 44], single-photon image sensors [45, 46], and stochastic electronics [47, 48]. This indicates the potential of AQFP logic to be widely used in future ICT.

3. Operating Principle

This section describes the operating principle of the QFP and AQFP, focusing on potential energy and adiabatic switching. We begin by deriving the potential energy of an rf SQUID, since the QFP and AQFP are based on an rf SQUID. We then derive the potential energy of the QFP and show that the QFP can perform adiabatic switching, i.e., the potential energy shape of the QFP changes gradually from a single well to a double well. Lastly, we explore the energy dissipation for adiabatic switching and show that AQFP logic operates with energy dissipation near the thermodynamic and quantum limits by maximizing the energy efficiency of adiabatic switching.

3.1 Potential energy of an rf SQUID

Figure 1 depicts a circuit diagram of an rf SQUID, which comprises a Josephson junction J and an inductor L and is biased by a magnetic flux Φ_b provided by a bias current I_b. The potential energy of the rf SQUID is given by the sum of the energy stored in J (U_j) and that in L

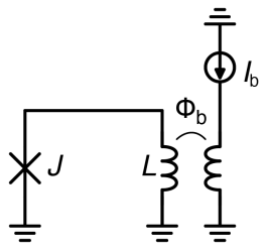


Fig. 1 rf SQUID biased by a magnetic flux Φ_b.

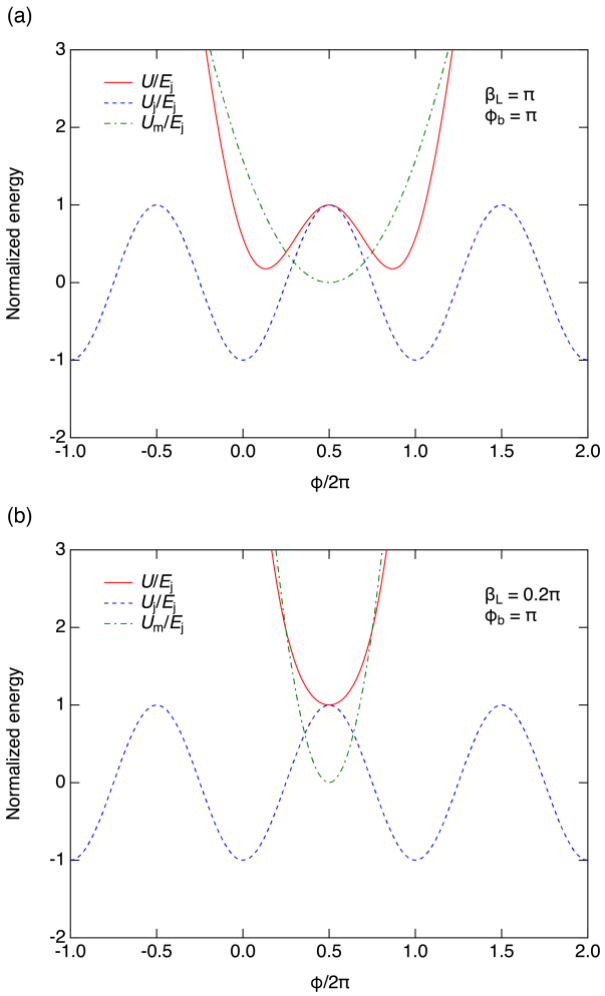


Fig. 2 Potential energy of an rf SQUID for $\Phi_b = 0.5\Phi_0$. (a) Double-well potential formed for $\beta_L = \pi$, (b) single-well potential formed for $\beta_L = 0.2\pi$.

(U_m). U_j and U_m are given as follows: $U_j = -E_j\cos\phi$ and $U_m = E_j\phi_L^2/2\beta_L$, where $E_j = I_c\Phi_0/2\pi$ is the Josephson energy, $\beta_L = 2\pi LI_c/\Phi_0$ is the normalized inductance, ϕ is the phase difference across J, ϕ_L is the normalized flux associated with L, I_c is the critical current of J, and Φ_0 is the flux quantum. According to flux quantization, the relation between the phase difference and magnetic fluxes is given by $\phi = \phi_L + \phi_b$, where $\phi_b = 2\pi\Phi_b/\Phi_0$ is the normalized bias flux; thus, the potential energy U of the rf SQUID is given by:

$$\frac{U}{E_j} = \frac{U_m}{E_j} + \frac{U_j}{E_j} = \frac{(\phi - \phi_b)^2}{2\beta_L} - \cos\phi. \quad (1)$$

This equation shows that a double-well potential is formed for $\phi_b = \pi$ (i.e., $\Phi_b = 0.5\Phi_0$) because U_j is maximized and U_m is minimized at $\phi = \pi$ in ϕ space, as shown in Fig. 2(a), which depicts U_j, U_m, and U as functions of ϕ for $\phi_b = \pi$ and $\beta_L = \pi$. The left-hand well of U corresponds to a counterclockwise current in the rf SQUID and the right-hand well corresponds to a clockwise current. However, this is not always the case. As shown in Fig. 2(b), the potential energy shape is a single well for $\beta_L = 0.2\pi$ under the same bias condition ($\phi_b = \pi$).

Importantly, a comparison between Figs. 2(a) and (b) suggests that the potential energy shape of an rf SQUID can be modulated between a single well and a double well by changing the value of β_L, i.e., an rf SQUID can perform adiabatic switching by gradually changing β_L. Typically, β_L is changed by varying I_c. In the PQ, I_c is directly modulated by applying a magnetic flux to the Josephson junction. In the QFP, the Josephson junction is replaced with a dc SQUID, which works as a Josephson junction with a variable critical current.

3.2 Quantum flux parametron (QFP)

Figure 3 depicts a circuit diagram of the QFP, which comprises a dc SQUID (J_1-L_1-L_2-J_2) and a load inductor L_q. The excitation current I_x applies a magnetic flux $\Phi_{x1} + \Phi_{x2}$ to the dc SQUID, thereby changing its equivalent critical current. In general, the circuit parameters of the QFP are symmetrical, so that $\Phi_x = \Phi_{x1} = \Phi_{x2}$. The input current I_{in} applies a magnetic flux Φ_{in} to L_q and tilts the potential energy so that the QFP switches to the correct logic state. The potential energy of the QFP is given by the sum of the energy stored in J_1, J_2, L_1, L_2, and L_q. The total energy stored in J_1 and J_2 is given by $U_j = E_j(-\cos\phi_1 - \cos\phi_2) = -2E_j\cos\phi_-\cos\phi_+$, where $E_j = I_c\Phi_0/2\pi$, $\phi_- = (\phi_1 - \phi_2)/2$, $\phi_+ = (\phi_1 + \phi_2)/2$, ϕ_1 and ϕ_2 are the phase differences across J_1 and J_2, respectively, and I_c is the critical current of J_1 and J_2. Assuming that L_1 and L_2 are sufficiently small, the energy stored in L_1 and L_2 can be neglected. The energy stored in L_q is given by $U_m = E_j\phi_q^2/2\beta_q$, where $\beta_q = 2\pi L_qI_c/\Phi_0$ and ϕ_q is the normalized flux associated with L_q. According to flux quantization, the relation between the phase differences and magnetic fluxes is given by:

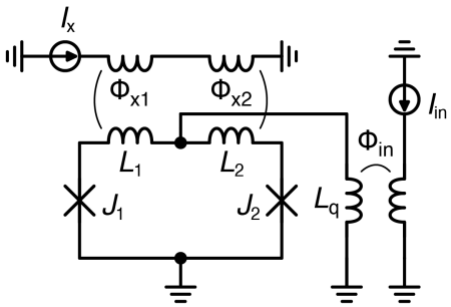


Fig. 3 QFP excited by an excitation current I_x. The input current I_{in} determines which logic state the QFP switches to.

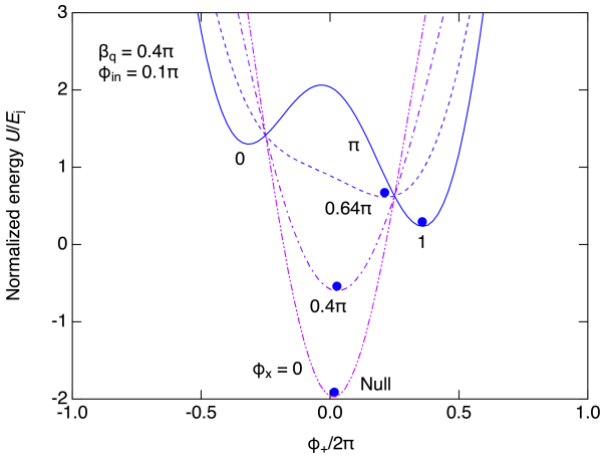


Fig. 4 Potential energy of the QFP for $\beta_q = 0.4\pi$ and $\phi_{in} = 0.1\pi$. The potential energy shape gradually changes from a single well to a double well, so that the circuit state can switch to logic 1 reversibly. This switching process is referred to as adiabatic switching.

$$\phi_1 - \phi_x = \phi_2 + \phi_x = \phi_q + \phi_{in}, \quad (2)$$

where $\phi_x = 2\pi\Phi_x/\Phi_0$ is the normalized excitation flux and $\phi_{in} = 2\pi\Phi_{in}/\Phi_0$ is the normalized input flux. Equation 2 indicates that $\phi_- = \phi_x$, and $\phi_+ = \phi_q + \phi_{in}$, so that $U_j = -2E_j\cos\phi_x\cos\phi_+$ and $U_m = E_j(\phi_+ - \phi_{in})^2/2\beta_q$. Consequently, $U = U_m + U_j$ is given as follows [14]:

$$\frac{U}{E_j} = \frac{(\phi_+ - \phi_{in})^2}{2\beta_q} - 2\cos\phi_x\cos\phi_+. \quad (3)$$

While an rf SQUID forms a double-well potential by shifting U_m in ϕ space by π with $\phi_b = \pi$, as shown in Fig. 2(a), the QFP forms a double-well potential by inverting the polarity of U_j with $\phi_x = \pi$ (see Eq. 3). Figure 4 shows the potential energy of the QFP as a function of ϕ_+ for $\beta_q = 0.4\pi$ and $\phi_{in} = 0.1\pi$, which tilts the potential energy towards logic 1, while ϕ_x changes from 0 to π. The potential energy shape gradually changes from a single well to a double well, so that the state of the QFP (the blue particle in the figure) is always in the potential minimum while switching from the initial state (null in the figure) to logic 1. This indicates that the logic state of the QFP can be switched in a thermodynamically

reversible manner (i.e., without energy dissipation) in the quasi-static limit. We refer to the switching process shown in Fig. 4 as adiabatic switching [17, 18] since it becomes an adiabatic process in the quasi-static limit.

Next, we derive the potential energy of the QFP with L_1 and L_2 taken into account. Assuming that $L = L_1 = L_2$, the total energy stored in L_1, L_2, and L_q is given by $U_m = E_j(\phi_{L1}^2 + \phi_{L2}^2)/2\beta_L + E_j\phi_q^2/2\beta_q$, where $\beta_L = 2\pi LI_c/\Phi_0$ and ϕ_{L1} and ϕ_{L2} are the normalized fluxes associated with L_1 and L_2, respectively. According to flux quantization, the relation between the phase differences and magnetic fluxes is given by:

$$\phi_1 + \phi_{L1} - \phi_x = \phi_2 + \phi_{L2} + \phi_x = \phi_q + \phi_{in}. \quad (4)$$

Thus, $\phi_{L1} = -[(\phi_+ - \phi_q - \phi_{in}) + (\phi_- - \phi_x)]$, and $\phi_{L2} = -[(\phi_+ - \phi_q - \phi_{in}) - (\phi_- - \phi_x)]$, so that $\phi_{L1}^2 + \phi_{L2}^2 = 2[(\phi_+ - \phi_q - \phi_{in})^2 + (\phi_- - \phi_x)^2]$. Consequently, $U = U_m + U_j$ is given by:

$$\frac{U}{E_j} = \frac{{\phi_q}^2}{2\beta_q} + \frac{(\phi_+ - \phi_q - \phi_{in})^2}{\beta_L} + \frac{(\phi_- - \phi_x)^2}{\beta_L} - 2\cos\phi_-\cos\phi_+. \quad (5)$$

Here we conduct the following approximation to remove ϕ_q from Eq. 5 [49, 50]. We assume that the third term on the right side of Eq. 5 is negligibly small since in general $\phi_- - \phi_x$ is close to zero. Then, Eq. 5 denotes the potential energy when the load inductor L_q is replaced with $L_q + L/2$. Recall that ϕ_+ denotes the phase difference across the dc SQUID (see Eq. 3); thus, $\phi_+ - \phi_q - \phi_{in}$ in the second term on the right side of Eq. 5 denotes the flux associated with $L/2$ that is connected to L_q in series, and the second term represents the energy stored in $L/2$. As a result, the first and second terms on the right side of Eq. 5 can be reduced to $(\phi_+ - \phi_{in})^2/(2\beta_q + \beta_L)$ and U can be approximated to [50]:

$$\frac{U}{E_j} \approx \frac{(\phi_+ - \phi_{in})^2}{2\beta_q + \beta_L} + \frac{(\phi_- - \phi_x)^2}{\beta_L} - 2\cos\phi_-\cos\phi_+. \quad (6)$$

This equation is used to estimate the potential energy shape when L_1 and L_2 are taken into account.

While we explained the operation of the QFP based on an rf SQUID since we wanted to discuss the potential energy shape, it is worth noting that the original explanation of the QFP by Goto is based on the Goto pair (i.e., the parametron using Esaki diodes) [51], which can be found in the literature [49, 52].

3.3 Adiabatic quantum-flux-parametron (AQFP)

The QFP can perform adiabatic switching without energy dissipation in the quasi-static limit; however, some amount of energy is dissipated at a finite operating speed. The switching energy E_{sw} (energy dissipation per switching event) of the QFP is determined by how slowly the QFP is operated, which is quantified by the ratio between two time constants: the characteristic time of the Josephson junctions (τ_j) and the duration time of the switching process (τ_x). Thus, E_{sw} is given as follows [16, 53]:

$$E_{sw} \approx 2I_c\Phi_0\frac{\tau_j}{\tau_x}, \quad (7)$$

where $I_c\Phi_0$ denotes the energy scale and coefficient 2 is required because we assume that the potential energy of the QFP is excited to a double-well potential and then reset to a single-well potential (i.e., the QFP switches twice) during a switching event. τ_j is given by the L/R time constant of the Josephson junction:

$$\tau_j \approx 2\pi\frac{L_j}{R} = \frac{\Phi_0}{I_cR} = \sqrt{\frac{2\pi\Phi_0C_s}{\beta_cJ_c}}, \quad (8)$$

where $L_j = \Phi_0/2\pi I_c$ is the Josephson inductance, R is the equivalent resistance of the subgap resistance and shunt resistor (which is added to the Josephson junction in parallel to adjust the quality factor Q), J_c is the critical current density, C_s is the junction capacitance per area, C is the junction capacitance, and $\beta_c = Q^2 = 2\pi R^2CI_c/\Phi_0$ is the McCumber parameter [54]. τ_x is the time required for ϕ_x to change from 0 to π, i.e., the rising/falling time of I_x. If I_x is sinusoidal with frequency f, $\tau_x = 1/2f$.

Equations 7 and 8 can be also derived from a phase-evolution viewpoint [15, 22]. While the QFP is excited, either J_1 or J_2 switches depending on ϕ_{in}. For a positive ϕ_{in}, J_1 switches and ϕ_1 increases by approximately 2π. The energy dissipation for this excitation process (E_x) is given by the voltage across J_1 (V_1) and R with regard to J_1:

$$E_x = \int_0^{\tau_x}\frac{{V_1}^2}{R}dt = \frac{1}{R}\left(\frac{\Phi_0}{2\pi}\right)^2\int_0^{\tau_x}\left(\frac{d\phi_1}{dt}\right)^2 dt \approx \frac{1}{R}\left(\frac{\Phi_0}{\tau_x}\right)^2\int_0^{\tau_x}dt = \frac{{\Phi_0}^2}{R\tau_x}, \quad (9)$$

where $V_1 = (\Phi_0/2\pi)(d\phi_1/dt)$, $d\phi_1/dt \approx 2\pi/\tau_x$, and t is time. Assuming that the reset process dissipates the same amount of energy $E_r = E_x$, E_{sw} is given by:

$$E_{sw} = E_x + E_r \approx \frac{2{\Phi_0}^2}{R\tau_x}, \quad (10)$$

which agrees with Eqs. 7 and 8.

Equations 7 and 8 show that E_{sw} decreases by increasing the value of J_c and/or β_c. Therefore, the AQFP uses high-J_c processes and high-β_c (i.e., underdamped) Josephson junctions to significantly reduce energy dissipation. Figure 5 shows the simulated E_{sw} of the AQFP and original QFP as a function of τ_x for I_c = 50 μA. E_{sw} of the AQFP is taken from our previous work [55] and E_{sw} of the original QFP is estimated from the literature [15], which shows $E_{sw} \sim 10^{-19}$ J for I_c = 25 μA, C = 1 pF, R = 1 Ω, and f = 10 GHz (E_{sw} is normalized by I_c = 50 μA in Fig. 5). Figure 5 shows that the AQFP operates with energy dissipation less than the original QFP by one to two orders of magnitude. Furthermore, E_{sw} of the AQFP can fall below the thermodynamic limit $k_BT\ln 2$, the Landauer bound [21], by increasing τ_x, where k_B is the Boltzmann constant and T is temperature. For

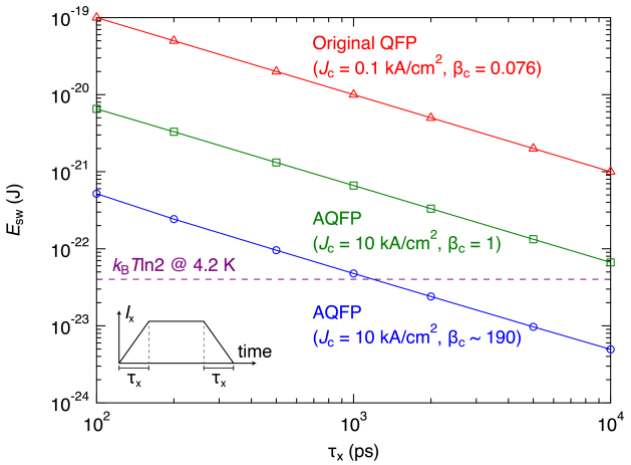


Fig. 5 Simulated switching energy of the AQFP and original QFP. The energy dissipation of the AQFP is significantly reduced by adopting high-J_c processes and/or underdamped Josephson junctions.

comparison, it should be noted that general logic devices, such as CMOS and RSFQ logic, operate non-adiabatically and irreversibly, thus dissipating much more energy than k_BT for every switching event [56].

Here we clarify the benefit of AQFP logic by comparing its energy dissipation with that of other logic families in a simple way. The average energy dissipation per device $\overline{E_{diss}}$ of CMOS logic is given by $\overline{E_{diss}} = P/\alpha f N_{tr}$ [57], where P is power dissipation, α is the activity factor, f is the clock frequency, and N_{tr} is transistor count. Taking Intel's Xeon Platinum 8180 microprocessor [58] as an example, P = 205 W, f = 2.5 GHz, and $N_{tr} = 8 \times 10^9$ [58, 59], which gives $\overline{E_{diss}} = 8.2 \times 10^{-17}$ J with the assumption that α = 0.125 [60]. This dissipation corresponds to ~20,000k_BT at 300 K and is far from the thermodynamic limit. For conventional superconductor logic, RSFQ, the average energy dissipation is given by $\overline{E_{diss}} = \overline{I_b} V_b/f \approx 0.8 \overline{I_c} V_b/f$, where $\overline{I_b}$ and $\overline{I_c}$ are the average bias and critical currents of the Josephson junctions, respectively, and V_b is the bias voltage. Assuming that $\overline{I_c}$ = 150 μA, V_b = 2.5 mV, and f = 50 GHz, $\overline{E_{diss}} = 6.0 \times 10^{-18}$ J, which corresponds to ~100,000k_BT at 4.2 K. As for AQFP logic, we have demonstrated an 8-bit carry look-ahead adder with $\overline{E_{diss}} = 1.4 \times 10^{-21}$ J, or 24k_BT, at 5 GHz [61].

Figure 6 shows $\overline{E_{diss}}$ of CMOS, RSFQ, QFP, and AQFP logic for comparison. The solid lines in Fig. 6 denote the energy-delay product (EDP) of each logic family. The two blue solid lines are for AQFP logic; one represents the EDP based on an 8-bit carry look-ahead adder with J_c = 10 kA/cm^2 [61] and the other represents the EDP based on a buffer with J_c = 2.5 kA/cm^2 [53]. AQFP logic can operate with much less energy dissipation than the other logic families, and furthermore, the energy dissipation is close to the thermodynamic and quantum limits, where the quantum limit corresponds to

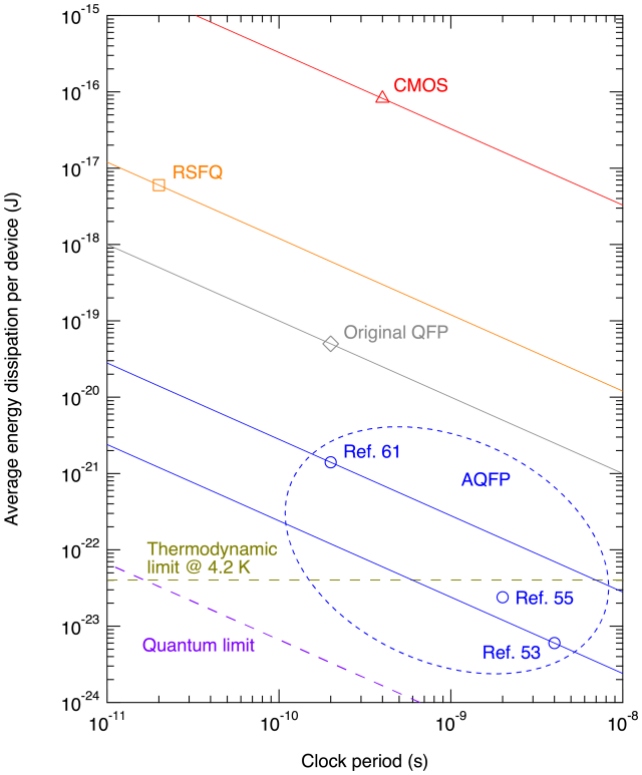


Fig. 6 Comparison of energy efficiency among several logic families. AQFP logic operates near the thermodynamic and quantum limits.

the Planck constant. This indicates the possibility of extremely energy-efficient computing systems using AQFP logic.

We note that, in addition to energy efficiency, many other factors, such as clock speed, circuit density, and cooling overhead, should be also taken into account in actual circuit design. Therefore, it is crucial to select the best logic family and/or combine multiple logic families [46, 62] for each application, since every logic family has different advantages and disadvantages.

4. Design Methodology

This section describes how to design AQFP circuits, particularly how to power and clock AQFP circuits (i.e., four-phase clocking) and how to design basic logic gates (i.e., the minimal design). As a design example, we show the details (schematic diagram, physical layout, and numerical simulation) of an AQFP full adder to give a clear image of what AQFP circuits look like and how they work.

4.1 Clocking scheme

Special clocking schemes are required for operating AQFP circuits because all AQFP logic gates, including both combinational and sequential circuits, must be

clocked by excitation currents. Furthermore, unlike CMOS, AQFP logic gates must be clocked in the order of logic operations. Figure 7(a) shows an AQFP buffer chain powered by a typical clocking scheme, four-phase clocking [34, 63]. The entire circuit is clocked and powered by a pair of ac excitation currents (I_{x1} and I_{x2}) with a phase separation of 90°, which apply ac magnetic flux with an amplitude of $0.5\Phi_0$ to each gate. Moreover, the dc offset current I_d applies a dc magnetic flux of $\pm 0.5\Phi_0$ to each gate. By doing so, logic operations are performed from phase ϕ_1 to phase ϕ_4 with a phase separation of 90°: the logic gates at ϕ_1 and ϕ_3 are clocked at the rising and falling edges of I_{x1}, respectively, and those at ϕ_4 and ϕ_2 are clocked at the rising and falling edges of I_{x2}, respectively.

Figure 7(b) depicts a circuit diagram of an AQFP buffer in the buffer chain. I_x (i.e., I_{x1} or I_{x2}) and I_d flow through the two excitation lines L_x and L_d, respectively, thereby applying excitation flux to the dc SQUID part (J_1-L_1-L_2-J_2). Unlike the QFP shown in Fig. 3, the input current I_{in} is directly applied via L_{in}, and the output current I_{out} is generated via the signal transformer, comprising L_q and L_{out} coupled to each other by k_{out}. Note that the signal transformer is important for our gate design scheme, the minimal design [64]. First, the LI_c product of the AQFP buffer is almost fixed by L_q because the output port is separated by the signal transformer, and thus the amplitude of the signal current I_s through L_q is almost independent of what are connected to the input and output ports. Second, the signal transformer enables logical negation: the AQFP gate shown in Fig. 7(b) operates as a buffer for a positive k_{out} but operates as an inverter for a negative k_{out}, i.e., a buffer and an inverter are interchangeable. These two points ensure that various logic gates can be designed by putting buffers and inverters together, as will be shown later.

Figure 8 shows simulation waveforms for an AQFP buffer chain powered by four-phase clocking with 5-GHz excitation currents I_{x1} and I_{x2}. The simulation was

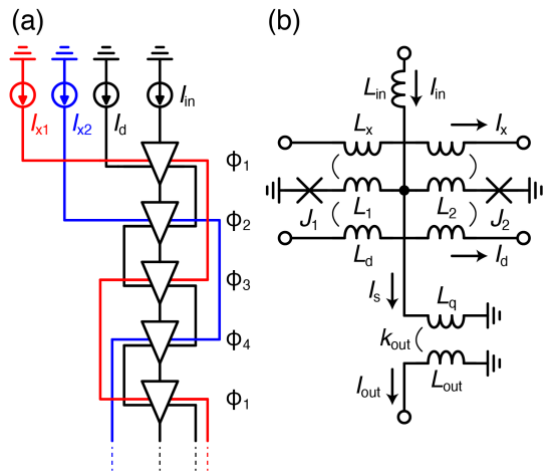


Fig. 7 (a) AQFP buffer chain powered by four-phase clocking. Logic operations are performed from ϕ_1 to ϕ_4 with a phase separation of 90°. (b) AQFP buffer. I_x and I_d apply ac and dc magnetic fluxes, respectively.

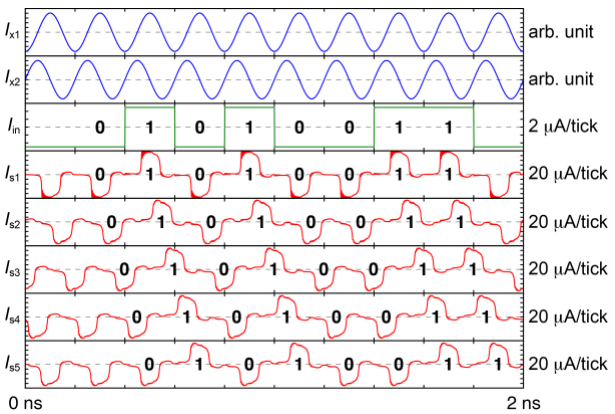


Fig. 8 Simulation waveforms for an AQFP buffer chain powered by four-phase clocking at 5 GHz. I_{s1} through I_{s5} represent the logic states of the first through fifth buffers, respectively.

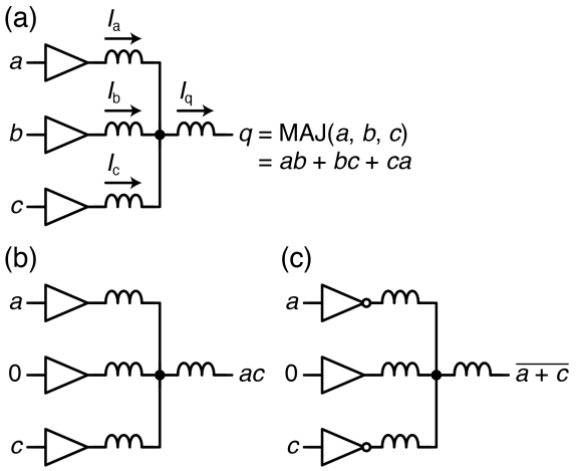


Fig. 9 Logic gate design based on majority logic. (a) Majority gate. The output logic q, i.e., the polarity of I_q, is determined by the majority vote of I_a, I_b, and I_c. (b) AND gate. (c) NOR gate.

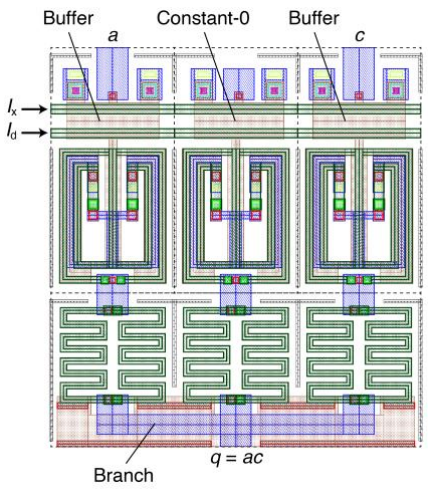


Fig. 10 AND cell for the HSTP, which comprises two buffer cells (20 μm by 40 μm each), a constant-0 cell (20 μm by 40 μm), and a branch cell (60 μm by 25 μm). The cell dimensions are 60 μm by 65 μm.

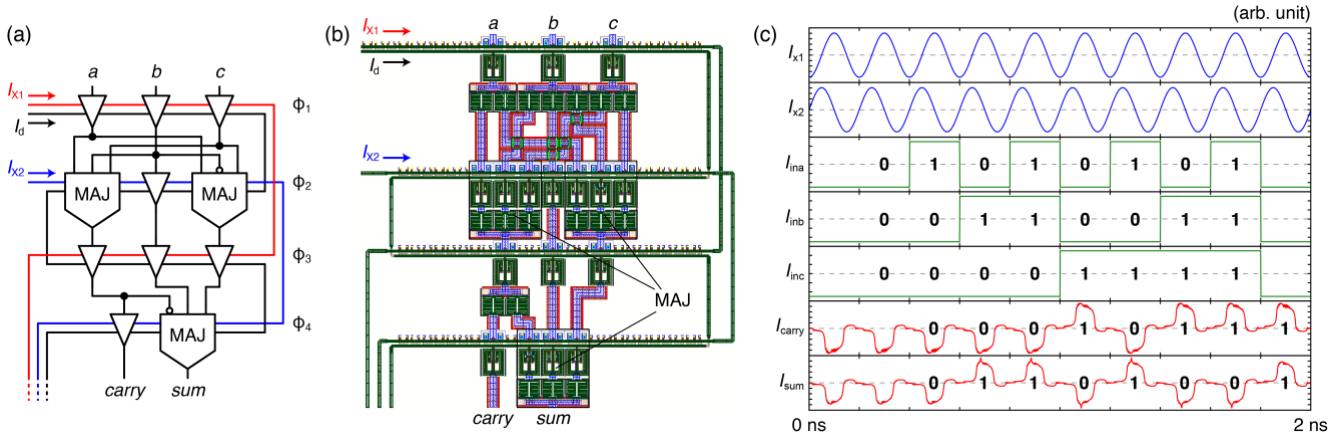


Fig. 11 Full adder. (a) Schematic diagram. A full adder is formed from three MAJ cells, and additional buffers are required for phase adjustment and fanout. (b) Layout design. The excitation currents flow through the meandered excitation lines with 50 Ω. (c) Numerical simulation at 5 GHz.

conducted using a Josephson circuit simulator, JSIM [65], and the circuit parameters used in the simulation are based on a recent cell design (I_c = 50 μA) [66]. I_{in} is the input current applied to the first buffer. I_{s1} through I_{s5}, which correspond to I_s in Fig. 7(b), are the signal currents that represent the logic states of the first through fifth buffers, respectively. The polarity of I_s represents the logic state of a buffer: a positive I_s denotes the logic-1 state and a negative I_s denotes the logic-0 state. Thus, Fig. 8 shows that data stream "01010011" propagates through the buffer chain with a latency of a quarter clock cycle (50 ps at 5 GHz) per gate. This latency is not sufficiently small for some applications; thus, we have also proposed a low-latency clocking scheme, delay-line clocking [67].

4.2 Logic gate design

AQFP logic gates are designed based on majority logic [14, 25], since logical values are represented by the polarity of currents. Figure 9 shows three examples of combinational circuit design. Figure 9(a) depicts a three-input majority (MAJ) gate comprising three buffers. The output currents from the three AQFP buffers (I_a, I_b, and I_c) are merged at the output port, so that the polarity of the output current I_q is determined by whether the majority is positive or negative among I_a, I_b, and I_c, assuming that the amplitude is almost the same among I_a, I_b, and I_c due to the signal transformer in each buffer. Thus, the output q is given by q = MAJ(a, b, c) = $ab + bc + ca$, where a, b, and c are the inputs. Furthermore, various logic gates can be designed based on the MAJ gate because majority logic includes both logical conjunction and disjunction. For instance, by fixing input b to 0, the MAJ gate becomes an AND gate that conducts $q = ac$, as shown in Fig. 9(b). Moreover, since buffers and inverters are interchangeable in AQFP logic, a NOR gate can be designed by replacing two buffers in the AND gate with two inverters [i.e., $q = \overline{a} \cdot \overline{c} = \overline{a + c}$], as shown in Fig. 9(c). As for sequential circuits, a flip-flop can be designed by making a feedback line [68] or storage loop [69] in an AQFP gate.

The three examples shown in Fig. 9 suggest that basic logic gates can be formed from several common components. Therefore, in the development of AQFP cell libraries, the minimal design [64] is adopted so that various logic cells can be quickly designed based on majority logic. In the minimal design, four types of building-block cells (buffer, inverter, constant, and branch cells) are designed in advance, and then other logic cells are designed by putting the building-block cells together like interlocking toy bricks. A constant cell [70] is a gate that generates a constant 0 or 1 signal and a branch cell consists of inductor branches for merging or dividing currents. As an example, we show the layout design of the AND cell for the AIST 10 kA/cm^2 Nb high-speed standard process (HSTP) [63] in Fig. 10. First, each building-block cell is carefully designed using the three-dimensional parameter extractor, InductEx [71, 72]. Then, the AND cell is designed by putting together two buffer cells, a constant-0 cell, and a branch cell, where the constant-0 cell generates a 0 signal and the branch cell merges the output currents from the buffer and constant cells. Likewise, many other logic cells can be designed by putting building-block cells together, without parameter or layout optimization; thus, AQFP cell libraries can be quickly developed and tailored for different fabrication processes [63, 64].

4.3 Circuit design example

Figure 11(a) depicts a circuit diagram of a full adder comprising three MAJ cells [25]. Additional buffers are inserted for phase adjustment and fanout; the output current from a MAJ cell can be small due to the interaction between the three buffers in the MAJ cell,

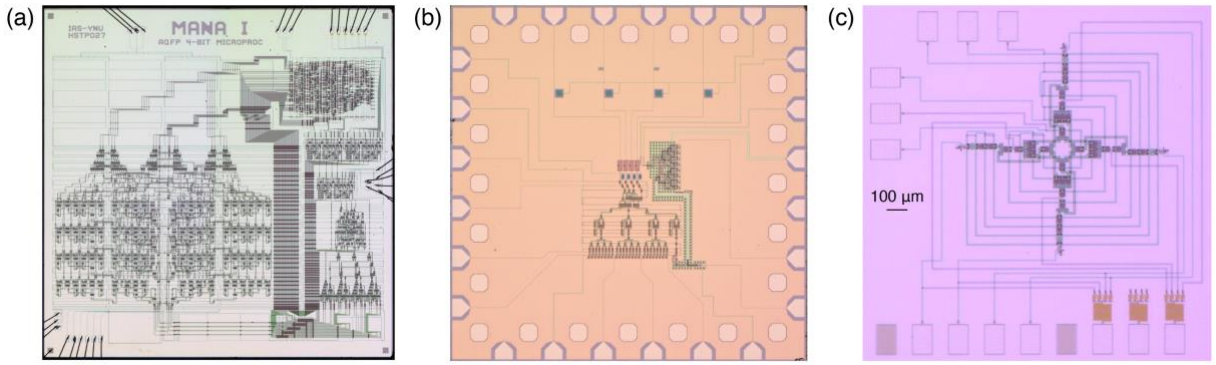


Fig. 12 AQFP chips. (a) MANA on a 10 mm × 10 mm HSTP chip. (b) AQFP/RSFQ hybrid interface on a 5 mm × 5 mm STP2 chip. (c) AQFP-based APS fabricated using the STP2.

and thus the fanout of a MAJ cell (also, an AND cell, OR cell, and other similar cells) is limited to one in our design rule. Figure 11(b) shows the layout design of the full adder for the HSTP. The AQFP logic cells are placed along the meandered excitation lines, through which the excitation currents I_{x1} and I_{x2} flow. Since the frequency of I_{x1} and I_{x2} is equal to the clock frequency, microwave excitation currents flow through the excitation lines at high clock frequencies. Hence, the impedance of the excitation lines, which are 50 Ω microstrip lines, are carefully designed using InductEx [66, 73] so that standing waves do not appear along the excitation lines. Figure 11(c) shows simulation waveforms for the AQFP full adder at 5 GHz, where I_{ina}, I_{inb}, and I_{inc} are the input currents, and I_{carry} and I_{sum} are the signal currents of the buffers placed after the full adder. This figure shows that the carry and sum signals are generated with a latency of four phases, i.e., one clock cycle.

5. Recent Progress

We have established design environment and tools for AQFP logic [74], such as hardware description language-based digital simulation [75], logic synthesis [76], routing and placement tools [77], and the energy estimation method [78], and demonstrated large-scale AQFP circuits with ~1,000 to ~20,000 Josephson junctions. Furthermore, we have developed various systems that exploit the physical features of AQFP logic. This section describes the recent progress on AQFP system development.

5.1 Low-power microprocessor

Since AQFP logic exhibits extremely high energy efficiency, the most straightforward application is the development of low-power microprocessors. We have designed and demonstrated datapath components, such as adders [61, 79], register files [80, 81], and an arithmetic and logic unit (ALU) [74]. Moreover, we have developed an AQFP microprocessor called Monolithic Adiabatic iNtegration Architecture (MANA) [10]. This processor adopts a reduced instruction set computer (RISC) architecture with 4-bit data words via 16-bit instruction words. Figure 12(a) shows a micrograph of the MANA chip that was fabricated using the HSTP, which includes 21,460 Josephson junctions. We have succeeded in demonstrating test programs at a low clock frequency, which include read/write of the register file, ALU execution, branching, and hardware stalling. The estimated energy dissipation of MANA is 3.0×10^{-17} J per operation. The above results indicate that large-scale, energy-efficient computing systems can be achieved using AQFP logic. Furthermore, we plan to build a more practical MANA by adopting the double-gate process [82] and directly coupled QFP logic [83] for higher circuit density, delay-line clocking [67] for reducing latency, and the high-speed voltage driver [84] and multi-block clock distribution [81] for high-frequency operation.

5.2 Reversible computer

A reversible computer [19, 20] is an ideal computer that can operate in a thermodynamically reversible manner, i.e., without energy dissipation, in the quasi-static limit. Many researchers have proposed physical models for building reversible computers [7, 20, 23, 32, 85–89]. We have been investigating reversible computing using AQFP logic since the AQFP is an intrinsically reversible device (based on the fact that adiabatic switching is a reversible process). We have proposed a reversible logic gate based on the AQFP, the reversible quantum-flux-parametron (RQFP) [43, 44]. The RQFP comprises six AQFP gates placed and interconnected symmetrically, and is logically and physically reversible due to the bijective truth table and symmetrical structure. In a numerical simulation, we showed that the RQFP can perform logic operations in a thermodynamically reversible manner (i.e., reversible computing) in the

quasi-static limit [44]. Furthermore, we have fabricated and demonstrated an RQFP gate [43] and RQFP-based reversible full adder [90]. These demonstrations indicate that the RQFP is a practical reversible logic gate and can be used as a building block for making reversible computers. We also verified Landauer's principle [21] in a numerical simulation to reveal the energy dissipation for data erasure [91]. It is noteworthy that whereas a single AQFP can operate reversibly via adiabatic switching, conventional AQFP logic gates, such as MAJ, AND, and OR gates, operate irreversibly and dissipate energy via non-adiabatic processes due to logical and physical irreversibility [44], which causes an inappropriate interaction between AQFPs and lead to non-adiabatic operations. Therefore, there is room for improvement in the energy efficiency of AQFP logic by adopting reversible computing. We have been developing a reversible microprocessor using the RQFP, which has the potential to operate with much less energy dissipation than MANA.

5.3 Single-photon image sensor

AQFP logic exhibits physical features that are suitable for detector applications, namely low-current drive and high sensitivity. First, the amount of supply currents for driving an AQFP circuit (typically, a few milliamps) does not increase with the circuit scale because many logic gates can be coupled to a few common excitation lines, as shown in Fig. 11(a). We have demonstrated an AQFP circuit with approximately 20,000 Josephson junctions using excitation currents of 4.8 mA [92]. Low-current drive is important for cryocooler implementation because the amount of supply currents is limited by the cooling power. Second, AQFP logic has high sensitivity because in adiabatic switching the circuit state can switch to the correct logic state by slightly tilting the potential energy, as shown in Fig. 4. We have demonstrated a high-sensitivity AQFP comparator with a sensitivity of 46 nA [93]. High-sensitivity circuits enable the analog-to-digital conversion of tiny signal currents from cryogenic detectors, such as superconducting nanowire single-photon detectors (SSPDs or SNSPDs) [94, 95], inside a cryocooler. Therefore, we proposed using AQFP logic as readout circuits for SSPD arrays to reduce the number of cables required for reading out the SSPD pixels [45], towards the development of single-photon image sensors. We demonstrated a single-pixel SSPD implemented with an AQFP comparator in a 0.1-W Gifford-McMahon (GM) cryocooler [96] to verify that AQFP logic has sufficient sensitivity to sample the signal currents from an SSPD. Furthermore, we proposed a readout circuit for large-scale SSPD arrays, the AQFP/RSFQ hybrid interface [46], which combines AQFP and RSFQ logic families to achieve both high scalability and high time resolution. Figure 12(b) shows a micrograph of a hybrid interface fabricated using the AIST 2.5 kA/cm^2 Nb standard process (STP2) [97]. As a proof of concept, we demonstrated a four-pixel SSPD array using the hybrid interface and found that each pixel was read out with low error rates and low timing jitter [46]. The next step is to develop hybrid interfaces for large-scale SSPD arrays.

5.4 Stochastic electronics

AQFP logic can perform stochastic operations using thermal fluctuations [91]. Imagine a potential energy shape during adiabatic switching (Fig. 4) for $\phi_{in} = 0$; in this case, the potential energy shape is always symmetrical during excitation. Hence, the circuit state switches to either logic 0 or 1 stochastically due to thermal fluctuations. This indicates that the probability distribution of the AQFP can be easily controlled by the input current. Therefore, we have developed AQFP-based stochastic electronics. We proposed a random number generator (RNG) based on an AQFP buffer and demonstrated high-quality random bit streams [48]; a similar RNG [98] was also proposed using a negative-inductance SQUID [85]. The AQFP RNG may be used for stochastic computing-based neural networks [99]. Furthermore, we proposed using AQFP logic to implement stochastic local search algorithms [47]. Specifically, we developed an amoeba-inspired problem solver (APS) [100, 101] using AQFP logic and demonstrated that the AQFP-based APS can find solutions to a simple logical constraint satisfaction problem using thermal fluctuations [47]. Figure 12(c) shows a micrograph of the AQFP-based APS. While this APS can solve only one instance with four variables, we plan to develop large-scale, practical APSs based on AQFP field-programmable gate arrays [62].

6. Conclusion

We reported a tutorial review on AQFP logic. Following a brief introduction of the historical background, we explained the operating principle of the QFP and AQFP, with a particular focus on the potential energy. We then described how to design AQFP circuits and detailed recent progress on AQFP system development. We hope that this tutorial review will provide insights into AQFP logic for those who are new to this research field.

Acknowledgments

The present study was supported by JSPS KAKENHI (Grants No. JP18H01493, No. JP18H05245, and No. JP19H05614). The circuits were fabricated in the Clean Room for Analog-digital superconductiVITY (CRAVITY) at the National Institute of Advanced Industrial Science and Technology (AIST). The authors would like to thank H. Terai, S. Miki, F. China, S.

Miyajima, and M. Yabuno for their contribution to the development of readout circuits for SSPDs, M. Aono for his contribution to research on the AQFP-based APS, C. J. Fourie for providing InductEx, and all the staff and students (also, ex-staff and ex-students) in our research group at Yokohama National University for their contribution to our research on AQFP logic.

References

[1] N. Jones, "How to stop data centres from gobbling up the world's electricity," *Nature*, vol.561, no. 7722, pp.163–166, Sep. 2018.
[2] O. A. Mukhanov, "Energy-efficient single flux quantum technology," *IEEE Trans. Appl. Supercond.*, vol.21, no. 3, pp.760–769, Jun. 2011.
[3] Q. P. Herr, A. Y. Herr, O. T. Oberg, and A. G. Ioannidis, "Ultra-low-power superconductor logic," *J. Appl. Phys.*, vol.109, no. 10, p.103903, May 2011.
[4] M. Tanaka, M. Ito, A. Kitayama, T. Kouketsu, and A. Fujimaki, "18-GHz, 4.0-aJ/bit operation of ultra-low-energy rapid single-flux-quantum shift registers," *Jpn. J. Appl. Phys.*, vol.51, p.053102, May 2012.
[5] N. Takeuchi, D. Ozawa, Y. Yamanashi, and N. Yoshikawa, "An adiabatic quantum flux parametron as an ultra-low-power logic device," *Supercond. Sci. Technol.*, vol.26, no. 3, p.035010, Mar. 2013.
[6] T. Kamiya, M. Tanaka, K. Sano, and A. Fujimaki, "Energy/space-efficient rapid single-flux-quantum circuits by using π-shifted Josephson junctions," *IEICE Trans. Electron.*, vol.E101.C, no. 5, pp.385–390, May 2018.
[7] W. Wustmann and K. D. Osborn, "Reversible fluxon logic: Topological particles allow ballistic gates along one-dimensional paths," *Phys. Rev. B*, vol.101, no. 1, p.014516, Jan. 2020.
[8] Q. P. Herr, J. Osborne, M. J. A. Stoutimore, H. Hearne, R. Selig, J. Vogel, E. Min, V. V Talanov, and A. Y. Herr, "Reproducible operating margins on a 72 800-device digital superconducting chip," *Supercond. Sci. Technol.*, vol.28, no. 12, p.124003, Dec. 2015.
[9] A. F. Kirichenko, I. V. Vernik, M. Y. Kamkar, J. Walter, M. Miller, L. R. Albu, and O. A. Mukhanov, "ERSFQ 8-bit parallel arithmetic logic unit," *IEEE Trans. Appl. Supercond.*, vol.29, no. 5, p.1302407, Aug. 2019.
[10] C. L. Ayala, T. Tanaka, R. Saito, M. Nozoe, N. Takeuchi, and N. Yoshikawa, "MANA: a Monolithic Adiabatic iNtegration Architecture microprocessor using 1.4-zJ/op unshunted superconductor Josephson junction devices," *IEEE J. Solid-State Circuits*, vol.56, no. 4, pp.1152–1165, Apr. 2021.
[11] S. Nagasawa, K. Hinode, T. Satoh, M. Hidaka, H. Akaike, A. Fujimaki, N. Yoshikawa, K. Takagi, and N. Takagi, "Nb 9-layer fabrication process for superconducting large-scale SFQ circuits and its process evaluation," *IEICE Trans. Electron.*, vol.E97.C, no. 3, pp.132–140, Mar. 2014.
[12] S. K. Tolpygo, V. Bolkhovsky, R. Rastogi, S. Zarr, A. L. Day, E. Golden, T. J. Weir, A. Wynn, and L. M. Johnson, "Advanced fabrication processes for superconductor electronics: current status and new developments," *IEEE Trans. Appl. Supercond.*, vol.29, no. 5, p.1102513, Aug. 2019.
[13] M. Hidaka and S. Nagasawa, "Fabrication process for superconducting digital circuits," *IEICE Trans. Electron.*, vol.E104.C, no. 9, pp.405–410, Sep. 2021.
[14] K. Loe and E. Goto, "Analysis of flux input and output Josephson pair device," *IEEE Trans. Magn.*, vol.21, no. 2, pp.884–887, Mar. 1985.
[15] M. Hosoya, W. Hioe, J. Casas, R. Kamikawai, Y. Harada, Y. Wada, H. Nakane, R. Suda, and E. Goto, "Quantum flux parametron: a single quantum flux device for Josephson supercomputer," *IEEE Trans. Appl. Supercond.*, vol.1, no. 2, pp.77–89, Jun. 1991.
[16] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Energy efficiency of adiabatic superconductor logic," *Supercond. Sci. Technol.*, vol.28, no. 1, p.015003, Jan. 2015.
[17] R. W. Keyes and R. Landauer, "Minimal energy dissipation in logic," *IBM J. Res. Dev.*, vol.14, no. 2, pp.152–157, Mar. 1970.
[18] J. G. Koller and W. C. Athas, "Adiabatic switching, low energy computing, and the physics of storing and erasing information," Workshop on Physics and Computation, pp.267–270, 1992.
[19] C. H. Bennett, "The thermodynamics of computation—a review," *Int. J. Theor. Phys.*, vol.21, no. 12, pp.905–940, Dec. 1982.
[20] E. Fredkin and T. Toffoli, "Conservative logic," *Int. J. Theor. Phys.*, vol.21, no. 3–4, pp.219–253, Apr. 1982.
[21] R. Landauer, "Irreversibility and heat generation in the computing process," *IBM J. Res. Dev.*, vol.5, no. 3, pp.183–191, Jul. 1961.
[22] K. Likharev, "Dynamics of some single flux quantum devices: I. Parametric quantron," *IEEE Trans. Magn.*, vol.13, no. 1, pp.242–244, Jan. 1977.
[23] K. K. Likharev, "Classical and quantum limitations on energy consumption in computation," *Int. J. Theor. Phys.*, vol.21, no. 3–4, pp.311–326, Apr. 1982.
[24] K. K. Likharev, "Superconductor digital electronics," *Phys. C Supercond. its Appl.*, vol.482, pp.6–18, Nov. 2012.
[25] E. Goto, "The Parametron, a digital computing element which utilizes parametric oscillation," *Proc. IRE*, vol.47, no. 8, pp.1304–1316, Aug. 1959.
[26] K. Likharev, S. Rylov, and V. Semenov, "Reversible conveyer computation in array of parametric quantrons," *IEEE Trans. Magn.*, vol.21, no. 2, pp.947–950, Mar. 1985.
[27] https://www.jst.go.jp/erato/en/research_area/completed/gjrj_P.html
[28] J. Casas, R. Kamikawai, N. Miyamoto, and E. Goto, "A quantum flux parametron (QFP) 12-bit shift register capable of stable microwave frequency operation," *Jpn. J. Appl. Phys.*, vol.30, no. 12B, pp.3938–3942, Dec. 1991.
[29] J. Casas, R. Kamikawai, and E. Goto, "High-frequency operation of quantum flux parametron (QFP) based shift registers and frequency prescalers," *IEEE J. Solid-State Circuits*, vol.27, no. 1, pp.97–105, Jan. 1992.
[30] N. Shimizu, Y. Harada, N. Miyamoto, and E. Goto, "A new A/D converter with quantum flux parametron," *IEEE Trans. Magn.*, vol.25, no. 2, pp.865–868, Mar. 1989.
[31] Y. Harada and J. B. Green, "High-speed experiments on a QFP-based comparator for ADCs with 18-GHz sample rate and 5-GHz input frequency," *IEEE Trans. Appl. Supercond.*, vol.2, no. 1, pp.21–25, Mar. 1992.
[32] E. Goto, W. Hioe, and M. Hosoya, "Physical limits to quantum flux parametron operation," *Phys. C Supercond.*, vol.185–189, pp.385–390, Dec. 1991.
[33] R. Ruby, G. Lee, H. Ko, and A. Barfknecht, "Switching probability of QFP comparators as a function of exciter slew-rate," *IEEE Trans. Appl. Supercond.*, vol.3, no. 1, pp.2694–2697, Mar. 1993.
[34] W. Hioe, M. Hosoya, S. Kominami, H. Yamada, R. Mita, and K. Takagi, "Design and operation of a quantum flux parametron bit-slice ALU," *IEEE Trans. Appl. Supercond.*, vol.5, no. 2, pp.2992–2995, Jun. 1995.
[35] M. Jeffery, "Analysis of a high-temperature superconductor quantum flux parametron operating at 77 K," *IEEE Trans. Appl. Supercond.*, vol.5, no. 4, pp.3522–3526, Dec. 1995.
[36] D. A. Feld, P. Sage, K. K. Berggren, and A. Siddiqui, "Measurement of the energy sensitivity of a superconductive

comparator," *IEEE Trans. Appl. Supercond.*, vol.9, no. 2, pp.4361–4366, Jun. 1999.
[37] Y. Tarutani, H. Hasegawa, T. Fukazawa, A. Tsukamoto, and K. Takagi, "Investigation of signal isolation and transient characteristics in quantum-flux-parametron (QFP) circuits," *IEEE Trans. Appl. Supercond.*, vol.9, no. 2, pp.4353–4356, Jun. 1999.
[38] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: a new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," *IEEE Trans. Appl. Supercond.*, vol.1, no. 1, pp.3–28, Mar. 1991.
[39] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, "Superconductor digital frequency divider operating up to 750 GHz," *Appl. Phys. Lett.*, vol.73, no. 19, p.2817, Nov. 1998.
[40] S. Borkar and A. A. Chien, "The future of microprocessors," *Commun. ACM*, vol.54, no. 5, pp.67–77, May 2011.
[41] R. F. Service, "What it'll take to go exascale," *Science.*, vol.335, no. 6067, pp.394–396, Jan. 2012.
[42] P. Ball, "Computer engineering: Feeling the heat," *Nature*, vol.492, no. 7428, pp.174–176, Dec. 2012.
[43] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Reversible logic gate using adiabatic superconducting devices," *Sci. Rep.*, vol.4, p.6354, Sep. 2014.
[44] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Reversibility and energy dissipation in adiabatic superconductor logic," *Sci. Rep.*, vol.7, no. 1, p.75, Mar. 2017.
[45] N. Takeuchi, T. Yamashita, S. Miyajima, S. Miki, N. Yoshikawa, and H. Terai, "Adiabatic quantum-flux-parametron interface for the readout of superconducting nanowire single-photon detectors," *Opt. Express*, vol.25, no. 26, pp.32650–32658, Dec. 2017.
[46] N. Takeuchi, F. China, S. Miki, S. Miyajima, M. Yabuno, N. Yoshikawa, and H. Terai, "Scalable readout interface for superconducting nanowire single-photon detectors using AQFP and RSFQ logic families," *Opt. Express*, vol.28, no. 11, pp.15824–15834, May 2020.
[47] N. Takeuchi, M. Aono, and N. Yoshikawa, "Superconductor amoeba-inspired problem solvers for combinatorial optimization," *Phys. Rev. Appl.*, vol.11, no. 4, p.044069, Apr. 2019.
[48] W. Luo, N. Takeuchi, O. Chen, and N. Yoshikawa, "Low-autocorrelation random number generator based on adiabatic quantum-flux-parametron logic," *IEEE Trans. Appl. Supercond.*, vol.31, no. 5, p.1302305, Aug. 2021.
[49] E. Goto and K. F. Loe, *DC Flux Parametron — A New Approach to Josephson Junction Logic* (World Scientific Series in Computer Science: Volume 6), Singapore: World Scientific Publishing Co. Pte. Ltd., 1986.
[50] H. L. Ko and G. S. Lee, "Noise analysis of the quantum flux parametron," *IEEE Trans. Appl. Supercond.*, vol.2, no. 3, pp.156–164, Sep. 1992.
[51] E. Goto, K. Murata, K. Nakazawa, K. Nakagawa, T. Moto-Oka, Y. Matsuoka, Y. Ishibashi, H. Ishida, T. Soma, and E. Wada, "Esaki diode high-speed logical circuits," *IRE Trans. Electron. Comput.*, vol.EC-9, no. 1, pp.25–29, Mar. 1960.
[52] W. Hioe and E. Goto, *Quantum Flux Parametron — A Single Quantum Flux Superconducting Logic Device* (Studies in Josephson Supercomputers: Volume 2), Singapore: World Scientific Publishing Co. Pte. Ltd., 1991.
[53] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Simulation of sub-k_BT bit-energy operation of adiabatic quantum-flux-parametron logic with low bit-error-rate," *Appl. Phys. Lett.*, vol.103, no. 6, p.062602, Aug. 2013.
[54] D. E. McCumber, "Effect of ac impedance on dc voltage-current characteristics of superconductor weak-link junctions," *J. Appl. Phys.*, vol.39, no. 7, pp.3113–3118, 1968.
[55] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Thermodynamic study of energy dissipation in adiabatic superconductor logic," *Phys. Rev. Appl.*, vol.4, no. 3, p.034007, Sep. 2015.
[56] V. V. Zhirnov, R. K. Cavin, J. A. Hutchby, and G. I. Bourianoff, "Limits to binary logic switch scaling-a gedanken model," *Proc. IEEE*, vol.91, no. 11, pp.1934–1939, Nov. 2003.
[57] V. Zhirnov, R. Cavin, and L. Gammaitoni, "Minimum Energy of Computing, Fundamental Considerations," in ICT - Energy - Concepts Towards Zero - Power Information and Communication Technology, G. Fagas, ed. InTech, 2014.
[58] https://ark.intel.com/content/www/us/en/ark/products/120496/intel-xeon-platinum-8180-processor-38-5m-cache-2-50-ghz.html
[59] https://en.wikipedia.org/wiki/Transistor_count
[60] E. Hung, J. J. Davis, J. M. Levine, E. A. Stott, P. Y. K. Cheung, and G. A. Constantinides, "KAPow: A system identification approach to online per-module power estimation in FPGA designs," 2016 IEEE 24th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), pp.56–63, May 2016.
[61] N. Takeuchi, T. Yamae, C. L. Ayala, H. Suzuki, and N. Yoshikawa, "An adiabatic superconductor 8-bit adder with $24k_BT$ energy dissipation per junction," *Appl. Phys. Lett.*, vol.114, no. 4, p.042602, Jan. 2019.
[62] Y. Okuma, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Design and demonstration of an adiabatic-quantum-flux-parametron field-programmable gate array using Josephson-CMOS hybrid memories," *IEEE Trans. Appl. Supercond.*, vol.29, no. 8, p.1103606, Dec. 2019.
[63] N. Takeuchi, S. Nagasawa, F. China, T. Ando, M. Hidaka, Y. Yamanashi, and N. Yoshikawa, "Adiabatic quantum-flux-parametron cell library designed using a 10 kA cm^{-2} niobium fabrication process," *Supercond. Sci. Technol.*, vol.30, no. 3, p.035002, Mar. 2017.
[64] N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Adiabatic quantum-flux-parametron cell library adopting minimalist design," *J. Appl. Phys.*, vol.117, no. 17, p.173912, May 2015.
[65] E. S. Fang and T. Van Duzer, "A Josephson Integrated Circuit Simulator (JSIM) for Superconductive Electronics Application," 1989 International Superconductivity Electronics Conference (ISEC '89), pp.407–410, 1989.
[66] N. Takeuchi, H. Suzuki, C. J. Fourie, and N. Yoshikawa, "Impedance design of excitation lines in adiabatic quantum-flux-parametron logic using InductEx," *IEEE Trans. Appl. Supercond.*, vol.31, no. 5, p.1300605, Aug. 2021.
[67] N. Takeuchi, M. Nozoe, Y. He, and N. Yoshikawa, "Low-latency adiabatic superconductor logic using delay-line clocking," *Appl. Phys. Lett.*, vol.115, no. 7, p.072601, Aug. 2019.
[68] T. Yamae, N. Takeuchi, and N. Yoshikawa, "Binary counters using adiabatic quantum-flux-parametron logic," *IEEE Trans. Appl. Supercond.*, vol.31, no. 2, p.1300305, Mar. 2021.
[69] N. Takeuchi, T. Ortlepp, Y. Yamanashi, and N. Yoshikawa, "Novel latch for adiabatic quantum-flux-parametron logic," *J. Appl. Phys.*, vol.115, no. 10, p.103910, Mar. 2014.
[70] T. Ando, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Adiabatic quantum-flux-parametron constant cells using asymmetrical structures," *IEEJ Trans. Fundam. Mater.*, vol.136, no. 12, pp.747–752, Dec. 2016 (in Japanese).
[71] C. J. Fourie, "Full-gate verification of superconducting integrated circuit layouts with InductEx," *IEEE Trans. Appl. Supercond.*, vol.25, no. 1, p.1300209, Feb. 2015.
[72] https://www.sun-magnetics.com
[73] C. J. Fourie, "Electronic design automation tools for superconducting circuits," *J. Phys. Conf. Ser.*, vol.1590, no. 1, p.012040, Jul. 2020.
[74] C. L. Ayala, R. Saito, T. Tanaka, O. Chen, N. Takeuchi, Y. He, and N. Yoshikawa, "A semi-custom design methodology and

environment for implementing superconductor adiabatic quantum-flux-parametron microprocessors," *Supercond. Sci. Technol.*, vol.33, no. 5, p.054006, May 2020.

[75] Q. Xu, C. L. Ayala, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "HDL-Based Modeling Approach for Digital Simulation of Adiabatic Quantum Flux Parametron Logic," *IEEE Trans. Appl. Supercond.*, vol.26, no. 8, p.1301805, Dec. 2016.

[76] Q. Xu, C. L. Ayala, N. Takeuchi, Y. Murai, Y. Yamanashi, and N. Yoshikawa, "Synthesis Flow for Cell-Based Adiabatic Quantum-Flux-Parametron Structural Circuit Generation With HDL Back-End Verification," *IEEE Trans. Appl. Supercond.*, vol.27, no. 4, p.1301905, Jun. 2017.

[77] Y. Murai, C. L. Ayala, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa, "Development and demonstration of routing and placement EDA tools for large-scale adiabatic quantum-flux-parametron circuits," *IEEE Trans. Appl. Supercond.*, vol.27, no. 6, p.1302209, Sep. 2017.

[78] T. Yamae, N. Takeuchi, and N. Yoshikawa, "Systematic method to evaluate energy dissipation in adiabatic quantum-flux-parametron logic," *J. Appl. Phys.*, vol.126, no. 17, p.173903, Nov. 2019.

[79] C. L. Ayala, N. Takeuchi, Y. Yamanashi, T. Ortlepp, and N. Yoshikawa, "Majority-logic-optimized parallel prefix carry look-ahead adder families using adiabatic quantum-flux-parametron logic," *IEEE Trans. Appl. Supercond.*, vol.27, no. 4, p.1300407, Jun. 2017.

[80] N. Tsuji, C. L. Ayala, N. Takeuchi, T. Ortlepp, Y. Yamanashi, and N. Yoshikawa, "Design and Implementation of a 16-Word by 1-Bit Register File Using Adiabatic Quantum Flux Parametron Logic," *IEEE Trans. Appl. Supercond.*, vol.27, no. 4, p.1300904, Jun. 2017.

[81] N. Tsuji, Y. Yamanashi, N. Takeuchi, C. Ayala, and N. Yoshikawa, "Design and implementation of scalable register files using adiabatic quantum flux parametron logic," 2017 16th International Superconductive Electronics Conference (ISEC), Jun. 2017.

[82] T. Ando, S. Nagasawa, N. Takeuchi, N. Tsuji, F. China, M. Hidaka, Y. Yamanashi, and N. Yoshikawa, "Three-dimensional adiabatic quantum-flux-parametron fabricated using a double-active-layered niobium process," *Supercond. Sci. Technol.*, vol.30, no. 7, p.075003, Jul. 2017.

[83] N. Takeuchi, K. Arai, and N. Yoshikawa, "Directly coupled adiabatic superconductor logic," *Supercond. Sci. Technol.*, vol.33, no. 6, p.065002, Jun. 2020.

[84] N. Takeuchi, H. Suzuki, and N. Yoshikawa, "Measurement of low bit-error-rates of adiabatic quantum-flux-parametron logic using a superconductor voltage driver," *Appl. Phys. Lett.*, vol.110, no. 20, p.202601, May 2017.

[85] V. K. Semenov, G. V. Danilov, and D. V. Averin, "Negative-inductance SQUID as the basic element of reversible Josephson-junction circuits," *IEEE Trans. Appl. Supercond.*, vol.13, no. 2, pp.938–943, Jun. 2003.

[86] C. S. Lent, M. Liu, and Y. Lu, "Bennett clocking of quantum-dot cellular automata and the limits to binary logic scaling," *Nanotechnology*, vol.17, no. 16, pp.4240–4251, Aug. 2006.

[87] B. Lambson, D. Carlton, and J. Bokor, "Exploring the thermodynamic limits of computation in integrated systems: magnetic memory, nanomagnetic logic, and the Landauer limit," *Phys. Rev. Lett.*, vol.107, no. 1, p.010604, Jul. 2011.

[88] J. Wenzler, T. Dunn, T. Toffoli, and P. Mohanty, "A nanomechanical Fredkin gate," *Nano Lett.*, vol.14, no. 1, pp.89–93, Jan. 2014.

[89] M. López-Suárez, I. Neri, and L. Gammaitoni, "Sub-k_BT micro-electromechanical irreversible logic gate," *Nat. Commun.*, vol.7, no. 1, p.12068, Jun. 2016.

[90] T. Yamae, N. Takeuchi, and N. Yoshikawa, "A reversible full adder using adiabatic superconductor logic," *Supercond. Sci. Technol.*, vol.32, no. 3, p.035005, Mar. 2019.

[91] N. Takeuchi and N. Yoshikawa, "Minimum energy dissipation required for a logically irreversible operation," *Phys. Rev. E*, vol.97, no. 1, p.012124, Jan. 2018.

[92] T. Narama, Y. Yamanashi, N. Takeuchi, T. Ortlepp, and N. Yoshikawa, "Demonstration of 10k gate-scale adiabatic-quantum-flux-parametron circuits," The 15th International Superconductive Electronics Conference (ISEC 2015), Jul. 2015.

[93] N. Takeuchi, T. Yamae, H. Suzuki, and N. Yoshikawa, "An adiabatic superconductor comparator with 46 nA sensitivity," *IEEE Trans. Appl. Supercond.*, vol.31, no. 5, p.1301105, Aug. 2021.

[94] G. N. Gol'tsman, O. Okunev, G. Chulkova, A. Lipatov, A. Semenov, K. Smirnov, B. Voronov, A. Dzardanov, C. Williams, and R. Sobolewski, "Picosecond superconducting single-photon optical detector," *Appl. Phys. Lett.*, vol.79, no. 6, pp.705–707, Aug. 2001.

[95] C. M. Natarajan, M. G. Tanner, and R. H. Hadfield, "Superconducting nanowire single-photon detectors: physics and applications," *Supercond. Sci. Technol.*, vol.25, no. 6, p.063001, Jun. 2012.

[96] N. Takeuchi, T. Yamashita, S. Miyajima, S. Miki, N. Yoshikawa, and H. Terai, "Demonstration of a superconducting nanowire single-photon detector using adiabatic quantum-flux-parametron logic in a 0.1-W Gifford-McMahon cryocooler," *IEEE Trans. Appl. Supercond.*, vol.29, no. 5, p.2201004, Aug. 2019.

[97] S. Nagasawa, Y. Hashimoto, H. Numata, and S. Tahara, "A 380 ps, 9.5 mW Josephson 4-Kbit RAM operated at a high bit yield," *IEEE Trans. Appl. Supercond.*, vol.5, no. 2, pp.2447–2452, Jun. 1995.

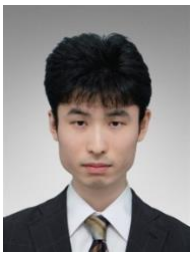
[98] H. Li, J.-S. Liu, H. Cai, Y.-S. Zhang, Q.-C. Liu, G. Li, and W. Chen, "True random number generator realized by extracting entropy from a negative-inductance superconducting quantum interference device," *Chinese Phys. Lett.*, vol.34, no. 1, p.018401, Jan. 2017.

[99] B. D. Brown and H. C. Card, "Stochastic neural computation. I. Computational elements," *IEEE Trans. Comput.*, vol.50, no. 9, pp.891–905, 2001.

[100] M. Aono, M. Naruse, S.-J. Kim, M. Wakabayashi, H. Hori, M. Ohtsu, and M. Hara, "Amoeba-Inspired Nanoarchitectonic Computing: Solving Intractable Computational Problems Using Nanoscale Photoexcitation Transfer Dynamics," *Langmuir*, vol.29, no. 24, pp.7557–7564, Jun. 2013.

[101] M. Aono, "Amoeba-inspired combinatorial optimization machines," *Jpn. J. Appl. Phys.*, vol.59, no. 6, p.060502, Jun. 2020.

Naoki Takeuchi received the B.S., M.E., and Ph.D. degrees from Yokohama National University, Yokohama, Japan, in 2008, 2010, and 2014, respectively, all in electrical and computer engineering. He was an electronic circuit designer at SONY from 2010 to 2011; a JSPS Postdoctoral Research Fellow at the NICT from 2014 to 2015; and a PRESTO Researcher at the JST from 2015 to 2019. He has been with the Institute of Advanced Sciences, Yokohama National University since 2015, where he is currently an Associate Professor; and also with the Research Center for Emerging Computing Technologies, the National Institute of Advanced Industrial Science and Technology (AIST) since 2021, where he is currently a Senior Researcher. His research interests include superconductor logic, cryogenic detectors, and non von Neumann computing. Dr. Takeuchi is a member of the Japan Society of Applied Physics; the Institute of Electronics, Information and Communication Engineers of Japan; and the Institute of Electrical and Electronics Engineers.



Taiki Yamae received the B.S. and M.E. degrees in electrical and computer engineering from Yokohama National University, Yokohama, Japan, in 2018 and 2020, respectively. Since 2020, he has been with the graduate school of engineering science, Yokohama National University, where he is currently a Ph.D. student, and with the Japan Society for the Promotion of Science, where he is a research fellow. He is currently studying superconducting integrated circuits, especially adiabatic quantum-flux-parametron logic. He is a member of the Japan Society of Applied Physics, the Institute of Electronics, Information and Communication Engineers of Japan, and Cryogenics and Superconductivity Society of Japan.

Christopher L. Ayala received the combined B.E./M.S. degree in 2009 and the Ph.D. degree in 2012 from Stony Brook University, Stony Brook, New York, USA, all in electrical and computer engineering. From 2013 to 2015, he was a Post-Doctoral Fellow with IBM Research, Zürich, Switzerland. Since 2015, he has been with the Institute of Advanced Sciences, Yokohama National University, Yokohama, Japan, where he is currently an Associate Professor. His research interests include emerging circuit technologies, superconductor logic, NEMS-MEMS, novel computer architectures, and electronic design automation (EDA). Dr. Ayala is a member of the Institute of Electrical and Electronics Engineers, the Japan Society of Applied Physics, the Institute of Electronics, Information and Communication Engineers of Japan, Eta Kappa Nu Honor Society, and the Tau Beta Pi Engineering Honor Society.

Hideo Suzuki graduated from Koishikawa Technical High School in 1971. He received the B.E. and Ph.D. degree from The Open University of Japan and Tokyo University in 1992 and 1994. In 1971, he joined Fujitsu Laboratories Ltd., where he was engaged in research on microwave solid-state devices and Gunn-effect logic devices. Since 1976, he has been engaged in research and development of superconducting electronical devices and systems. He temporarily transferred to Superconductivity Research Laboratory, ISTEC, from 1998 to 2000, and from 2003 to 2012, and has been continuing research and development of superconducting devices and systems. He was engaged in research on high-speed semiconducting devices from 2001 to 2002 at Fujitsu Lab. Since 2013, he has been with the Institute of Advanced Sciences, Yokohama National University, Yokohama, Japan, where he is currently a Visiting Professor. His research interests include superconducting electronic devices and systems, and cryogenic test instruments. Dr. Suzuki is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Japan Society of Applied Physics.

Nobuyuki Yoshikawa received the B.E., M.E., and Ph.D. degrees in electrical and computer engineering from Yokohama National University, Japan, in 1984, 1986, and 1989, respectively. Since 1989, he has been with the Department of Electrical and Computer Engineering, Yokohama National University, where he is currently a Professor. His research interests include superconductive devices and their application in digital and analog circuits. He is also interested in single-flux-quantum circuits, quantum computing devices and cryo-CMOS devices. Prof. Yoshikawa is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Japan Society of Applied Physics, the Institute of Electrical Engineering of Japan, Cryogenics and Superconductivity Society of Japan, and Institute of Electrical and Electronics Engineers.