


*This form must be filled out by the student, signed and handed in to the module administrator early in the semester. Both the student and the supervisor must sign the agreement on main details and mutual responsibilities. The student should discuss their GA achievement plan with the supervisor, before completing this form. Only the student signs their GA achievement plan, as it is their own responsibility. **This plan is NOT a guaranteed recipe for passing Project (E) 448.** Rather, it serves as a record of the student having considered these important aspects at an appropriately early stage. GA achievement plans should be revised as needed and in consultation with the supervisor, during the course of the project.*



## Main details

Student	Initials and surname	JS Ketteringham	SU number	24009385
Supervisor	Initials and surname			
Project title	Development of a basic but full gate library, using AQFP cells, for the development of complex multi-gates.			
Project description, including the aim, scope and envisioned approach (max. 150 words)	The aim of this project is to design and implement logic gates to create the fundamental digital building blocks such as AND, OR, NAND and XOR gates from AQFP (Adiabatic Quantum-Flux-Parametron) circuits. These gates are then utilized to construct other complex multi-gates such as a half adder and a full adder. These multi-gates will be essential in the development of complex circuitry used in computer systems.			

## Mutual responsibilities

1. It is the responsibility of the student to clarify aspects such as the definition and scope of the project, the place of study, research methodology, reporting opportunities and -methods (e.g. progress reports, internal presentations and conferences) with the supervisor.
2. It is the responsibility of the supervisor to give regular guidance and feedback with regard to the literature, methodology and progress.
3. The rules regarding submission and evaluation of the project is outlined in the module framework and SUNLearn page and will be strictly adhered to.
4. The supervisor conveyed the departmental view on plagiarism to the student, and the student acknowledges the seriousness of such an offence.
5. The supervisor certifies that the project as described above has sufficient scope to achieve, in principle, the required GAs.
6. It is the responsibility of the student to initiate a discussion with the supervisor on GA achievement prior to filling out and handing in this form.


## Signatures for agreement on main details and mutual responsibilities

Role	Signature	Date
Student		18/07/2023
Supervisor	Prof. C. J. FOURIE 	31/07/2023

Student's graduate attribute (GA) achievement plan

How will GA 1 ( <b>problem solving</b> ) be achieved?
Creating the logic gates from AQFP circuits is a problem I have never faced before. It is a complex problem as it requires an understanding of the AQFP circuit and how the Josephson junction works within these circuits. It requires that these AQFP circuits are connected in various manners to create the basic logic gates. Once the gates have been created the following problem will be using these logic gates to create the complex multi-gates. The completion of this project will show the achievement of GA 1.
How will GA 2 ( <b>application of scientific and engineering knowledge</b> ) be achieved?
Engineering knowledge provides a good understanding of electromagnetics, systems and signals and circuit theory applied to non-semiconductor circuits beyond CMOS. This knowledge will be applied to the development of the AQFP circuits and the complex multi-gates.
How will GA 3 ( <b>engineering design</b> ) be achieved?
Engineering design will be applied when designing the logic gates, full and half adders. The design should be such that not only does everything work but the components are set up in such a way that they are easy to understand, neat, and allows one to easily find problems. The logic gates will be designed in such a way that they may be used to create other multi-gates apart from the half and full adders without vastly changing the design of the basic logic gates.
How will GA 4 ( <b>investigations, experiments and data analysis</b> ) be achieved? ( <i>&lt;=100 words</i> )
This attribute will be met by developing a well-structured experiment that will be set up to thoroughly verify the functionality of the logic gates and complex multi-gates. Multiple tests will be run to record the results and iteratively adjust the circuits until the results of the experiment are satisfactory and consistent.
How will GA 5 ( <b>engineering methods, skills and tools, including IT</b> ) be achieved? ( <i>&lt;=100 words</i> )
The project will be completed using a range of engineering software tools, which include but are not limited to, InductEx, JoSim, Circuit layout software such as Spice and MS projects to plan and monitor the progress of the project.
How will GA 6 ( <b>professional and technical communication</b> ) be achieved? ( <i>&lt;=100 words</i> )
The project includes a written report and an oral presentation. These demonstrate competence to communicate effectively, both orally and in writing.
How will GA 8 ( <b>individual work</b> ) be achieved? ( <i>&lt;=100 words</i> )
The student will take primary responsibility for the successful completion of all aspects of the project.
How will GA 9 ( <b>independent learning ability</b> ) be achieved? ( <i>&lt;=100 words</i> )
For successful completion of the project, the student is required to acquire knowledge independently (from the literature or the internet, for example) and without the context of this required knowledge being fully specified in the project definition.

**Signature acknowledging own responsibility to achieve GAs**

Student	Signature	Date
		18/07/2023