

Design Example Report

Title	<i>255 W 80 PLUS Platinum PC Power Supply Using HiperPFS™-2 PFS7328H and HiperLCS™ LCS703HG</i>
Specification	90 VAC – 265 VAC Input; 12 V, 19.71 A and 12 V, 1.5 A Outputs
Application	PC Power Supply
Author	Applications Engineering Department
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Summary and Features

- Integrated PFC stage using PFS7328H from HiperPFS-2 family of ICs
- Integrated LLC stage using LCS703HG from HiperLCS family of ICs
- Standby supply using TNY279PG from TinySwitch™-III family of ICs
- CAPZero™ (CAP004DG) IC used to discharge X capacitors for higher efficiency compared to resistive solution
- Secondary synchronous rectification
- Meeting 80 PLUS platinum efficiency
- System efficiency 92.1% / 93.4% / 91.1% for 20/50/100 % loads respectively at 115 VAC
- System efficiency 91.9% / 94.6% / 93.3 % for 20/50/100 % loads respectively at 230 VAC

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This engineering report describes a 12 V, 19.71 A main converter and 12 V, 1.5 A standby converter design example power supply for 90 VAC to 265 VAC PC power supplies which can also serve as a general purpose evaluation board for the combination of a PFS power factor stage with an LCS output stage using devices from the Power Integrations's HiperPFS-2 and HiperLCS device families.

The design is based on the PFS7328H IC for the PFC front end, with a TNY279PG utilized in an isolated flyback standby supply. An LCS703HG IC is used for the LLC output stage.

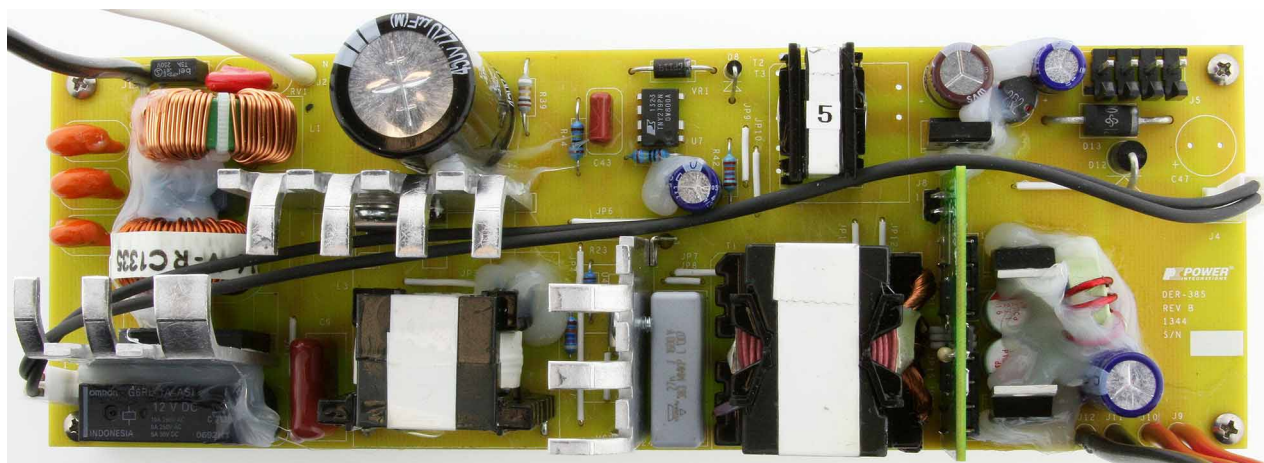


Figure 1 – DER-385 Photograph, Top View.

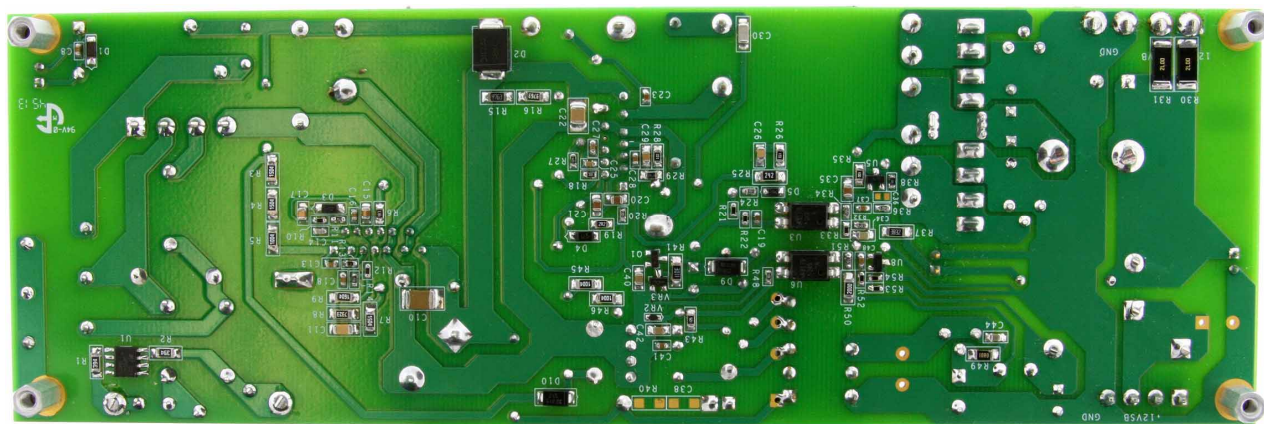


Figure 2 – DER-385 Photograph, Bottom View.





Figure 3 – DER-385 Input Connector.

Note: C1, C2 and C3 were placed on the input connector.

The circuit shown in this report is optimized for >0.9 power factor, over an input voltage range of 90 VAC to 230 VAC, at 100% load, 50% load and 20% load.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire input.
Frequency	f_{LINE}	47	50/60	63	Hz	
THD				<15	%	Full Load, 115 VAC
Power Factor	PF	0.97		<15	%	Full Load, 230 VAC Full Load, 230 VAC
Main Converter Output						
Output Voltage	V_M	11.4	12	12.6	V	12VDC $\pm 5\%$
Output Ripple	$V_{RIPPLE(M)}$			120	mV P-P	20 MHz bandwidth
Output Current	I_M	0.00	19.71	N/A	A	Supply is protected under no-load conditions
Standby Converter Output						
Output Voltage	V_{SB}	11.4	12	12.6	V	12 VDC $\pm 5\%$
Output Ripple	$V_{RIPPLE(SB)}$			120	mV P-P	20 MHz bandwidth
Output Current	I_{SB}	0.00	1.5	N/A	A	Supply is protected under no-load conditions
Total Output Power						
Continuous Output Power	P_{OUT}		255		W	
Efficiency						
Total system at Full Load	η_{sys}	91 93			%	Measured at 115 VAC, Full Load Measured at 230 VAC, Full Load
Environmental						
Conducted EMI						Meets CISPR22 / EN55022 Class B
Harmonic Currents						EN 61000-3-2 Class D
Ambient Temperature	T_{AMB}	0		50	$^{\circ}C$	See thermal section for conditions

Note: This power supply requires forced air cooling for >50% loads.



3 Schematic

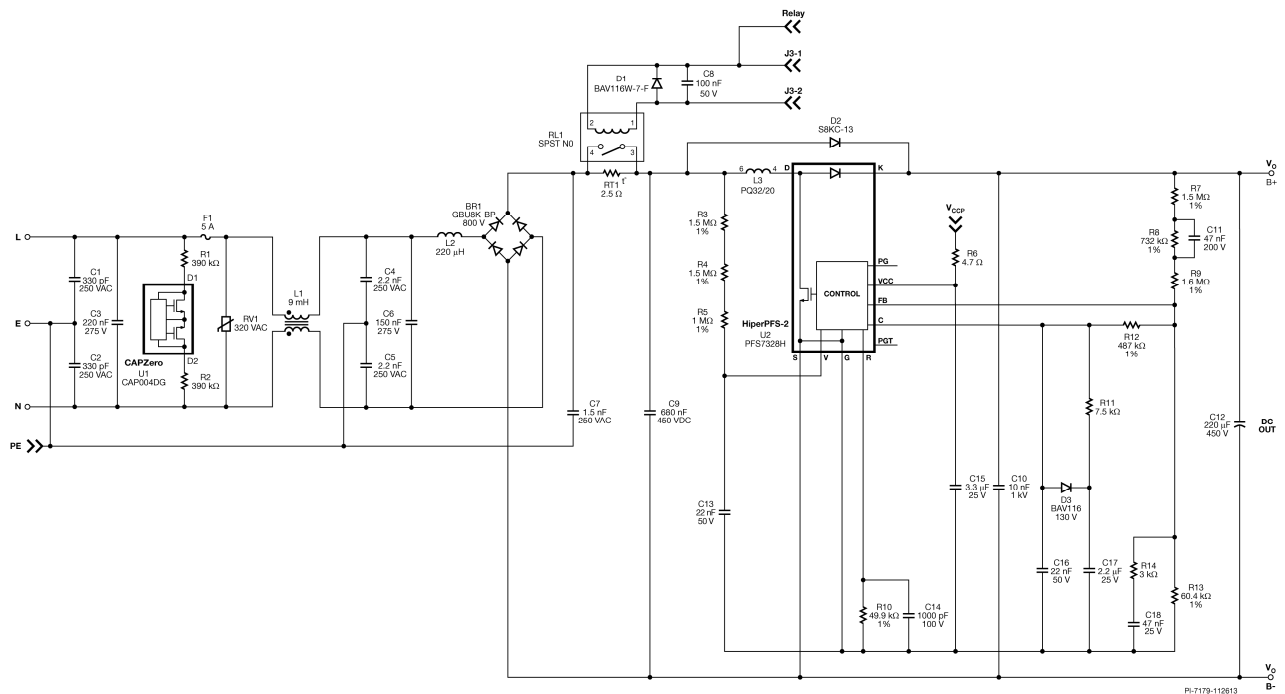


Figure 4 – Schematic DER-385 PC Platinum Power Supply Application Circuit - Input Filter, Bridge Rectifier Section and PFS Section.



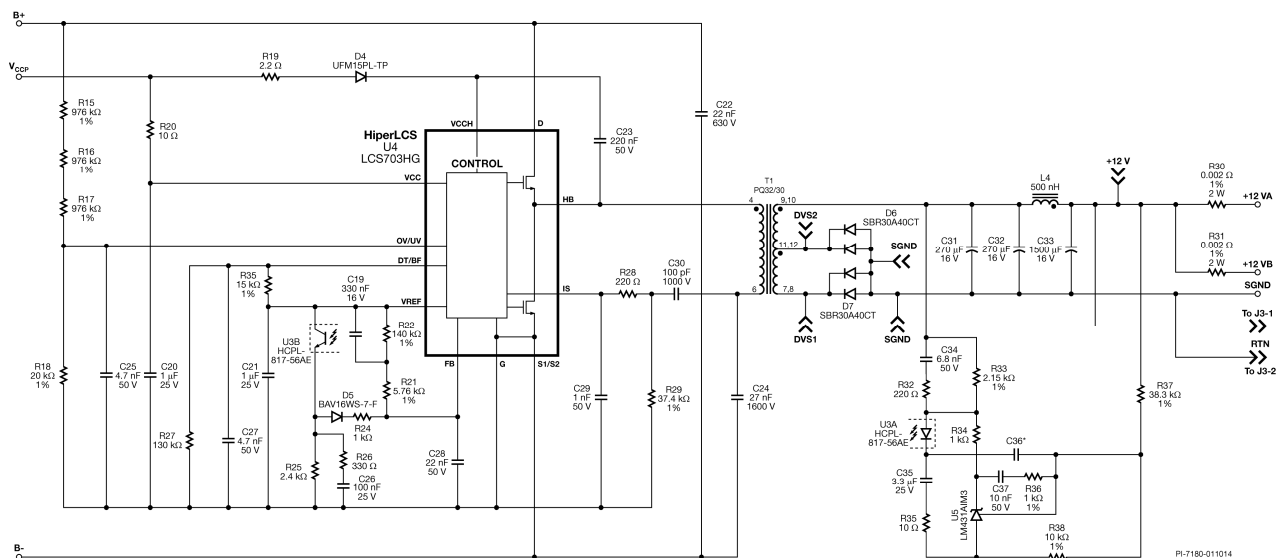


Figure 5 – Schematic DER-385 PC Platinum Power Supply Application Circuit – Main Converter Section.

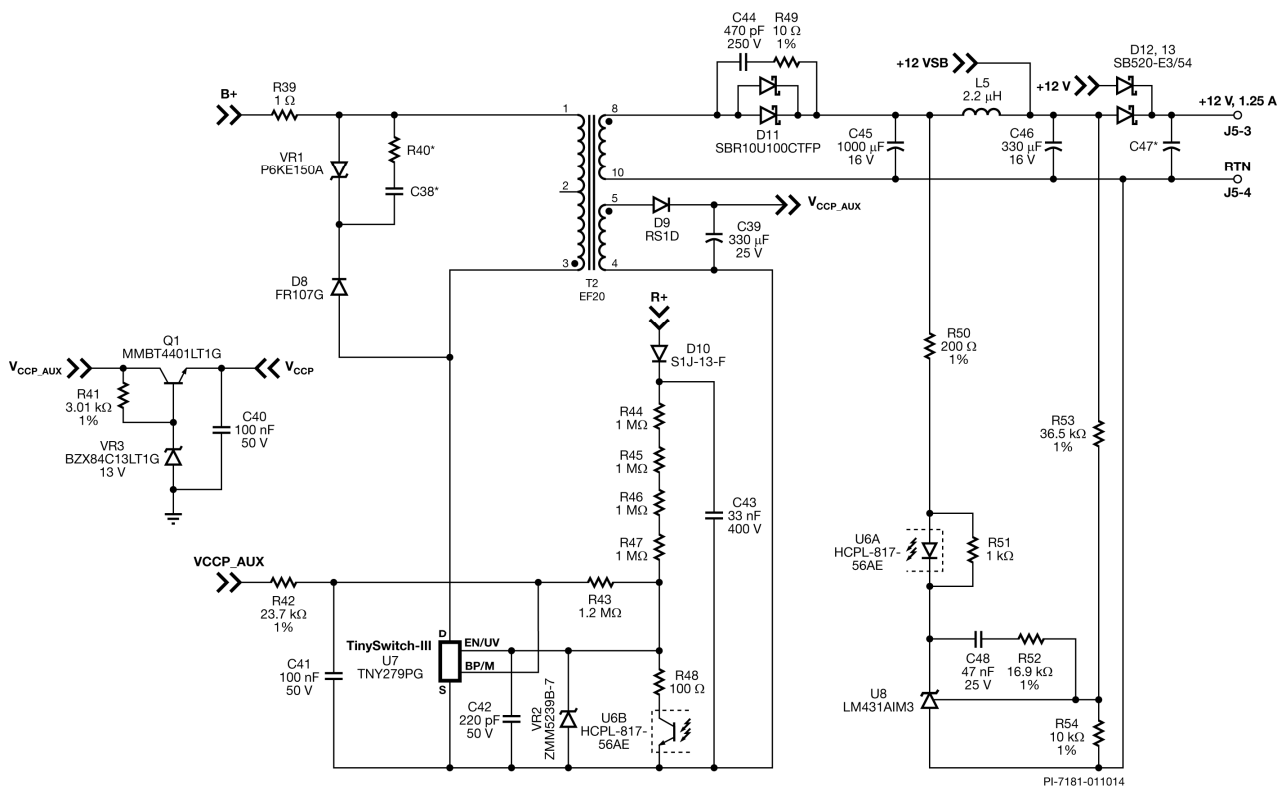
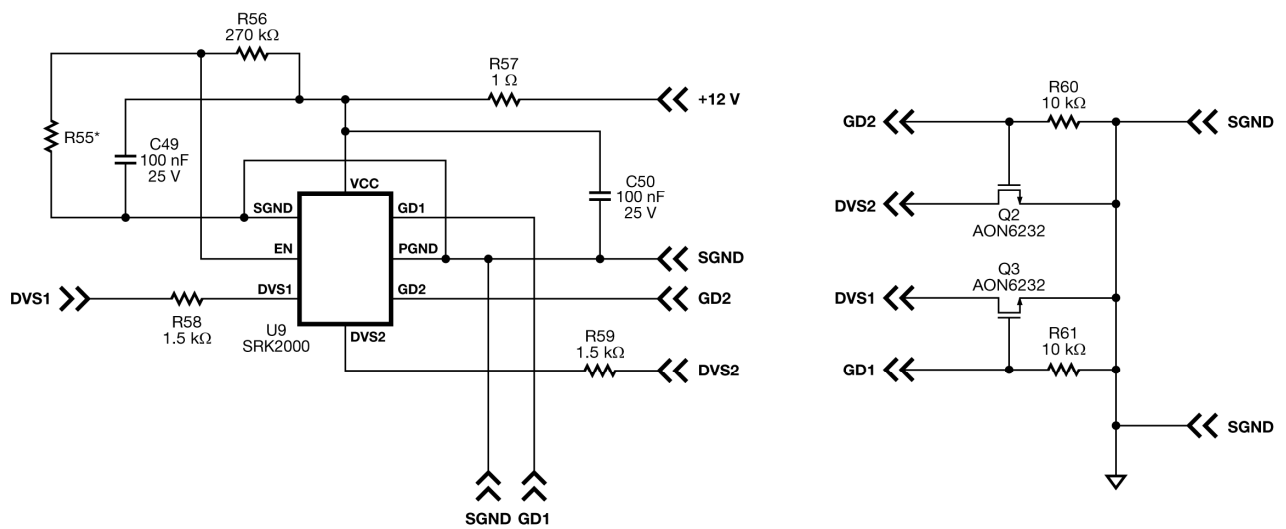


Figure 6 – Schematic DER-385 PC Platinum Power Supply Application Circuit – Standby Section.





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Figure 7 – Schematic DER-385 PC Platinum Power Supply Application Circuit – Sync. Rectifier Section.

Note: * marked components are optional.



4 Circuit Description

The circuit shown in Figures 4, 5, and 6 utilizes the PFS7328H, the LCS703HG, the TNY279PG, and the CAP004DG (optional) devices from Power Integrations in a 12 V, 255 W power factor corrected LLC power supply intended to power a PC power supply.

4.1 Input Filter / Boost Converter / Bias Supply

The schematic in Figures 4 and 5 shows the input EMI filter and PFC stage. The power factor corrector utilizes the PFS7328H PFC controller with integrated power MOSFET and diode. The schematic in Figure 6 shows the bias and standby supply is an isolated flyback using the TNY279PG. The CAP004DG discharges X capacitors C3 and C6 only when the AC input voltage is not present, eliminating the static power loss of resistors R1 and R2.

4.1.1 EMI Filtering

Fuse F1 provides overcurrent protection to the circuit and isolates it from the AC supply in the event of a fault. Diode bridge BR1 rectifies the AC input. Capacitors C1, C2, C3, C4, C5, C6 and C7 in conjunction with inductors L1 and L2, constitute the EMI filter for attenuating both common mode and differential mode conducted noise. Film capacitor C9 provides input decoupling charge storage to reduce input ripple current at the switching frequency and its harmonics.

Resistors R1, R2 and CAPZero IC U1 are provided to discharge the EMI filter capacitors after line voltage has been removed from the circuit, while dissipating zero power during operation.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

The primary heat sink for U2 and U4 are connected to primary return to eliminate the heat sink as a source of radiated/capacitively coupled noise and EMI.

4.1.2 Inrush Limiting

Thermistor RT1 provides inrush limiting. It is shorted by relay RL1 during normal operation, gated by activation of the main output voltage increasing efficiency by approximately 1 - 1.5%.

The relay RL1 turns on when the main output supply reaches regulation, shorting out thermistor RT1.

4.1.3 Main PFC Stage

The boost converter stage consists of the boost inductor L3 and the PFS7328H IC U2. This converter stage operates as a PFC boost converter, thereby maintaining a sinusoidal input current to the power supply while regulating the output DC voltage.



During start-up, diode D2 provides an inrush current path to the output capacitor C12, bypassing the switching inductor L3 and PFS device U2 in order to prevent a resonant interaction between the switching inductor and output capacitor.

Capacitor C10 provide a short, high-frequency return path to RTN for improved EMI results and to reduce U2 MOSFET drain voltage overshoot after turn-off. Capacitor C15 decouples and bypasses the U2 VCC pin.

The input voltage of the power supply is sensed by the IC U2 using resistors R3, R4 and R5. The capacitor C13 bypasses the V pin on IC U2.

An output voltage resistive divider network consisting of resistors R7, R8, R9 and R13 provide a scaled voltage proportional to the output voltage as feedback to the controller IC U2. The capacitor C11 provides fast dv/dt feedback to the U2 FB pin for undershoot and overshoot response of the PFC circuit.

Resistor R12 and capacitor C17 provide the control loop dominant pole. C18, C16 and R14 attenuate high-frequency noise.

The resistor R11 in series with capacitor C17 provides low frequency compensation zero while diode D3 protects against error operation caused by an accidentally shorted C17.

4.1.4 Standby Supply

Components U7, T2, D11, C45, D8 and VR1 comprise a simple isolated flyback supply to provide standby power. Transformer T2 was designed by using EF20 core.

Using ON/OFF control, U7 skips switching cycles to regulate the output voltage, based on feedback to its ENABLE/UNDERVOLTAGE (EN/UV) pin. The EN/UV pin current is sampled, just prior to each switching cycle, to determine if that switching cycle should be enabled or disabled. If the EN/UV pin current is $<115\ \mu\text{A}$, the next switching cycle begins, and is terminated when the current through the MOSFET reaches the internal current limit threshold. To evenly spread switching cycles, preventing group pulsing, the EN/UV pin threshold current is modulated between $115\ \mu\text{A}$ and $60\ \mu\text{A}$ based on the state during the previous cycle. A state-machine within the controller adjusts the power MOSFET current limit threshold to one of four levels, depending on the load being demanded from the supply. As the load on the supply drops, the current limit threshold is reduced. This ensures that the effective switching frequency stays above the audible range until the transformer flux density is low. When the standard production technique of dip varnishing is used for the transformer, audible noise is practically eliminated.

Diode D11 rectifies the output of T2. Output voltage ripple was minimized by using a low ESR capacitor for C45. A post filter L5 and C46 attenuates the high frequency switching noise.



Main and standby outputs were ORed by using D12 and D13 in order to improve total system efficiency.

The supply's output voltage regulation set point is set by the resistors R53 and R54, along with the U8 reference voltage. Resistor R50 limits the maximum current during load transients. When the output voltage rises above the set point, the LED in U6 becomes forward biased. On the primary-side, the phototransistor of U6 turns on and draws current out of the EN/UV pin of U7. Just before the start of each switching cycle, the controller checks the EN/UV pin current. If the current flowing out of the EN/UV pin is greater than 115 μ A, that switching cycle will be disabled. As switching cycles are enabled and disabled, the output voltage is kept very close to the regulation set point.

4.2 LLC Converter

The schematic in Figure 5 depicts a 12 V, 237 W LLC DC-DC converter implemented using the LCS703HG.

4.3 Primary

Integrated circuit U4 incorporates the control circuitry, drivers and output MOSFETs necessary for an LLC resonant half-bridge (HB) converter. The HB output of U4 drives output transformer T1 via a blocking/resonating capacitor (C24). This capacitor was rated for the operating ripple current and to withstand the high voltages present during fault conditions.

Transformer T1 was designed for a leakage inductance of 115 μ H. This, along with resonating capacitor C24, sets the primary series resonant frequency at ~90 kHz according to the equation:

$$f_R = \frac{1}{6.28\sqrt{L_L \times C_R}}$$

f_R is the series resonant frequency in Hertz, L_L is the transformer leakage inductance in Henries, and C_R is the value of the resonating capacitor (C24) in Farads.

The transformer turns ratio was set by adjusting the primary turns such that the operating frequency at nominal input voltage and full load is close to, but slightly less than, the previously described resonant frequency.

An operating frequency of 90 kHz was found to be a good compromise between transformer size, output filter capacitance (enabling ceramic capacitors), and efficiency.

The number of secondary winding turns was chosen to provide a good compromise between core and copper losses. AWG #40 Litz wire was used for the primary and AWG #38 Litz wire, for the secondary, this combination providing high-efficiency at the



operating frequency (~90 kHz). The number of strands within each gauge of Litz wire was chosen as a balance between winding fit and copper losses.

The core material selected was PC95 (from TDK). This material yielded better (low-loss) performance.

Components D4, R19, and C23 comprise the bootstrap circuit to supply the internal high-side driver of U4.

Components C20 and R20, provide filtering and bypassing of the +12 V input which is the V_{CC} supply for U4. *Note: V_{CC} voltage of >15 V may damage U4.*

Voltage divider resistors R15, R16, R17 and R18 sets the high-voltage turn-on, turn-off, and overvoltage thresholds of U4. The voltage divider values are chosen to set the LLC turn-on point at 360 VDC and the turn-off point at 285 VDC, with an input overvoltage turn-off point at 473 VDC.

Capacitor C22 is a high-frequency bypass capacitor for the +380 V input, connected with short traces between the D and S1/S2 pins of U4.

Capacitor C30 forms a current divider with C24, and is used to sample a portion of the primary current. Resistor R29 senses this current, and the resulting signal is filtered by R28 and C29. Capacitor C30 should be rated for the peak voltage present during fault conditions, and should use a stable, low-loss dielectric such as metalized film, SL ceramic, or NPO/COG ceramic. The capacitor used in the DER-385 is a ceramic disc with "SL" temperature characteristic, commonly used in the drivers for CCFL tubes. The values chosen set the 1 cycle (fast) current limit at 6.52 A and the 7-cycle (slow) current limit at 3.62 A, according to the equation:

$$I_{CL} = \frac{0.5}{\left(\frac{C30}{C24 + C30} \right) \times R29}$$

I_{CL} is the 7-cycle current limit in Amperes, R29 is the current limit resistor in Ohms, and C24 and C30 are the values of the resonating and current sampling capacitors in nanofarads, respectively. For the one-cycle current limit, substitute 0.9 V for 0.5 V in the above equation.

Resistor R28 is set to 220 Ω , the minimum recommended value. The value of C29 is set to 1 nF to avoid nuisance tripping due to noise, but not so high as to substantially affect the current limit set values as calculated above. These components should be placed close to the IS pin for maximum effectiveness. The IS pin can tolerate negative currents, the current sense does not require a complicated rectification scheme.



The Thevenin equivalent combination of R23 and R27 sets the dead-time at 625 ns and maximum operating frequency for U4 at 434 kHz. The F_{MAX} input of U4 is filtered by C27. The combination of R23 and R27 also selects burst mode “2” for U4. This sets the lower and upper burst threshold frequencies at 160 kHz and 187 kHz, respectively.

The FEEDBACK pin has an approximate characteristic of 2.6 kHz per μA into the FEEDBACK pin. As the current into the FEEDBACK pin increases so does the operating frequency of U4, reducing the output voltage. The series combination of R21 and R22 sets the minimum operating frequency for U9 to ~62 kHz. This value was set to be lower than the frequency required for regulation a full load and minimum bulk capacitor voltage. Resistor R21 is bypassed by C19 to provide output soft start during start-up by initially allowing a higher current to flow into the FEEDBACK pin when the feedback loop is open. This causes the switching frequency to start high and then decrease until the output voltage reaches regulation. Resistor R21 is typically set at the same value as R23 so that the initial frequency at soft-start is equal to the maximum switching frequency as set by R23. If the value of R22 is less than this, it will cause a delay before switching occurs when the input voltage is applied.

Optocoupler U3 drives the U4 FEEDBACK pin through R24 which limits the maximum optocoupler current into the FEEDBACK pin. Capacitor C28 filters the FEEDBACK pin. Resistor R25 loads the optocoupler output to force it to run at a relatively high quiescent current, increasing its gain. Resistors R24 and R25 also improve large signal step response and burst mode output ripple. Diode D5 isolates R25 from the F_{MAX} /soft start network.

4.4 Output Synchronous Rectification

The output of transformer T1 is rectified and filtered by using synchronous rectification controller U9, MOSFETs Q2, Q3, diodes D6, D7 and capacitors C31, C32. These capacitors are organic polymer capacitors, carefully chosen for output ripple current rating. Synchronous rectification was chosen in order to meet 80 plus platinum efficiency requirements. MOSFETs Q2 and Q3 were selected optimally to get higher MOSFET conduction period and higher efficiency. Utmost care has to be taken while laying out the synchronous rectifier controller and its associated components. -12 mV (instead of -25 mV) drain voltage sensing turnoff threshold was chosen in order to get higher MOSFET conduction period at a given load. Diodes D6 and D7 were used in order to improve the efficiency further by avoiding MOSFET body diode conduction when the MOSFET was turned off. Additional output filtering is provided by L4 and C33.

Resistors R37 and R38, along with the U5 reference voltage, set the output voltage of the supply. Error amplifier U5 drives the feedback optocoupler U3 via R33. Components C34, C26, and C37, R33, R32, R36, and R26 determine the gain-phase characteristics of the supply. These values were chosen to provide stable operation at nominal and extreme load/input voltage combinations. Resistor R34 allows the minimum required operating current to flow in U3 when no current flow occurs in the LED of optocoupler U3.



Components C35 and R35 are used for soft finish network to eliminate output overshoot at turn-on.



5 PCB Layout

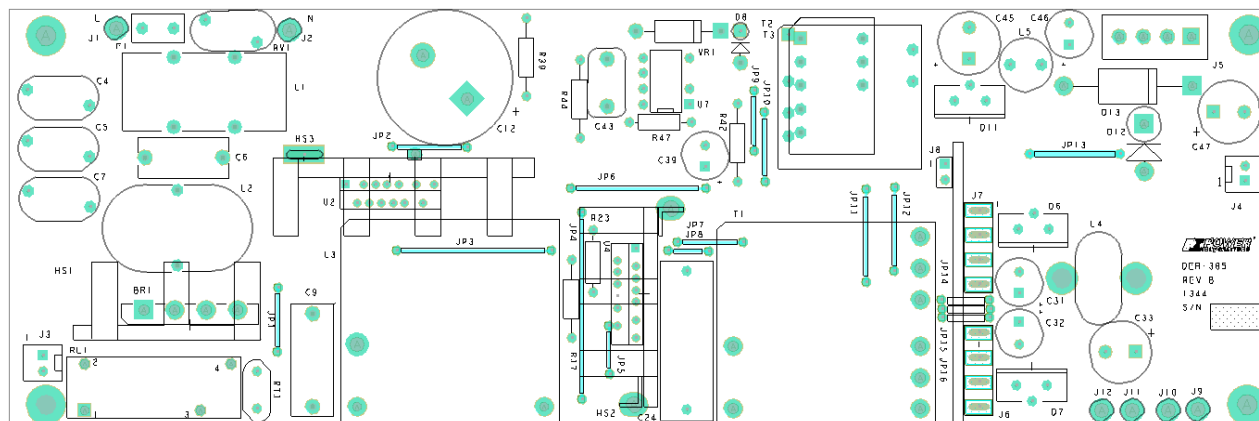


Figure 8 – Printed Circuit Layout – Main Board, Top Side.

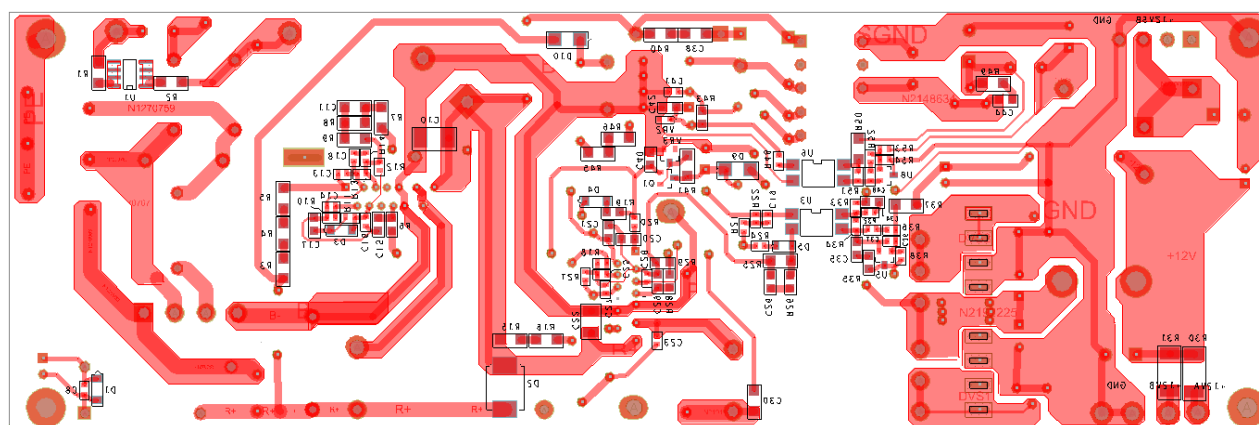


Figure 9 – Printed Circuit Layout – Main Board, Bottom Side.



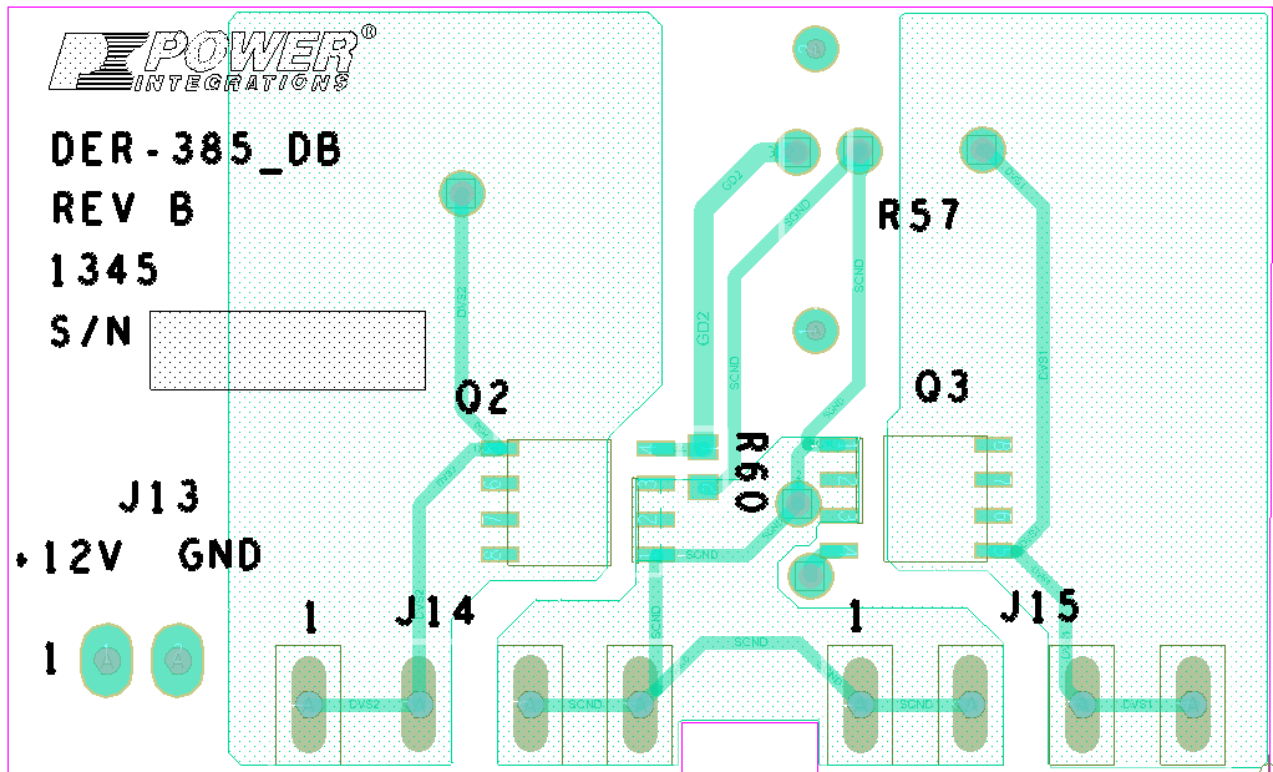


Figure 10 – Printed Circuit Layout – Daughter Board, Top Side.

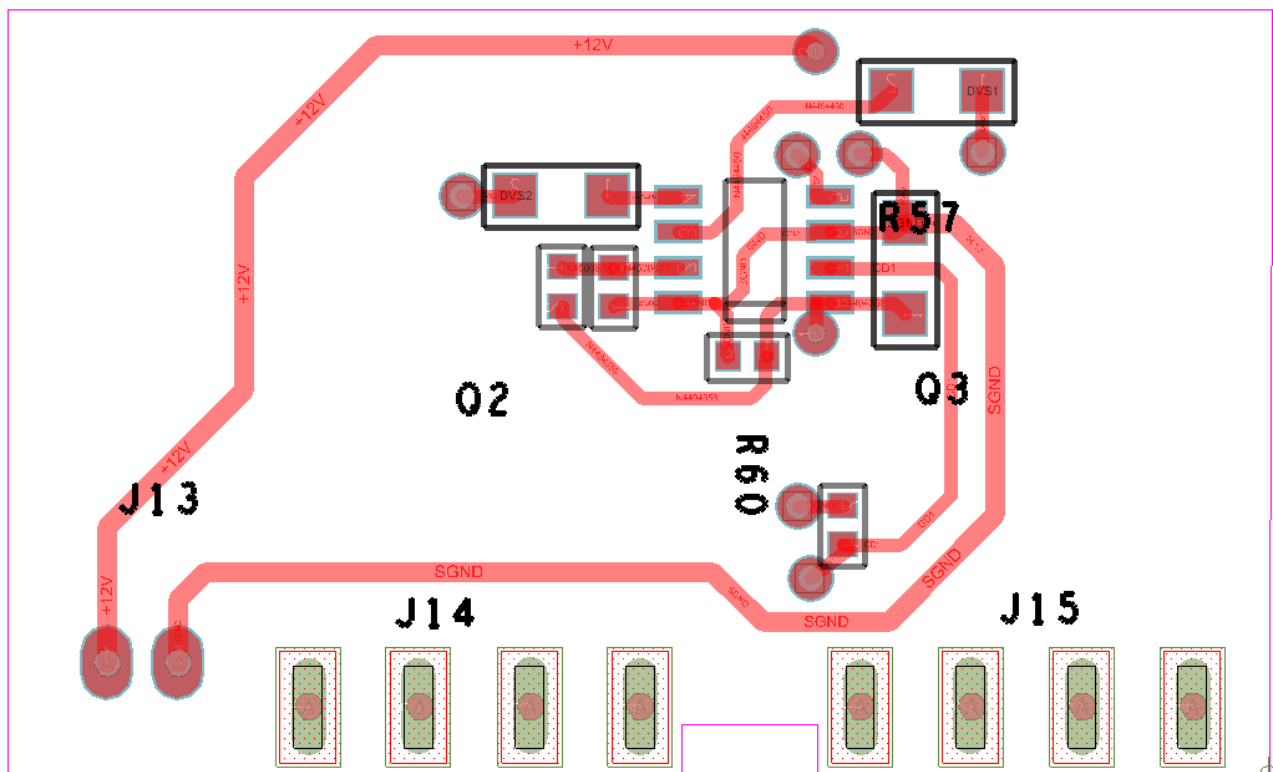


Figure 11 – Printed Circuit Layout – Daughter Board, Bottom Side.



6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
Main Board BOM					
1	1	BR1	800 V, 8 A, Bridge Rectifier, GBU Case	GBU8K-BP	Micro Commercial
2	2	C1 C2	330 pF, 250 VAC, Film, X1Y1	CD90-B2GA331KYNS	TDK
3	1	C3	220 nF, 275VAC, Film, X2	R46KI322050M2K	Kemet
4	2	C4 C5	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
5	1	C6	150 nF, 275 VAC, Film, X2	LE154-M	OKAYA
6	1	C7	1.5 nF, Ceramic, Y1	440LD15-R	Vishay
7	2	C8 C41	100 nF 50 V, Ceramic, X7R, 0603	C1608X7R1H104K	TDK
8	1	C9	680 nF, 450 VDC, Disc Ceramic	ECQ-E2W684KH	Panasonic
9	1	C10	10 nF, 1 kV, Ceramic, X7R, 1812	VJ1812Y103KXGAT	Vishay
10	1	C11	47 nF, 200 V, Ceramic, X7R, 1206	12062C473KAT2A	AVX
11	1	C12	220 μ F, 450 V, Electrolytic, (22 x 45)	ESMQ451VSN221MP45S	United Chemi-con
12	3	C13 C16 C28	22 nF 50 V, Ceramic, X7R, 0603	C1608X7R1H223K	TDK
13	1	C14	1000 pF, 100 V, Ceramic, COG, 0603	C1608C0G2A102J	TDK
14	2	C15 C35	3.3 μ F, 25 V, Ceramic, X7R, 0805	C2012X7R1E335K	TDK
15	1	C17	2.2 μ F, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
16	2	C18 C48	47 nF 25 V, Ceramic, X7R, 0603	CC0603KRX7R8BB473	Yageo
17	1	C19	330 nF, 16 V, Ceramic, X7R, 0603	C1608X7R1C334K080AC	TDK
18	2	C20 C21	1 μ F, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
19	1	C22	22 nF, 630 V, Ceramic, X7R, 1210	GRM32QR72J223KW01L	Murata
20	1	C23	220 nF 50 V, Ceramic, X7R, 0603	CGA3E3X7R1H224K	TDK
21	1	C24	27 nF, 1600 V, Film	BFC238350273	Vishay
22	2	C25 C27	4.7 nF 50 V, Ceramic, X7R, 0603	GRM188R71H472KA01D	Murata
23	1	C26	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
24	1	C29	1 nF, 50 V, Ceramic, X7R, 0805	08055C102KAT2A	AVX
25	1	C30	100 pF, 1000 V, Ceramic, NPO, 1206	102R18N101JV4E	Johanson Dielectrics
26	2	C31 C32	270 μ F, 16 V, Al Organic Polymer, Gen. Purpose, 20%	RL81C271MDN1KX	Nichicon
27	1	C33	1500 μ F, 16 V, Electrolytic, Low ESR, 37 m Ω , (10 x 30)	ELXZ160ELL152MJ30S	Nippon Chemi-Con
28	1	C34	6.8 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB682	Yageo
29	1	C37	10 nF 50 V, Ceramic, X7R, 0603	C0603C103K5RACTU	Kemet
30	1	C39	330 μ F, 25 V, Electrolytic, Low ESR, 90 m Ω , (8 x 15)	ELXZ250ELL331MH15D	Nippon Chemi-Con
31	1	C40	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
32	1	C42	220 pF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB221	Yageo
33	1	C43	33 nF, 400 V, Film	ECQ-E4333KF	Panasonic
34	1	C44	470 pF, 250 V, Ceramic, GCM, 0805	GCM21A7U2E471JX01D	Murata
35	1	C45	1000 μ F, 16 V, Electrolytic, (10 x 16)	KMG16WV1000UF10X16	Sam Young
36	1	C46	330 μ F, 16 V, Electrolytic, Low ESR, 120 m Ω , (8 x 12)	ELXZ160ELL331MH12D	Nippon Chemi-Con
37	2	D1 D3	130 V, 5%, 250 mW, SOD-123	BAV116W-7-F	Diodes, Inc.
38	1	D2	DIODE GEN PURPOSE, 800 V, 8 A, SMC	S8KC-13	Diodes, Inc.
39	1	D4	600 V, 1 A, Ultrafast Recovery, 75 ns, SOD-123	UFM15PL-TP	Micro Commercial
40	1	D5	75 V, 0.15 A, Switching, SOD-323	BAV16WS-7-F	Diodes, Inc.
41	2	D6 D7	Diode SBR 40 V, 30 A, TO220AB	SBR30A40CT	Diodes, Inc.
42	1	D8	1000 V, 1 A, Fast Recovery Diode, GP DO-41	FR107G-B	Rectron
43	1	D9	200 V, 1 A, Fast Recovery, 150 ns, SMA	RS1D-13-F	Diodes, Inc.
44	1	D10	600 V, 1 A, Standard Recovery, SMA	S1J-13-F	Diodes, Inc.



45	1	D11	Diode SBR 100 V, 5 A, ITO, 220AB	SBR10U100CTFP	Diodes, Inc.
46	2	D12 D13	20 V, 5 A, Schottky, DO-201AD	SB520-E3/54	Vishay
47	1	F1	5 A, 250 V, Slow, Long Time Lag, RST	RST 5	Belfuse
48	3	GREASE1-GREASE3	Thermal Grease, Silicone, 5 oz Tube	CT40-5	ITW Chemtronics
49	1	HEATSHRINK1	Heat Shrink 3/16 IN X 4 FT BLACK	FIT221B-3/16 BK100	Alpha Wire
50	1	HS1	Heat Sink, Custom, Al, 3003, 0.090" Thk		Custom
51	1	HS2	Heat Sink, Custom, Al, 3003, 0.090" Thk		Custom
52	1	HS3	Heat Sink, Custom, Al, 3003, 0.078" Thk		Custom
53	6	J1 J2 J9-J12	PCB Terminal Hole, #18 AWG	N/A	N/A
54	2	J3 J4	2 Position (1 x 2) header, 0.1 pitch, Vertical	22-23-2021	Molex
55	1	J5	4 Position (1 x 4) header, 0.156 pitch, Vertical	26-48-1045	Molex
56	1	J8	2 Position (1 x 2) header, 0.1 pitch, Vertical		Molex
57	3	JP1 JP7 JP9	Wire Jumper, Insulated, #24 AWG, 0.4 in	C2003A-12-02	Gen Cable
58	3	JP2 JP10 JP12	Wire Jumper, Insulated, #24 AWG, 0.5 in	C2003A-12-02	Gen Cable
59	1	JP3	Wire Jumper, Insulated, #24 AWG, 1.0 in	C2003A-12-02	Gen Cable
60	1	JP4	Wire Jumper, Insulated, #24 AWG, 1.2 in	C2003A-12-02	Gen Cable
61	2	JP5 JP8	Wire Jumper, Insulated, #24 AWG, 0.3 in	C2003A-12-02	Gen Cable
62	1	JP6	Wire Jumper, Insulated, #24 AWG, 0.9 in	C2003A-12-02	Gen Cable
63	2	JP11 JP13	Wire Jumper, Insulated, #24 AWG, 0.6 in	C2003A-12-02	Gen Cable
64	3	JP14-JP16	Wire Jumper, Insulated, TFE, #22 AWG, 0.3 in	C2004-12-02	Alpha
65	1	L1	9 mH, 5 A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine Technologies
66	1	L2	220 μ H, 3.6 A, Vertical Toroidal	2216-V-RC	Bourns
67	1	L3	Bobbin, PQ32/20, Vertical, 12 pins	YC-PQ3220	Ying Chin
68	1	L4	Custom, DER-385 Main Post Filter Inductor, 500 nH		
69	1	L5	2.2 μ H, 6.0 A	RFB0807-2R2L	Coilcraft
70	4	MTG_HOLE1-MTG_HOLE4	Mounting Hole No 4		
71	4	P3-P6	CONN TERM FEMALE #22-30 AWG TIN	08-50-0113	Molex
72	1	Q1	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401LT1G	Diodes, Inc.
73	2	R1 R2	390 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ394V	Panasonic
74	3	R3 R4 R7	1.50 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
75	3	R5 R45 R46	1.00 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1004V	Panasonic
76	1	R6	4.7 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
77	1	R8	732 k Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7323V	Panasonic
78	1	R9	1.60 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1604V	Panasonic
79	1	R10	49.9 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4992V	Panasonic
80	1	R11	7.5 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ752V	Panasonic
81	1	R12	487 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4873V	Panasonic
82	1	R13	60.4 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF6042V	Panasonic
83	1	R14	3 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
84	2	R15 R16	976 k Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF9763V	Panasonic
85	1	R17	976 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-976K	Yageo
86	1	R18	20 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2002V	Panasonic
87	1	R19	2.2 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ2R2V	Panasonic
88	1	R20	10 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
89	1	R21	5.76 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF5761V	Panasonic
90	1	R22	140 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1403V	Panasonic
91	1	R23	15 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-15K0	Yageo



92	4	R24 R34 R36 R51	1 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
93	1	R25	2.4 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ242V	Panasonic
94	1	R26	330 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ331V	Panasonic
95	1	R27	130 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ134V	Panasonic
96	1	R28	220 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ221V	Panasonic
97	1	R29	37.4 Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF37R4V	Panasonic
98	2	R30 R31	0.002 Ω , 1%, 2 W, Thick Film, 2512	PMR100HZPFV2L00	Rohm Semi
99	1	R32	220 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ221V	Panasonic
100	1	R33	2.15 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2151V	Panasonic
101	1	R35	10 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
102	1	R37	38.3 k Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3832V	Panasonic
103	2	R38 R54	10 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
104	1	R39	1 Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-1R0	Yageo
105	1	R41	3.01 k Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3011V	Panasonic
106	1	R42	23.7 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-23K7	Yageo
107	1	R43	1.2 M Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ125V	Panasonic
108	2	R44 R47	1 M Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-1M00	Yageo
109	1	R48	100 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
110	1	R49	10 Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
111	1	R50	200 Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2000V	Panasonic
112	1	R52	16.9 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1692V	Panasonic
113	1	R53	36.5 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3652V	Panasonic
114	1	RL1	RELAY GEN PURPOSE SPST 8 A 12 V	G6RL-1A-ASI-DC12	OMRON
115	1	RT1	NTC Thermistor, 2.5 Ω , 5 A	SL10 2R505	Ametherm
116	1	RTV1	RTV 670810.10ZCLR Silico	RTV670810.10ZCLR	GE
117	1	RV1	320 V, 23 J, 10 mm, RADIAL	V320LA10P	Littlefuse
118	2	SCREW1 SCREW2	SCREW MACHINE PHIL 4-40 X 5/16 SS	PMSSS 440 0031 PH	Building Fasteners
119	5	SCREW3-SCREW7	SCREW MACHINE PHIL 4-40 X 1/4 SS	PMSSS 440 0025 PH	Building Fasteners
120	4	STDOFF1-STDOFF4	Standoff Hex, 4-40, 0.375" L, Al, F/F	1892	Keystone
121	1	T1	Bobbin, PQ32/30, Vertical, 12 pins	BQ32/30-1112CPFR	TDK
122	1	T2	Bobbin, EF20, Vertical, 10 pins		
123	1	U1	CAPZero, SO-8C	CAP004DG	Power Integrations
124	1	U2	HiperPFS-2, ESIP16/13	PFS7328H	Power Integrations
125	2	U3 U6	Optocoupler, TRAN OUT 4-SMD	HCPL-817-56AE	Avago Technologies
126	1	U4	HiperLCS, ESIP16/13	LCS703HG	Power Integrations
127	2	U5 U8	IC, REG ZENER SHUNT ADJ SOT-23	LM431AIM3/NOPB	National Semi
128	1	U7	TinySwitch-III, DIP-8C	TNY279PG	Power Integrations
129	1	VR1	150 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE150A	Littlefuse
130	1	VR2	9.1 V, 5%, 150 mW, SSMINI-2	DZ2S091M0L	Panasonic
131	1	VR3	13 V, 5%, 225 mW, SOT23	BZX84C13LT1G	On Semi
132	3	WASHER1-WASHER3	WASHER FLAT #4 SS	FWSS 004	Building Fasteners
133	3	WIRE14AWG_INS_J1 WIRE14AWG_INS_J11 WIRE14AWG_INS_J12	Wire, UL1015, #14 AWG, Blk, PVC, Length To be specified by designer	1015-14/41-00	Anixter
134	3	WIRE14AWG_INS_J2 WIRE14AWG	Wire, UL1015, #14 AWG, Red, PVC, Length To be specified by designer	1015-14/41-02	Anixter



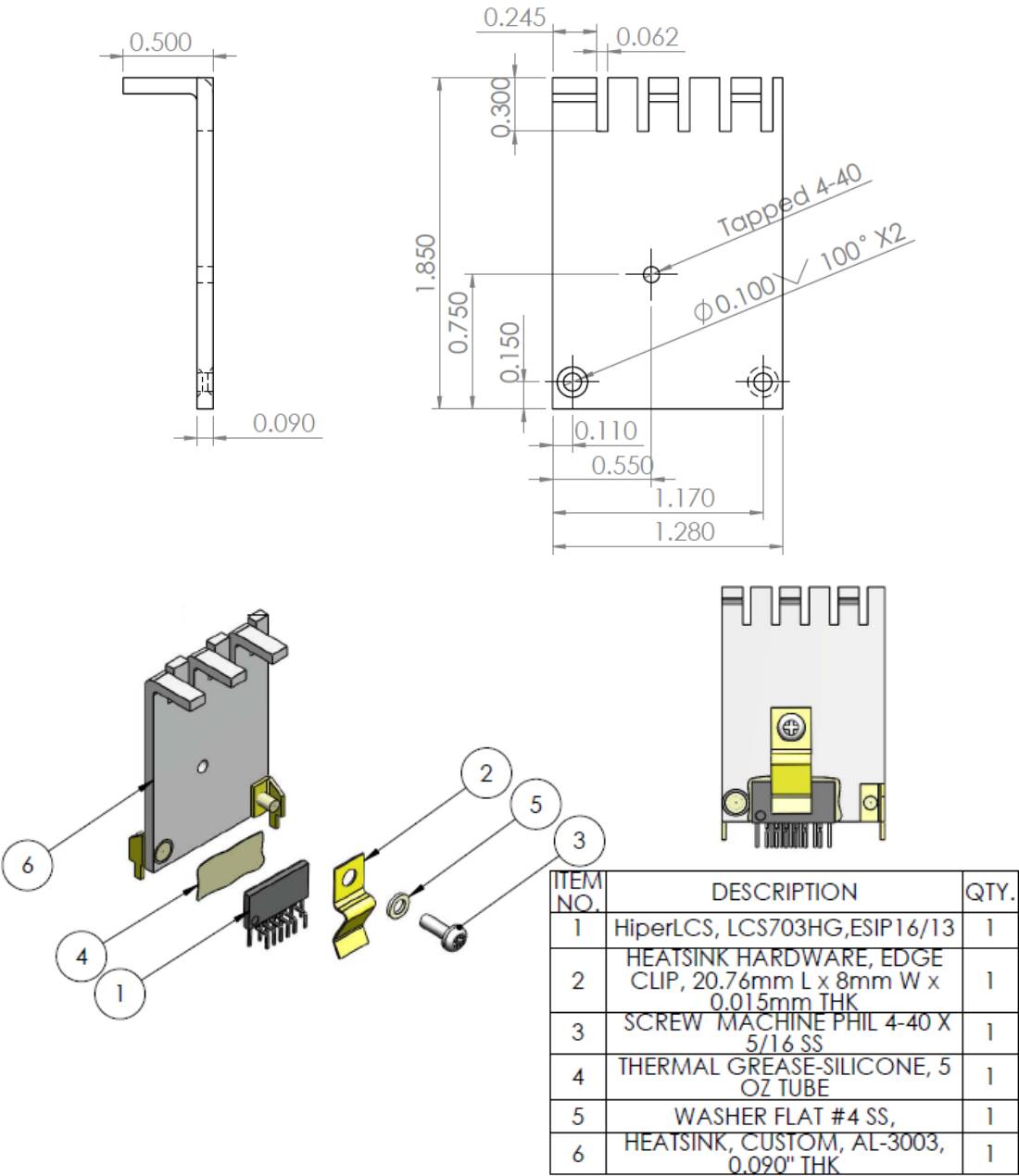
		_INS_J9 WIRE14AWG _INS_J10			
135	1	WIRE22AWG _INS1	Wire, UL1007, #22 AWG, Blk, PVC, Length To be specified by designer	1007-22/7-00	Anixter
136	1	WIRE22AWG _INS2	Wire, UL1007, #22 AWG, Red, PVC, Length To be specified by designer	1007-22/7-02	Anixter
Daughter Board BOM					
1	1	C49	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
2	1	C50	100 nF, 25 V, Ceramic, X7R, 1206	C1206F104K3RACTU	Kemet
3	1	J13	2 Position (1 x 2) header, 0.1 pitch, RT angle, gold	TSW-102-08-L-S-RA	Samtec Inc
4	2	J14 J115	4.00 mm Header, 4 Circuits, 3.81 mm Tail Length	75730-0204	Molex
5	2	Q2 Q3	40 V, 85 A N-Channel, DFN5X6	AON6232	Alpha & Omega Semi
6	1	R56	270 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ274V	Panasonic
7	1	R57	1 Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-1R0	Yageo
8	2	R58 R59	1.5 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ152V	Panasonic
9	2	R60 R61	10 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
10	1	U9	IC SMART DVR SYNC RECT 8-SOIC	SRK2000DTR	ST Micro



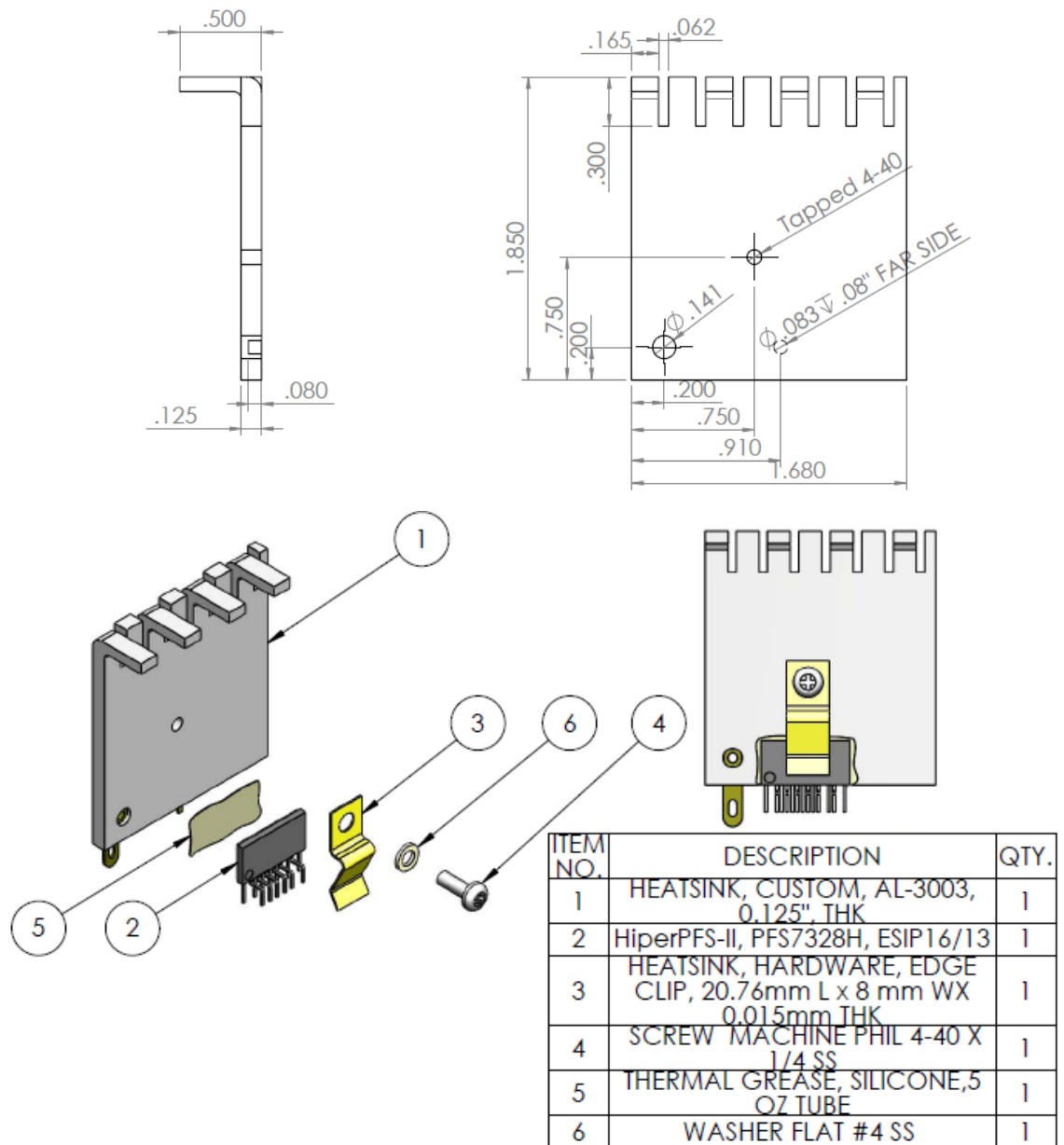
7 Heat Sink Assemblies

7.1 LLC Heat Sink

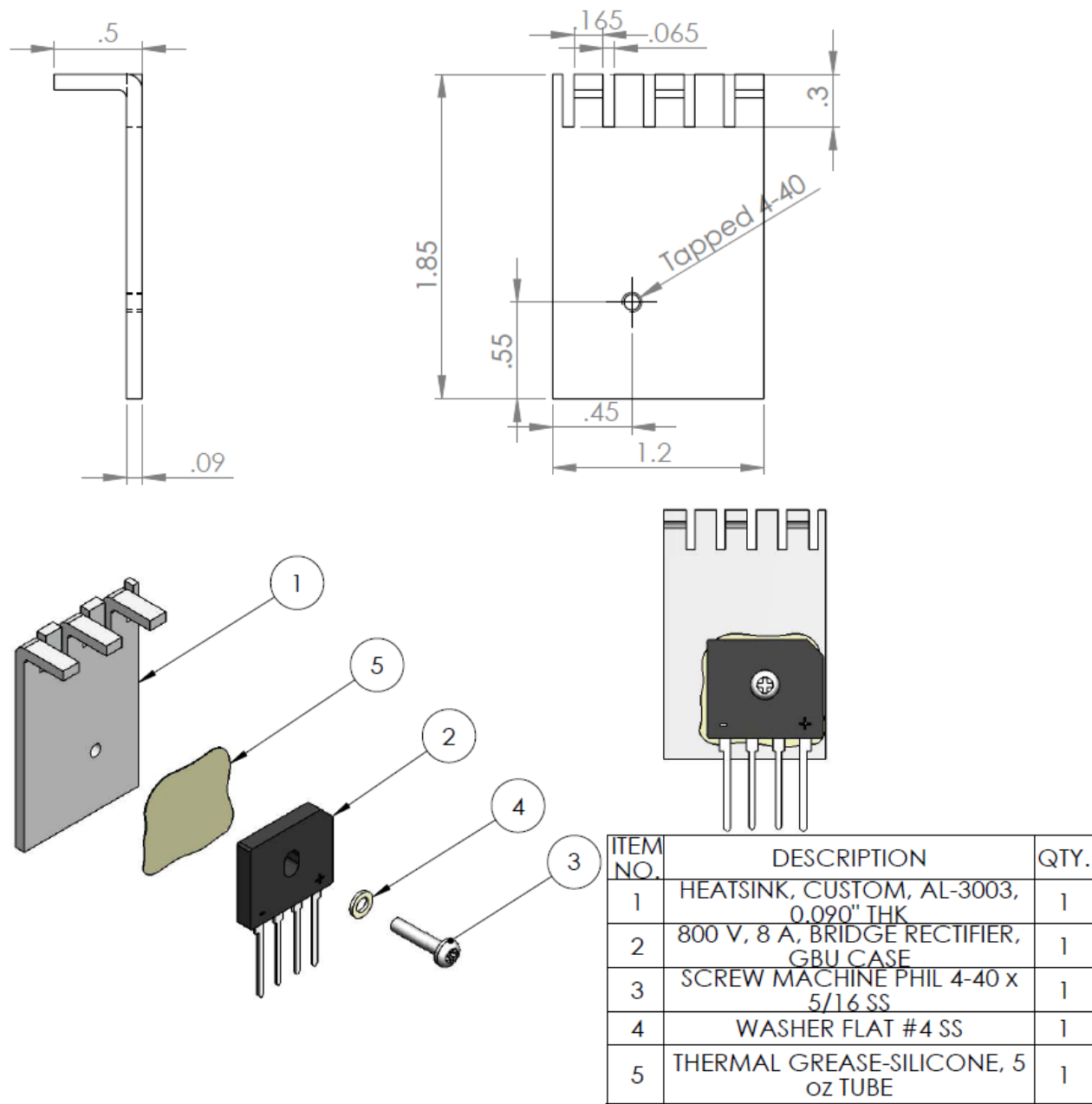
7.1.1 LLC Heat Sink Drawing and Assembly



7.1.2 PFS Heat Sink Drawing and Assembly



7.1.3 Bridge Rectifier Heat Sink Drawing and Assembly



8 Magnetics

8.1 PFC Choke (L3) Specification

8.1.1 Electrical Diagram

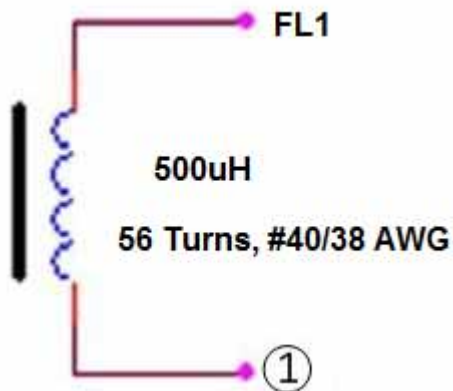


Figure 12 – PFC Choke Electrical Diagram.

8.1.2 Electrical Specifications

Inductance	Pins 1-FL1 measured at 100 kHz, 0.4 V _{RMS}	500 μ H \pm 5%
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8.1.3 Materials

Item	Description
[1]	Core: PQ32/20, PC44 core material.
[2]	Served litz wire: #40 / #38 AWG.

8.1.4 PFC Inductor Final Assembly

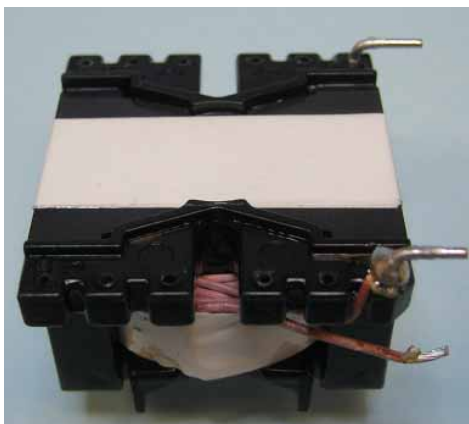


Figure 13 – PFC Choke Final Assembly.

8.2 LLC Transformer (T1) Specification

8.2.1 Electrical Diagram

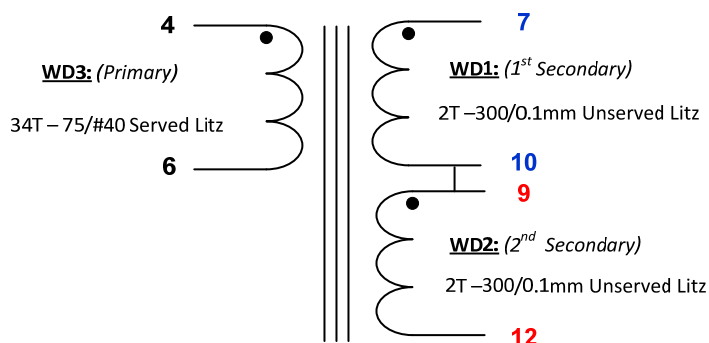


Figure 14 – LLC Transformer Electrical Diagram.

8.2.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 4-6 and pins 7-12.	3000 VAC
Primary Inductance	Pins 4-6, all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	650 μ H \pm 5%.
Resonant Frequency	Pins 4-6, all other windings open	1400 kHz (Min.)
Primary Leakage Inductance	Pins 4-6, with pins 7,9,10 and 12 shorted, measured at 100 kHz, 0.4 V _{RMS} .	115 μ H \pm 10%.

8.2.3 Materials

Item	Description
[1]	Core: PQ32/30-TDK PC95 and gapped ALG 560 nH/T ² .
[2]	Bobbin: PQ32/30-Vertical, 12 pins (6/6).
[3]	Magnet wire: 75 / #40 AWG Served Litz.
[4]	Magnet wire: 300 / 0.1 mm Unserved Litz; or 300/#38 AWG Unserved Litz.
[5]	Margin tape: 3M 44, margin tape, cream, 6.0 mm wide; or equivalent.
[6]	Tape: 3M 1298 Polyester Film, 8.0 mm wide, 2.0 mils thick; or equivalent.
[7]	Tape: 3M 1298 Polyester Film, 18.0 mm wide, 2.0 mils thick or equivalent.
[8]	Teflon tube: #16, Alpha Wire TFT-200016.



8.2.4 Build Diagram

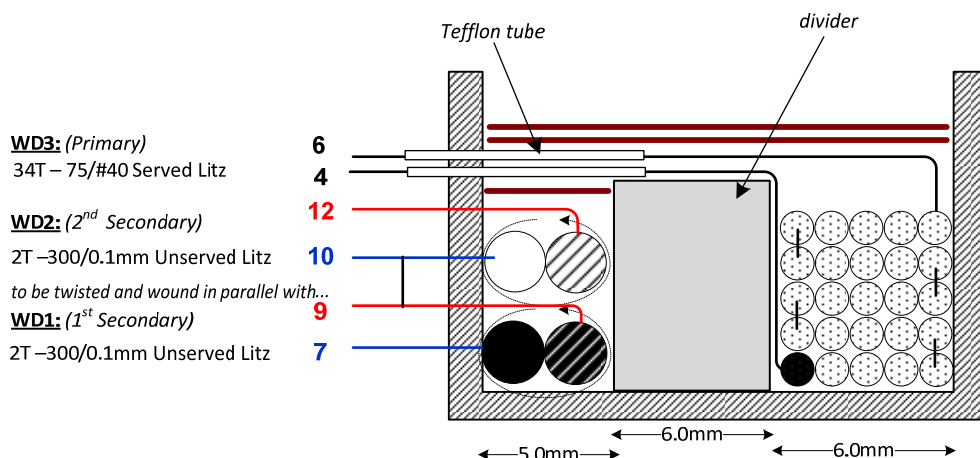


Figure 15 – LLC Transformer Build Diagram.

8.2.5 Winding Instructions

Winding Preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction. Place margin tape item [5] on the bobbin with to create 2 chambers with location shown as in fig. 2 above. Prepare 2 strands of wire item [4] ~ 8" length, tin ends. Label one strand to distinguish from other and designate it as FL1, FL2. Other strand will be designated as FL3 and FL4. Twist these 2 strands together ~8 twists evenly along length leaving 1" free at each end. Tin other ends.
WD1 & WD2 Secondary	Use wires assembly prepared above, start with FL1 on pin 7 and FL3 on pin 9, tightly wind 2 turns in left chamber. Finish with FL2 on pin 10 and FL4 in pin 12. Secure winding with tape item [6].
Insulation	Place 1 layer of tape item [5].
WD3 Primary	Start at pin 4, wind 34 turns of wire item [3] in the right chamber with tight tension and finish at pin 6. Insert Teflon tubes ~ 20 mm long item [8] for both ends of this winding.
Insulation	Place 2 layers of tape item [7].
Final Assembly	Grind, assemble, and secure core halves with tape.

8.3 Standby Transformer (T2) Specification

8.3.1 Electrical Diagram

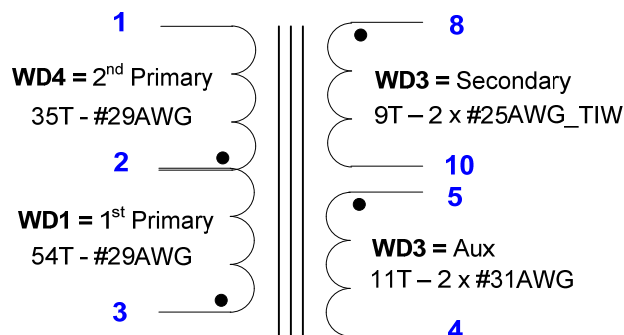


Figure 16 – Transformer Electrical Diagram.

8.3.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-5 to pins 6-10.	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	1157 μ H \pm 10%
Resonant Frequency	Pins 1-3, all other windings open.	1.2 MHz (Min.)
Leakage Inductance	Pins 1-3, with secondary pins shorted, measured at 100 kHz, 0.4 V _{RMS} .	15 μ H (Max.)

8.3.3 Materials

Item	Description
[1]	Core: EF20. part #: PC44EF20-Z.
[2]	Bobbin: EF20, Vertical, 10 pins, (5/5).
[3]	Magnet wire: #29 AWG.
[4]	Magnet wire: #31 AWG.
[5]	Magnet wire: #25 AWG Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 2 mils thick, 20 mm wide.
[7]	Varnish.



8.3.4 Transformer Build Diagram

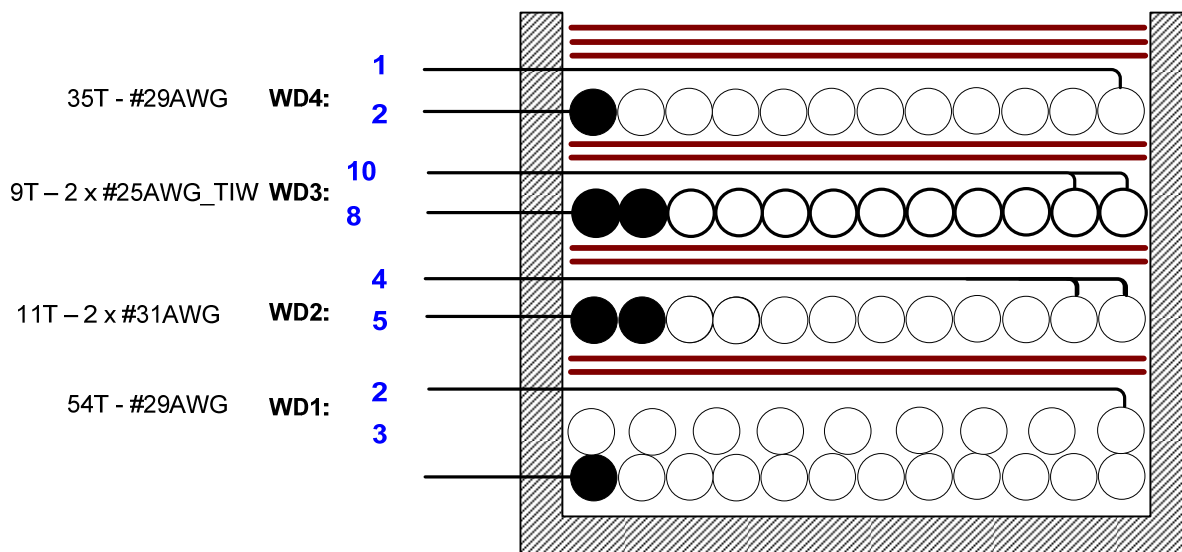


Figure 17 – Bias Transformer Build Diagram.

8.3.5 Transformer Build Instructions

Winding Preparation	Position the bobbin on the mandrel such that the pin side is on the left side of bobbin mandrel. Winding direction is clock-wise direction
WD1 1st Primary	Start at pin 3, wind 54 turns of wire item [3] from left to right with tight tension in two layers, and terminate at pin 2
Insulation	2 layers of tape item [6]
WD2 Auxiliary	Start at pin 5, wind 11 bi-filar turns of wire item [4] from left to right also with tight tension in one layer, at the last turn bring the wire back to the left and terminate at pin 4
Insulation	2 layers of tape item [6]
WD3 Secondary	Start at pin 8 wind 9 bi-filar turns of wire item [5] from left to right also with tight tension in one layer, at the last turn bring the wire back to the left and terminate at pin 10
Insulation	2 layers of tape item [6]
WD4 2nd Primary	Start at pin 2, wind 35 turns of wire item [3] from right to left with tight tension in one layer, at the last turn bring the wire back to the right and terminate at pin 1
Insulation	3 layers of tape item [6]
Finish	Assemble, grind the cores to get 1.157 mH, and secure the cores with tape. Varnish [7]

8.4 Output Inductor (L4) Specification

8.4.1 Electrical Diagram

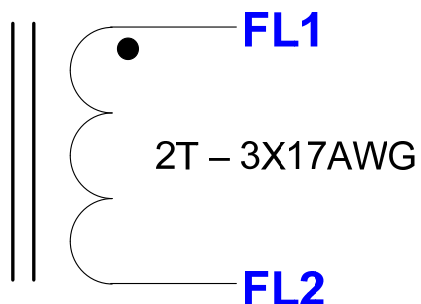


Figure 18 – Inductor Electrical Diagram.

8.4.2 Electrical Specifications

Inductance	Pins FL1-FL2, all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	500 nH, ±15%
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8.4.3 Materials

Item	Description
[1]	Powdered Iron Toroidal Core: Micrometals T60-52.
[2]	Magnet wire: #17 AWG Solderable Double Coated.

9 LLC Converter Design Spreadsheet

HiperLCS_042413; Rev.1.3; Copyright Power Integrations 2013	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_042413_Rev1-3.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					
Vbulk_nom	380		380	V	Nominal LLC input voltage
Vbrownout			280	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
Vbrownin			353	V	Startup threshold on bulk capacitor
VOV_shut			465	V	OV protection on bulk voltage
VOV_restart			448	V	Restart voltage after OV protection.
CBULK	220.00		220	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbrownout to change bulk cap value
tHOLDUP			29.5	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs				The spreadsheet assumes AC stacking of the secondaries	
VO1	12.00		12.0	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	19.71		19.7	A	Main output maximum current
VD1	0.10		0.10	V	Forward voltage of diode in Main output
PO1			237	W	Output Power from first LLC output
VO2			0.0	V	Second Output Voltage
IO2			0.0	A	Second output current
VD2			0.70	V	Forward voltage of diode used in second output
PO2			0.00	W	Output Power from second LLC output
P_LLC			237	W	Specified LLC output power
LCS Device Selection					
Device			LCS703		LCS Device
RDS-ON (MAX)			1.12	ohms	RDS-ON (max) of selected device
Coss			312	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
Pcond_loss			2.8	W	Conduction loss at nominal line and full load
Tmax-hs			90	deg C	Maximum heatsink temperature
Theta J-HS			8.7	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			115	deg C	Expected Junction temperature
Ta max			50	deg C	Expected max ambient temperature
Theta HS-A			14	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)					
Vres_target	380.00		380	V	Desired Input voltage at which power train operates at resonance. If greater than Vbulk_nom, LLC operates below resonance at VBULK.
Po			238	W	LLC output power including diode loss
Vo			12.10	V	Main Output voltage (includes diode drop) for calculating Nsec and turns ratio
f_target	90.00		90	kHz	Desired switching frequency at Vbulk_nom. 66 kHz to 300 kHz, recommended 180-250 kHz
Lpar			535	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri	650.00		650	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for slight loss of



					ZVS at ~80% of Vnom
Lres	115.00		115.0	uH	Series inductance or primary leakage inductance of integrated transformer; if left blank auto-calculation is for K=4
Kratio			4.7		Ratio of Lpar to Lres. Maintain value of K such that $2.1 < K < 11$. Preferred Lres is such that $K < 7$.
Cres	27.00		27.0	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec			2.249	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
m			50	%	Leakage distribution factor (primary to secondary). >50% signifies most of the leakage is in primary side. Gap physically under secondary yields >50%, requiring fewer primary turns.
n_eq			15.42		Turns ratio of LLC equivalent circuit ideal transformer
Npri	34.0		34.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target and m=50%
Nsec	2.0		2.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=200 mT, using selected core (below)
f_predicted			92	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_eq and primary turns
f_res			90	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout			62	kHz	Expected switching frequency at Vbrownout, full load. Set HiperLCS minimum frequency to this value.
f_par			38	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion			56	kHz	LLC full load gain inversion frequency. Operation below this frequency results in operation in gain inversion region.
Vinversion			252	V	LLC full load gain inversion point input voltage
Vres_expected			373	V	Expected value of input voltage at which LLC operates at resonance.
RMS Currents and Voltages					
IRMS_LLC_Primary			1.59	A	Primary winding RMS current at full load, Vbulk_nom and f_predicted
Winding 1 (Lower secondary Voltage) RMS current			15.6	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current			9.8	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			0.0	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms			102	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)					
New primary turns			34.0		Trial transformer primary turns; default value is from resonant section
New secondary turns			2.0		Trial transformer secondary turns; default value is from resonant section
New Lpri			650	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres			27.0	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res same as in main resonant section above)



New estimated Lres			115.0	uH	Trial transformer estimated Lres
New estimated Lpar			535	uH	Estimated value of Lpar for trial transformer
New estimated Lsec			2.249	uH	Estimated value of secondary leakage inductance
New Kratio			4.7		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio			15.42		Estimated effective transformer turns ratio
V powertrain inversion new			252	V	Input voltage at LLC full load gain inversion point
f_res_trial			90	kHz	New Series resonant frequency
f_predicted_trial			92	kHz	New nominal operating frequency
IRMS_LLC_Primary			1.59	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current			15.7	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Lower Secondary Voltage Capacitor RMS current			10.2	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			15.7	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Vres_expected_trial			373	V	Expected value of input voltage at which LLC operates at resonance.
Transformer Core Calculations (Calculates From Resonant Parameter Section)					
Transformer Core	PQ32/30		PQ32/30		Transformer Core
Ae			1.61	cm^2	Enter transformer core cross-sectional area
Ve			12.00	cm^3	Enter the volume of core
Aw			95.3	mm^2	Area of window
Bw			18.6	mm	Total Width of Bobbin
Loss density			200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT			6.7	cm	Mean length per turn
Nchambers			2		Number of Bobbin chambers
Wsep	6.00		6.0	mm	Winding separator distance (will result in loss of winding area)
Ploss			2.4	W	Estimated core loss
Bpkfmin			152	mT	First Quadrant peak flux density at minimum frequency.
BAC			205	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
Primary Winding					
Npri			34.0		Number of primary turns; determined in LLC resonant section
Primary gauge	40		40	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Primary litz strands	75		75		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor			50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P			32	mm^2	Winding window area for primary
Fill Factor			66%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary			49.72	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C			113.43	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C			152.00	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current			1.59	A	Measured RMS current through the primary winding



ACR_Trf_Primary			329.24	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss			0.84	W	Total primary winding copper loss at 85 C
Primary Layers			4.84		Number of layers in primary Winding
Secondary Winding 1 (Lower secondary voltage OR Single output)					Note - Power loss calculations are for each winding half of secondary
Output Voltage			12.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns			2.00		Secondary winding turns (each phase)
Sec 1 RMS current (total, AC+DC)			15.6	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Winding current (DC component)			9.86	A	DC component of winding current
Winding current (AC RMS component)			12.10	A	AC component of winding current
Sec 1 Wire gauge			38	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge			0.100	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	300		300		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1			7.82	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1			1.05	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1			1.41	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			1.09	W	Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1			1.41	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1			0.41	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses			1.51	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current			9.8	A	Output capacitor RMS current
Co1	540.00		540.0	uF	Secondary 1 output capacitor
Capacitor ripple voltage			0.5	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			15.6	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 1 Layers	2.00		2.00		Number of layers in secondary 1 Winding
Secondary Winding 2 (Higher secondary voltage)					Note - Power loss calculations are for each winding half of secondary
Output Voltage			0.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns			0.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)			15.6	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)			0.0	A	DC component of winding current
Winding current (AC RMS component)			0.0	A	AC component of winding current
Sec 2 Wire gauge			38	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge			0.100	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands			0		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25			23453.09	m-ohm/m	Resistivity in milli-ohms per meter



C_sec2					
Transformer Secondary MLT			6.71	cm	Mean length per turn
DCR_25C_Sec2			0.00	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2			0.00	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2			0.00	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2			0.00	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses			0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Capacitor RMS current			0.0	A	Output capacitor RMS current
Co2			N/A	uF	Secondary 2 output capacitor
Capacitor ripple voltage			N/A	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			0.0	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 2 Layers			1.00		Number of layers in secondary 2 Winding
Transformer Loss Calculations				Does not include fringing flux loss from gap	
Primary copper loss (from Primary section)			0.84	W	Total primary winding copper loss at 85 C
Secondary copper Loss			1.51	W	Total copper loss in secondary winding
Transformer total copper loss			2.34	W	Total copper loss in transformer (primary + secondary)
AW_S			32.28	mm^2	Area of window for secondary winding
Secondary Fill Factor			49%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz
Signal Pins Resistor Values					
f_min			62	kHz	Minimum frequency when optocoupler is cut-off. Only change this variable based on actual bench measurements
Dead Time	625		625	ns	Dead time
Burst Mode	2		2		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max			434	kHz	Max internal clock frequency, dependent on dead-time setting. Is also start-up frequency
f_burst_start			160	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop			187	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor			14.93	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor			134	k-ohms	Resistor from DT/BF pin to G pin
Rstart	5.76		5.76	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup. Use default value unless additional start-up delay is desired.
Start up delay			1.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin			133.3	k-ohms	Resistor from VREF pin to FB pin, to set min operating frequency; This resistor plus Rstart determine f_MIN. Includes 7% HiperLCS frequency tolerance to ensure f_min is below f_brownout
C_softstart			0.33	uF	Softstart capacitor. Recommended values are between



					0.1 uF and 0.47 uF
Ropto			2.4	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor	20.00		20.0	k-ohm	Lower resistor in OV/UV pin divider
OV/UV pin upper resistor			2.92	M-ohm	Total upper resistance in OV/UV pin divider
LLC Capacitive Divider Current Sense Circuit					
Slow current limit	3.62		3.62	A	8-cycle current limit - check positive half-cycles during brownout and startup
Fast current limit			6.52	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor	100		100	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor			37.4	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor			220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor			1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency			724	kHz	This pole attenuates IS pin signal
Loss Budget					
LCS device					
Conduction loss			2.8	W	Conduction loss at nominal line and full load
Output diode Loss			2.0	W	Estimated diode losses
Transformer estimated total copper loss			2.34	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss			2.4	W	Estimated core loss
Total transformer losses			4.7	W	Total transformer losses
Total estimated losses			9.6	W	Total losses in LLC stage
Estimated Efficiency			96%	%	Estimated efficiency
PIN			246	W	LLC input power
Secondary Turns and Voltage Centering Calculator					This is to help you choose the secondary turns - Outputs not connected to any other part of spreadsheet
V1			12.00	V	Target regulated output voltage Vo1. Change to see effect on slave output
V1d1			0.10	V	Diode drop voltage for Vo1
N1			3.00		Total number of turns for Vo1
V1_Actual			12.00	V	Expected output
V2			0.00	V	Target output voltage Vo2
V2d2			0.70	V	Diode drop voltage for Vo2
N2			1.00		Total number of turns for Vo2
V2_Actual			3.33	V	Expected output voltage
Separate Series Inductor (For Non-Integrated Transformer Only)					Not applicable if using integrated magnetics - not connected to any other part of spreadsheet
Lsep			115.00	uH	Desired inductance of separate inductor
Ae_Ind			0.53	cm^2	Inductor core cross-sectional area
Inductor turns			27		Number of primary turns
BP_fnom			194	mT	AC flux for core loss calculations (at f_predicted and full load)
Expected peak primary current			3.6	A	Expected peak primary current
BP_fmin			294	mT	Peak flux density, calculated at minimum frequency fmin
Inductor Litz gauge			40	AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor			0.080	mm	Equivalent diameter of wire in metric units



Metric Wire gauge					
Inductor litz strands			125.00		Number of strands used in Litz wire
Inductor parallel wires			1		Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Sep_Ind			29.8	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT			7.00	cm	Mean length per turn
Inductor DCR 25 C			56.4	m-ohm	Estimated resistance at 25 C (for reference)
Inductor DCR 100 C			75.6	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor			120.9	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss			0.31	W	Total primary winding copper loss at 85 C
Feedback section					
VMAIN	Auto		12.0		Output voltage rail that optocoupler LED is connected to
ITL431_BIAS			1.0	mA	Minimum operating current in TL431 cathode
VF			1.0	V	Typical Optocoupler LED forward voltage at IOPTO_BJTMAX (max current)
VCE_SAT			0.3	V	Optocoupler transistor saturation voltage
CTR_MIN			0.8		Optocoupler minimum CTR at VCE_SAT and at IOPTO_BJT_MAX
VTL431_SAT			2.5	V	TL431 minimum cathode voltage when saturated
RLED_SHUNT			1.0	k-ohms	Resistor across optocoupler LED to ensure minimum TL431 bias current is met
ROPTO_LOAD	2.40		2.40	k-ohms	Resistor from optocoupler emitter to ground, sets load current
IFMAX			177.70	uA	FB pin current when switching at FMAX (e.g. startup)
IOPTO_BJT_MAX			1.42	mA	Optocoupler transistor maximum current - when bursting at FMAX (e.g. startup)
RLED_SERIES_MAX			2.76	k-ohms	Maximum value of gain setting resistor, in series with optocoupler LED, to ensure optocoupler can deliver IOPTO_BJT_MAX. Includes -10% tolerance factor.



10 Standby Converter Design Spreadsheet

ACDC_TinySwitch-III_042413; Rev.1.27; Copyright Power Integrations 2008	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-III_042413_Rev1-27.xls; TinySwitch-III Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	11.50			Volts	Output Voltage (at continuous power)
IO	1.57			Amps	Power Supply Output Current (corresponding to peak power)
Power			18.055	Watts	Continuous Output Power
n	0.70				Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z	0.50				Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC	3.00			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	220.00		220	uFarads	Input Capacitance
ENTER TinySwitch-III VARIABLES					
TinySwitch-III	TNY279G		TNY279G		User defined TinySwitch-III
Chosen Device		TNY279G			
Chose Configuration	STD		Standard Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.605	Amps	Minimum Current Limit
ILIMITTYP			0.650	Amps	Typical Current Limit
ILIMITMAX			0.709	Amps	Maximum Current Limit
fSmin			124000	Hertz	Minimum Device Switching Frequency
I ² fmin			50.193	A ² kHz	I ² f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR			120	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	Volts	TinySwitch-III on-state Drain to Source Voltage
VD			0.7	Volts	Output Winding Diode Forward Voltage Drop
KP			0.60		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.34		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB	14		14.00	Volts	Bias Winding Voltage
VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
NB			10.33		Bias Winding Number of Turns
VZOV			20.00	Volts	Over Voltage Protection zener diode voltage.
UVLO VARIABLES					
V_UV_TARGET			124.49	Volts	Target DC under-voltage threshold, above which the power supply will start
V_UV_ACTUAL			119.70	Volts	Typical DC start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			4.89	Mohms	Calculated value for UV Lockout resistor
RUV_ACTUAL			4.70	Mohms	Closest standard value of resistor to RUV_IDEAL
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EF20		EF20		Enter Transformer Core
Core		EF20		P/N:	PC40EF20-Z
Bobbin		EF20_BOB		P/N:	EF20_BOBBIN



		BIN			
AE			0.335	cm ²	Core Effective Cross Sectional Area
LE			4.49	cm	Core Effective Path Length
AL			1570	nH/T ²	Ungapped Core Effective Inductance
BW			12.2	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			3		Number of Primary Layers
NS			9		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			113	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.54		Duty Ratio at full load, minimum primary inductance and minimum input voltage
Iavg			0.25	Amps	Average Primary Current
IP			0.61	Amps	Minimum Peak Primary Current
IR			0.36	Amps	Primary Ripple Current
IRMS			0.38	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1157	uHenries	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 1041 uH
LP_TOLERANCE			10	%	Primary inductance tolerance
NP			89		Primary Winding Number of Turns
ALG			148	nH/T ²	Gapped Core Effective Inductance
BM			2766	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			828	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1675		Relative Permeability of Ungapped Core
LG			0.26	mm	Gap Length (Lg > 0.1 mm)
BWE			36.6	mm	Effective Bobbin Width
OD			0.41	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.35	mm	Bare conductor diameter
AWG			28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			161	Cmils	Bare conductor effective area in circular mils
CMA			430	Cmils/Am p	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			5.95	Amps	Peak Secondary Current
IS RMS			3.42	Amps	Secondary RMS Current
IRIPPLE			3.04	Amps	Output Capacitor RMS Ripple Current
CMS			684	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			647	Volts	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			50	Volts	Output Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					



VO1			11.5	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			1.570	Amps	Output DC Current
PO1			18.06	Watts	Output Power
VD1			0.7	Volts	Output Diode Forward Voltage Drop
NS1			9.00		Output Winding Number of Turns
ISRMS1			3.422	Amps	Output Winding RMS Current
IRIPPLE1			3.04	Amps	Output Capacitor RMS Ripple Current
PIVS1			50	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			SB560		Recommended Diodes for this output
CMS1			684	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.73	mm	Minimum Bare Conductor Diameter
ODS1			1.36	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2				Amps	Output DC Current
PO2			0.00	Watts	Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.52		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3				Amps	Output DC Current
PO3			0.00	Watts	Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.52		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			18.055	Watts	Total Output Power
Negative Output	N/A		N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2



11 Power Factor Controller Design Spreadsheet

Hiper_PFS-II_Boost_101813; Rev.1.2; Copyright Power Integrations 2013	INPUT	INFO	OUTPUT	UNITS	Hiper_PFS- II_Boost_100413_Rev1-2.xls; Continuous Mode Boost Converter Design Spreadsheet
Enter Applications Variables					
Input Voltage Range			Universal		Input voltage range
VACMIN			90	V	Minimum AC input voltage
VACMAX			265	V	Maximum AC input voltage
VBROWNIN			76.69	V	Expected Minimum Brown-in Voltage
VBROWNOUT			68.33	V	Specify brownout voltage.
VO	385.00		385.00	V	Nominal Output voltage
PO	265.00		265.00	W	Nominal Output power
fL			50	Hz	Line frequency
TA Max			40	deg C	Maximum ambient temperature
n			0.93		Enter the efficiency estimate for the boost converter at VACMIN
KP	0.450		0.45		Ripple to peak inductor current ratio at the peak of VACMIN
VO_MIN			365.75	V	Minimum Output voltage
VO_RIPPLE_MAX			20	V	Maximum Output voltage ripple
tHOLDUP	18.00		18	ms	Holdup time
VHOLDUP_MIN			310	V	Minimum Voltage Output can drop to during holdup
I_INRUSH			40	A	Maximum allowable inrush current
Forced Air Cooling	Yes		Yes		Enter "Yes" for Forced air cooling. Otherwise enter "No"
PFS Parameters					
PFS Part Number	Auto		PFS7328H		Selected PFS device
MODE	EFFICIENCY		EFFICIENCY		Mode of operation of PFS. For full mode enter "FULL" otherwise enter "EFFICIENCY" to indicate efficiency mode
R_RPIN			49.9	k-ohms	R pin resistor value
C_RPIN			1.00	nF	R pin capacitor value
IOCP min			9.00	A	Minimum Current limit
IOCP typ			9.50	A	Typical current limit
IOCP max			9.90	A	Maximum current limit
RDSON			0.46	ohms	Typical RDSon at 100 °C
RV1			1.50	Mohms	Line sense resistor 1
RV2			1.50	Mohms	Line sense resistor 2
RV3			1.00	Mohms	Line sense resistor 3
C_VCC			3.30	uF	Supply decoupling capacitor
R_VCC			15.00	ohms	VCC resistor
C_V			22.00	nF	V pin decoupling capacitor
C_C			22.00	nF	Feedback C pin decoupling capacitor
Power_Good_Vo_Threshold_VPG(L)			333.00	V	Vo threshold at which VPG is triggered
PGT set resistor			103.79	kohm	Power good threshold setting resistor
FS_PK			65.4	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
FS_AVG			53.0	kHz	Estimated average frequency of operation over line cycle (at



					VACMIN)
IP			5.25	A	MOSFET peak current
PFS_IRMS			2.59	A	PFS MOSFET RMS current
PCOND_LOSS_PFS			3.08	W	Estimated PFS conduction losses
PSW_LOSS_PFS			1.30	W	Estimated PFS switching losses
PFS_TOTAL			4.39	W	Total Estimated PFS losses
TJ Max			100	deg C	Maximum steady-state junction temperature
Rth-JS			3.00	degC/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			6.52	degC/W	Maximum thermal resistance of heatsink
Basic Inductor Calculation					
LPFC			501	uH	Value of PFC inductor at peak of VACMIN and Full Load
LPFC (0 Bias)			501	uH	Value of PFC inductor at No load. This is the value measured with LCR meter
LP_TOL	5.00		5	%	Tolerance of PFC Inductor Value
LPFC_RMS			3.07	A	Inductor RMS current (calculated at VACMIN and Full Load)
Inductor Construction Parameters					
Core Type	Ferrite		Ferrite		Enter "Sendust", "Pow Iron" or "Ferrite"
Core Material	Auto		PC44		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44 or equivalent for Ferrite cores. Fixed at 52 material for Pow Iron cores.
Core Geometry	Auto		PQ		Select from Toroid or EE for Sendust cores and from EE, or PQ for Ferrite cores
Core	PQ32/20		PQ32/20		Core part number
AE			170	mm^2	Core cross sectional area
LE			55.5	mm	Core mean path length
AL			6530	nH/t^2	Core AL value
VE			9.44	cm^3	Core volume
HT			5.12	mm	Core height/Height of window
MLT			67.1	cm	Mean length per turn
BW			8.98	mm	Bobbin width
NL			56		Inductor turns
LG			1.64	mm	Gap length (Ferrite cores only)
ILRMS			3.07	A	Inductor RMS current
Wire type	LITZ		LITZ		Select between "Litz" or "Regular" for double coated magnet wire
AWG	38		38	AWG	Inductor wire gauge
Filar	40		40		Inductor wire number of parallel strands
OD			0.102	mm	Outer diameter of single strand of wire
AC Resistance Ratio			1.02		Ratio of AC resistance to the DC resistance (using Dowell curves)
J		Warning	9.48	A/mm^2	!!! Warning Current density is too high and may cause heating in the inductor wire. Reduce J
BP_TARGET	3900		3900	Gauss	Target flux density at selected saturation current level (Ferrite cores only)
BM			2765	Gauss	Maximum operating flux density
BP			3871	Gauss	Peak Flux density (Estimated at selected saturation current level)



LPFC_CORE_LOSS			0.09	W	Estimated Inductor core Loss
LPFC_COPPER_LOSS			3.23	W	Estimated Inductor copper losses
LPFC_TOTAL LOSS			3.33	W	Total estimated Inductor Losses
FIT		Warning	102.63%	%	!!! Warning. Windings may not fit on this inductor. Use bigger core or reduce KP or reduce wire gauge if possible
Layers			5.7		Estimated layers in winding
Inductor saturation current	7.000	Info	7.0	A	Inductor saturation current is lower than IOCP_max. Verify transient conditions on the bench.
Critical Parameters					
IRMS			3.17	A	AC input RMS current
IO_AVG			0.69	A	Output average current
Output Diode (DO)					
Part Number	Auto		INTERNAL		PFC Diode Part Number
Type			SPECIAL		Diode Type - Special - Diodes specially catered for PFC applications, SiC - Silicon Carbide type, UF - Ultrafast recovery type
Manufacturer			PI		Diode Manufacturer
VRRM			600	V	Diode rated reverse voltage
IF			3	A	Diode rated forward current
TRR			31	ns	Diode Reverse recovery time
VF			1.47	V	Diode rated forward voltage drop
PCOND_DIODE			1.01	W	Estimated Diode conduction losses
PSW_DIODE			0.90	W	Estimated Diode switching losses
P_DIODE			1.92	W	Total estimated Diode losses
TJ Max			100	deg C	Maximum steady-state operating temperature
Rth-JS			3.85	degC/W	Maximum thermal resistance (Junction to heatsink)
HEATSINK Theta-CA			6.52	degC/W	Maximum thermal resistance of heatsink
Output Capacitor					
CO	Auto		220.00	uF	Minimum value of Output capacitance
VO_RIPPLE_EXPECTED			10.7	V	Expected ripple voltage on Output with selected Output capacitor
T_HOLDUP_EXPECTED			21.6	ms	Expected holdup time with selected Output capacitor
ESR_LF			0.75	ohms	Low Frequency Capacitor ESR
ESR_HF			0.30	ohms	High Frequency Capacitor ESR
IC_RMS_LF			0.49	A	Low Frequency Capacitor RMS current
IC_RMS_HF			1.40	A	High Frequency Capacitor RMS current
CO_LF_LOSS			0.18	W	Estimated Low Frequency ESR loss in Output capacitor
CO_HF_LOSS			0.59	W	Estimated High frequency ESR loss in Output capacitor
Total CO LOSS			0.77	W	Total estimated losses in Output Capacitor
Input Bridge (BR1) and Fuse (F1)					
I ² t Rating			15.45	A ² s	Minimum I ² t rating for fuse
Fuse Current rating			4.96	A	Minimum Current rating of fuse
VF			0.90	V	Input bridge Diode forward Diode drop
IAVG			3.09	A	Input average current at 70 VAC.
PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input



					bridge
PCOND_LOSS_BRIDGE			5.13	W	Estimated Bridge Diode conduction loss
CIN			0.82	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
RT			9.37	ohms	Input Thermistor value
D_Precharge			1N5407		Recommended precharge Diode
Feedback Components					
R1			1.50	Mohms	Feedback network, first high voltage divider resistor
R3			1.60	Mohms	Feedback network, third high voltage divider resistor
R2			787.00	kohms	Feedback network, second high voltage divider resistor
C1			47.00	nF	Feedback network, loop speedup capacitor
R4			60.40	kohms	Feedback network, lower divider resistor
R6			487.00	kohms	Feedback network - pole setting resistor
R7			7.68	kohms	Feedback network - zero setting resistor
C2			47.00	nF	Feedback component- noise suppression capacitor
R5			3.00	kohms	Damping resistor in serie with C3
C3			2.20	uF	Feedback network - compensation capacitor
D1			BAV116		Feedback network - capacitor failure detection Diode
Loss Budget (Estimated at VACMIN)					
PFS Losses			4.39	W	Total estimated losses in PFS
Boost diode Losses			1.92	W	Total estimated losses in Output Diode
Input Bridge losses			5.13	W	Total estimated losses in input bridge module
Inductor losses			3.33	W	Total estimated losses in PFC choke
Output Capacitor Loss			0.77	W	Total estimated losses in Output capacitor
Total losses			15.53	W	Overall loss estimate
Efficiency			0.94		Estimated efficiency at VACMIN. Verify efficiency at other line voltages
CAPZero component selection recommendation					
CAPZero Device			CAP002DG		(Optional) Recommended CAPZero device to discharge X-Capacitor with time constant of 1 second
Total Series Resistance (R1+R2)			1.50	k-ohms	Maximum Total Series resistor value to discharge X-Capacitors
EMI filter components recommendation					
CIN	680.00		680.00	nF	Metallized polyester film capacitor after bridge, ratio with Po
CX2	150.00		150.00	nF	X capacitor after differential mode choke and before bridge, ratio with Po
LDM_calc			305.49	uH	estimated minimum differential inductance to avoid <10kHz resonance in input current
CX1	220.00		220.00	nF	X capacitor before common mode choke, ratio with Po
LCM			10.00	mH	typical common mode choke value



LCM_leakage	60.00		60.00	uH	estimated leakage inductance of CM choke, typical from 30~60uH
CY1 (and CY2)			220.00	pF	Typical Y capacitance for common mode noise suppression
LDM_Actual			245.49	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
Note: CX2 can be placed between CM chock and DM choke depending on EMI design requirement.					

Note:

There is a warning in the spreadsheet for current density in PFC choke. Whenever such a warning is issued, thermal performance of the PFC choke should be checked while operating continuously at the lowest input voltage. In this design, it was found that the temperature rise of the choke was within acceptable limits with the available airflow.

There is a warning in the spreadsheet for FIT factor, however when wounding the choke it was found that the winding can be accommodated without any problems.



12 Performance Data

All measurements were taken at room temperature and 50/60 Hz input frequency unless otherwise specified, Output voltage measurements were taken at the output connectors.

12.1 System Efficiency

Figures below show the total supply efficiency (PFC and LLC stages). AC input was supplied using a sine wave source.

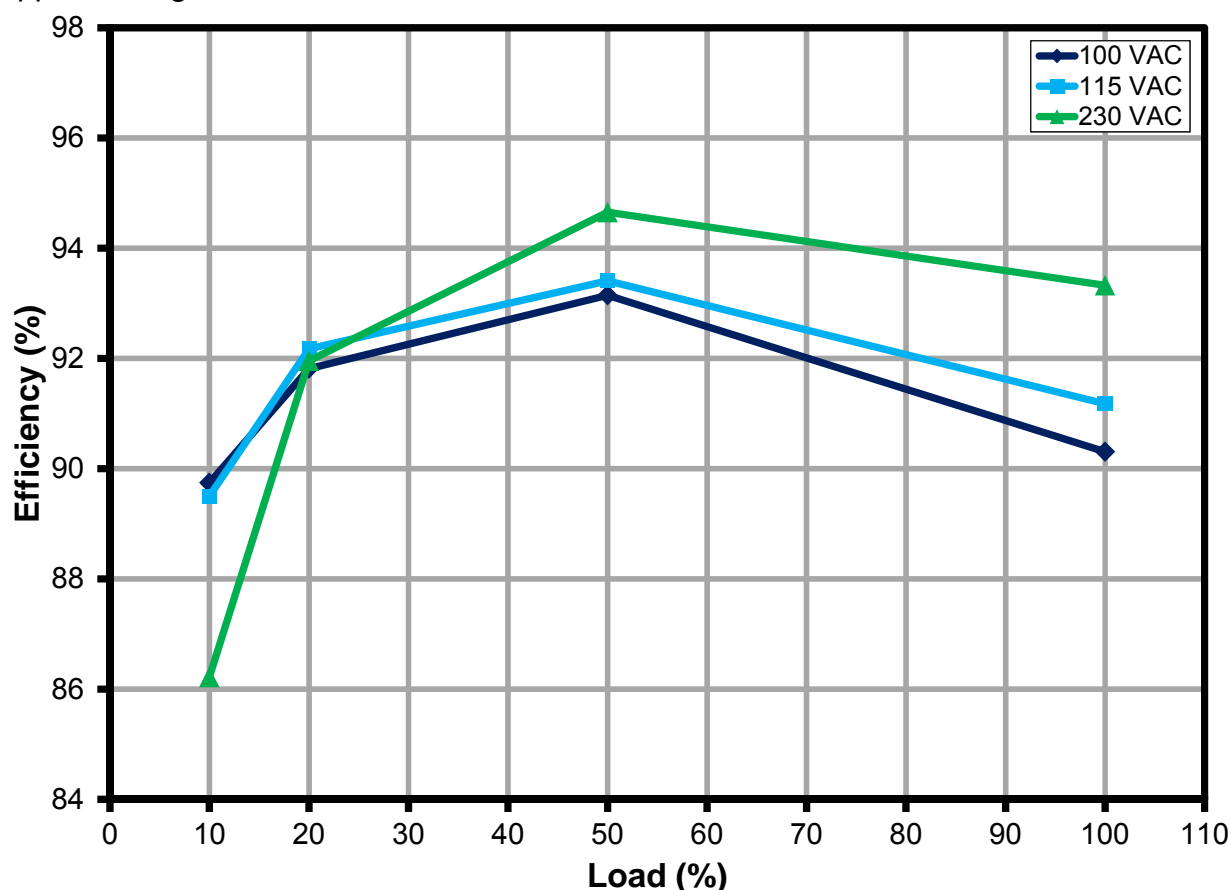


Figure 19 – System Efficiency vs. Load.

Note: Fan was running with full power and it was turned off for loads $\leq 50\%$.

Note: All the efficiency readings were taken by keeping the power supply inside a metal enclosure.

Note: Cable drop was not included in the efficiency measurements.

Power Supply is meeting 80 plus platinum efficiency requirements.

V _{IN} (VAC)	Load (%)	Measured Efficiency (%)	Platinum Efficiency Specification (%)
100 / 115 / 230	20	91.81 / 92.17 / 91.96	90 / 90 / 90
100 / 115 / 230	50	93.14 / 93.41 / 94.65	92 / 92 / 94
100 / 115 / 230	100	90.31 / 91.17 / 93.33	89 / 89 / 91



12.2 Power Factor

Power factor measurements were made using a sine wave AC source.

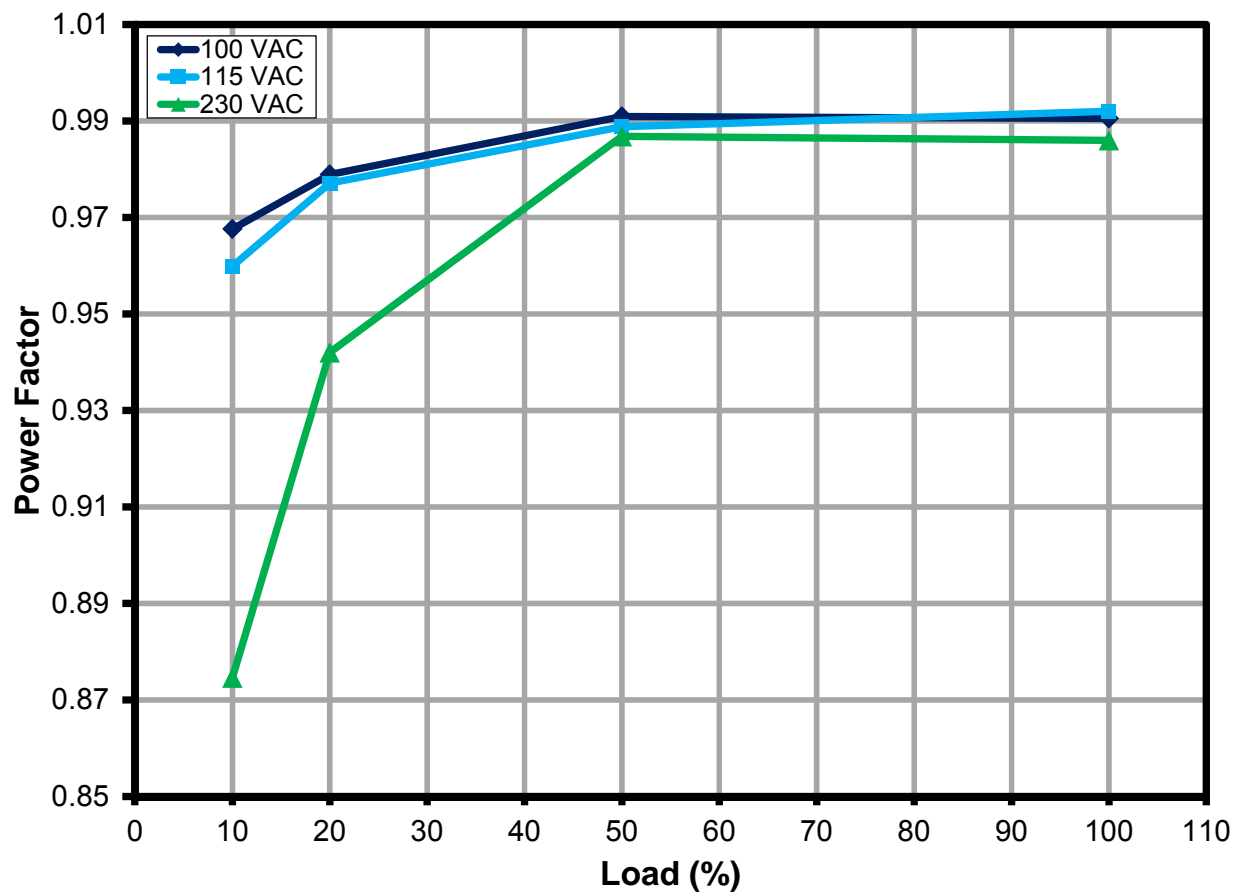


Figure 20 – Power Factor vs. Input Voltage, 50% and 100% Load.

12.3 THD

THD measurements were taken at 100%, 50% and 20% load using a sine wave source and a Yokogawa WT310 power analyzer with harmonic measurement option.

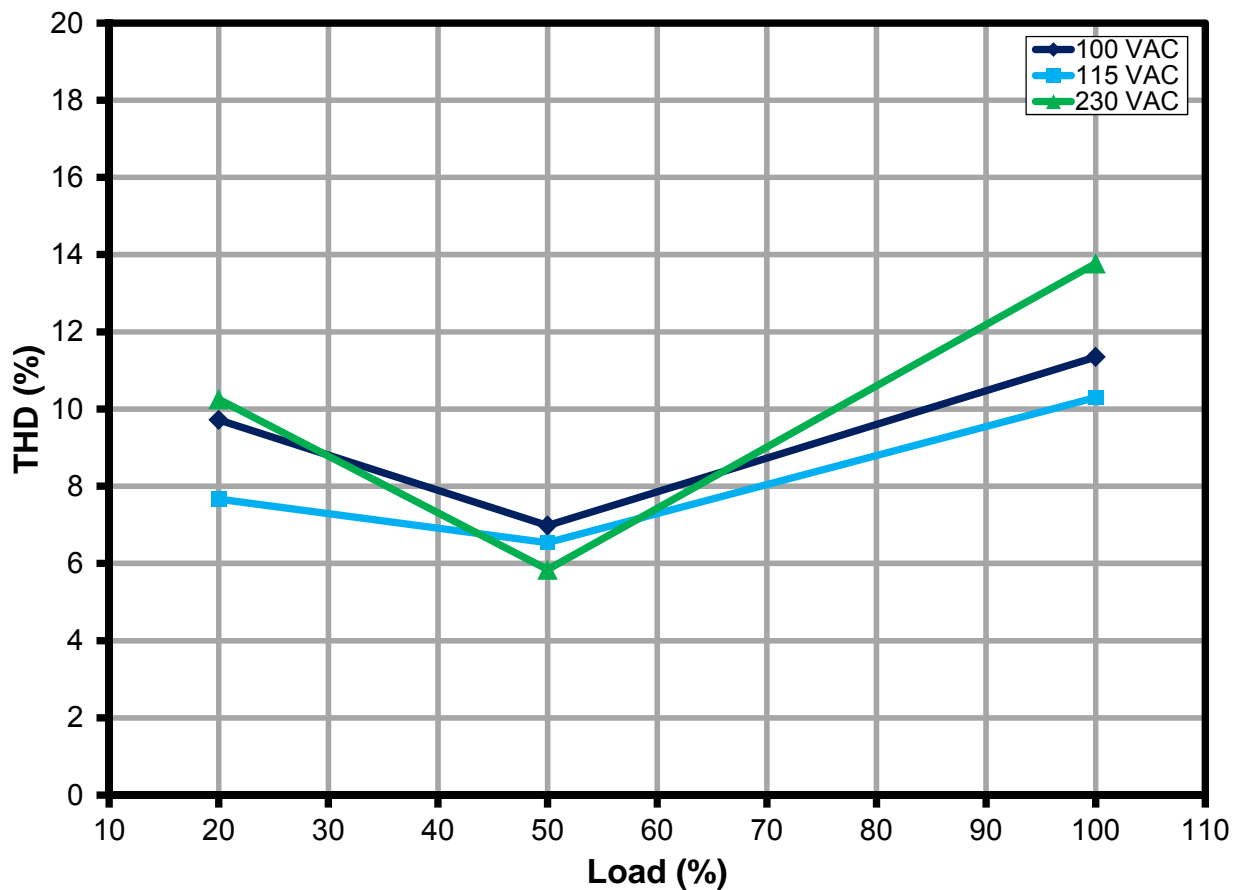


Figure 21 – THD vs. Load.



12.4 Output Regulation

The PFC regulates the LLC and standby supply input voltage under normal conditions so the outputs will not be affected by the AC input voltage. Variations due to temperature and component tolerances are not represented. The 12 V (+12 VA and +12 VB voltages after current sensing resistors) output varies by less than 1% over a line voltage range of 100 VAC to 230 VAC.

12.4.1 Line Regulation

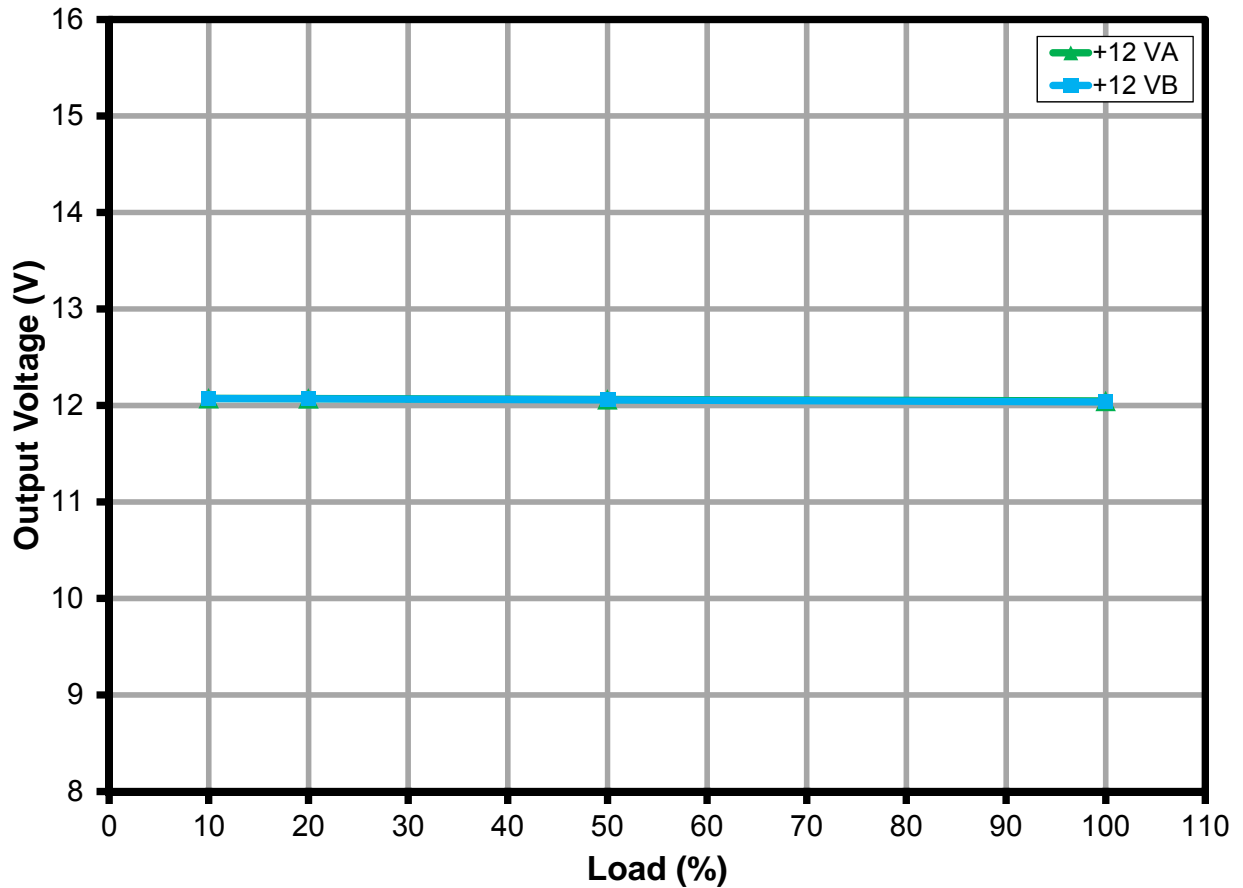


Figure 22 – Output Voltage vs. Input Line Voltage (Line Regulation).

12.4.2 Load Regulation

The 12 V output varies by less than 1% over a load range of 10% to 100% load.

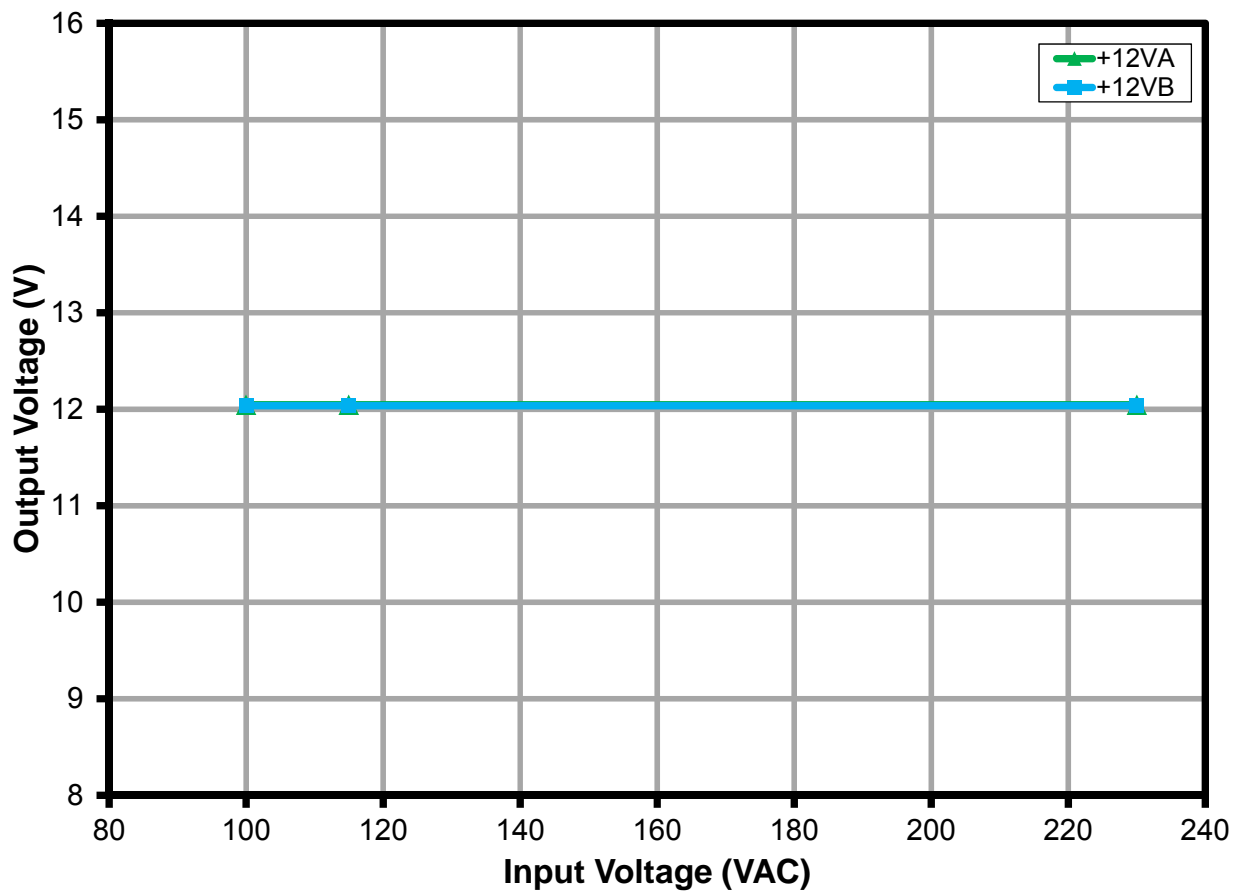


Figure 23 – Output Voltage vs. Output Load Current (Load Regulation).

13 Input Current Harmonics vs. EN 61000-3-2 Class D Limits

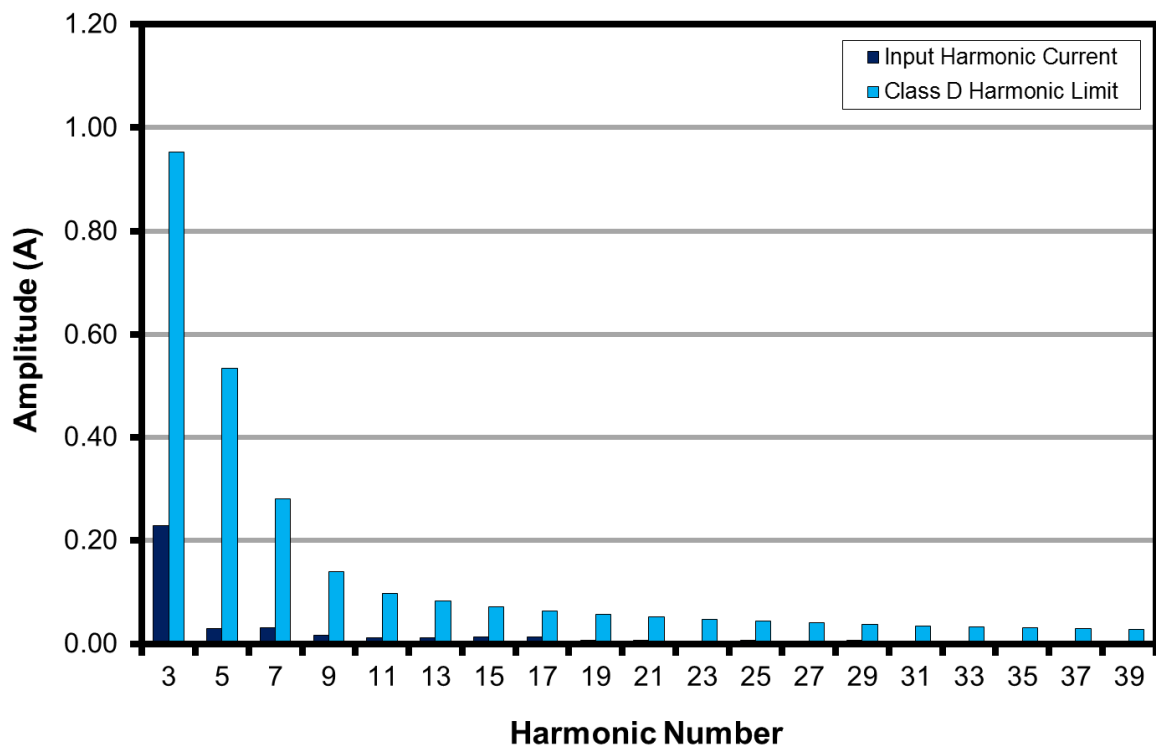


Figure 24 – AC Input Harmonics vs. EN 61000-3-2 Class D Limits, 115 VAC, 60 Hz, 100% Load.

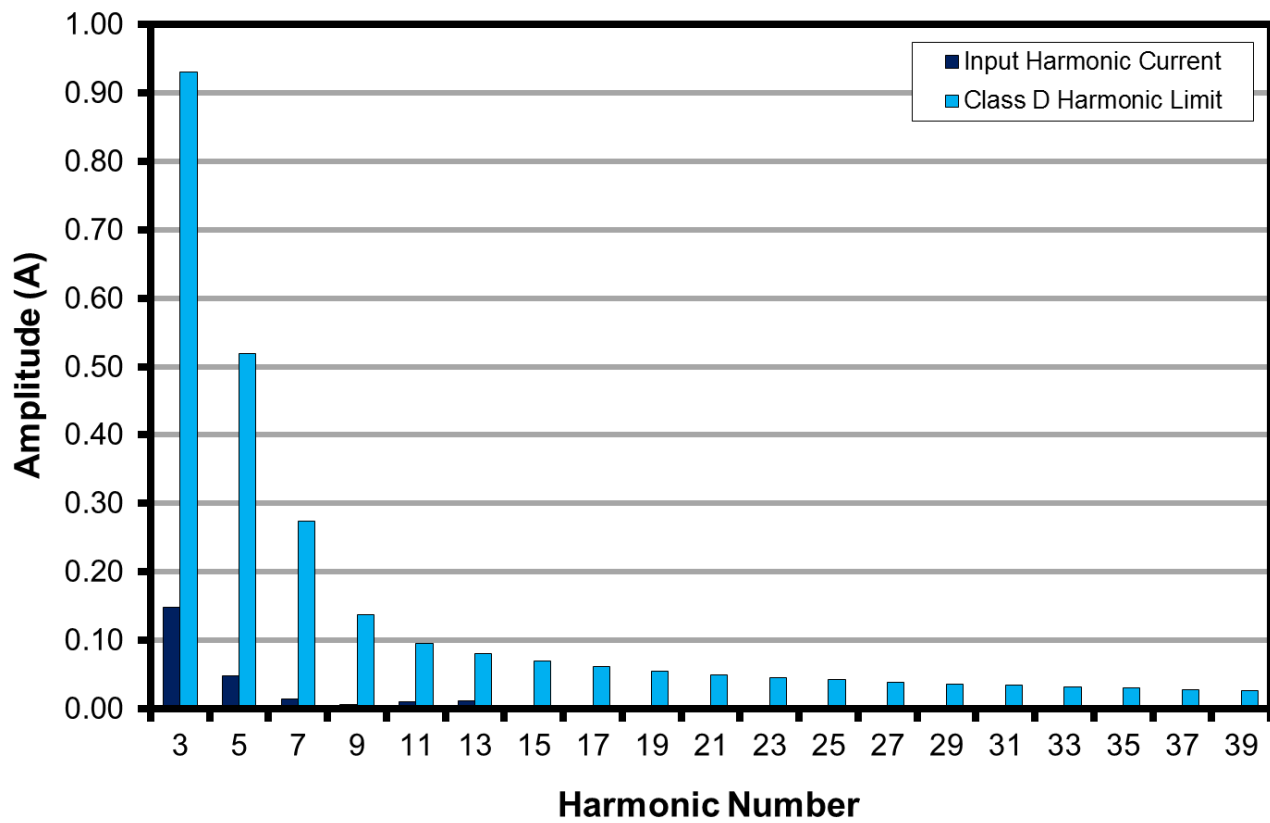


Figure 25 – AC Input Harmonics vs. EN 61000-3-2 Class D Limits, 230 VAC, 50 Hz, 100% Load.

14 Waveforms

14.1 Input Voltage and Current

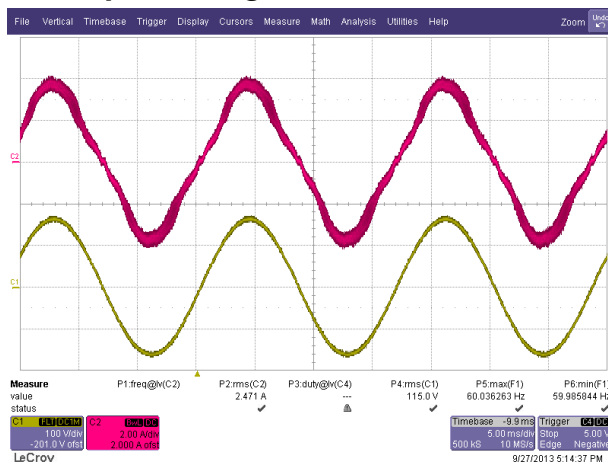


Figure 26 – 115 VAC, 255 W Load.
Upper: I_{IN} , 2 A / div.
Lower: V_{IN} , 100 V, 5 ms / div.

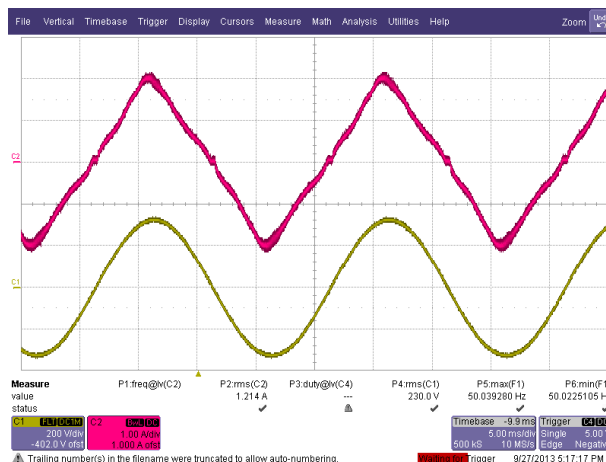


Figure 27 – 230 VAC, 255 W Load.
Upper: I_{IN} , 1 A / div.
Lower: V_{IN} , 200 V, 5 ms / div.

14.2 LLC Primary Voltage and Current

The LLC stage current was measured by adding a current sensing loop between C34 and B- that measures the LLC transformer (T1) primary current. The primary voltage waveform was measured at HB node.

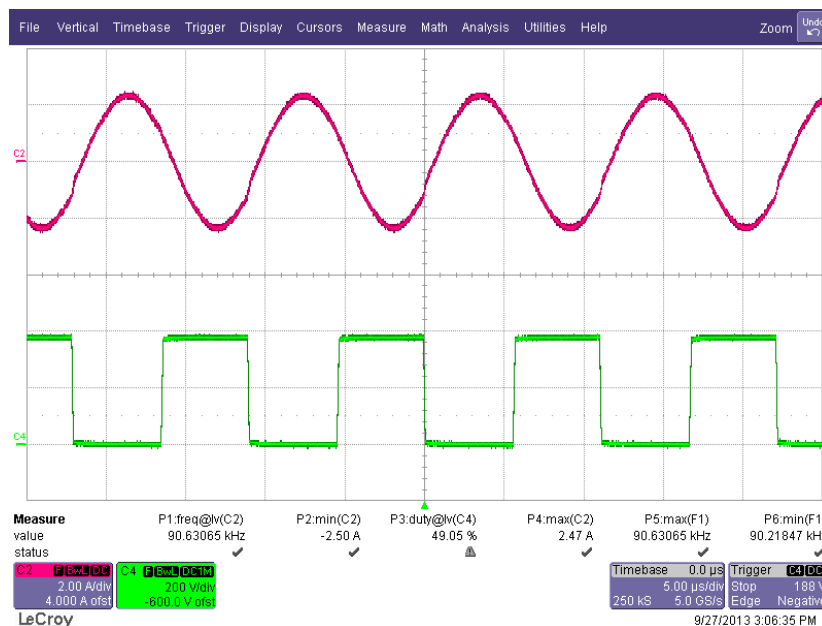


Figure 28 – LLC Stage Primary Voltage and Current.
Upper: Current, 2 A / div.
Lower: Voltage, 200 V, 5 μs / div.

14.3 PFC Switch Voltage and Current - Normal Operation

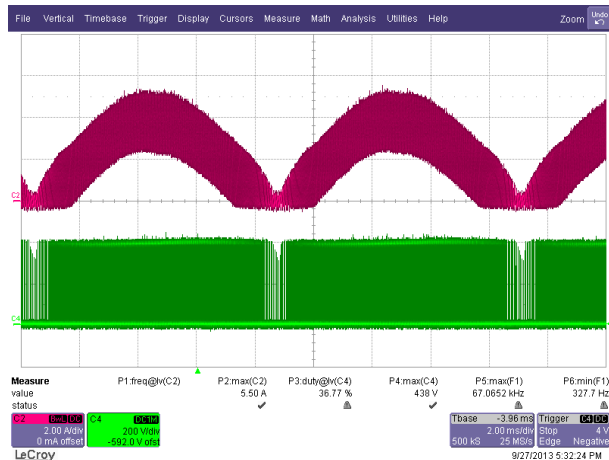


Figure 29 – PFC Stage Drain Voltage and Inductor Current, Full Load, 115 VAC
Upper: $I_{INDUCTOR}$, 2 A / div.
Lower: V_{DRAIN} , 200 V, 2 ms / div.

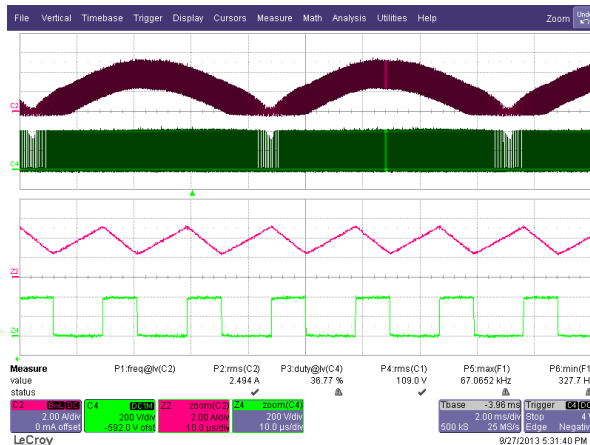


Figure 30 – PFC Stage Drain Voltage and Inductor Current, Full Load, 115 VAC.
Upper: $I_{INDUCTOR}$, 2 A / div.
Lower: V_{DRAIN} , 200 V, 10 μ s / div. (Zoom in on top of sine wave.)

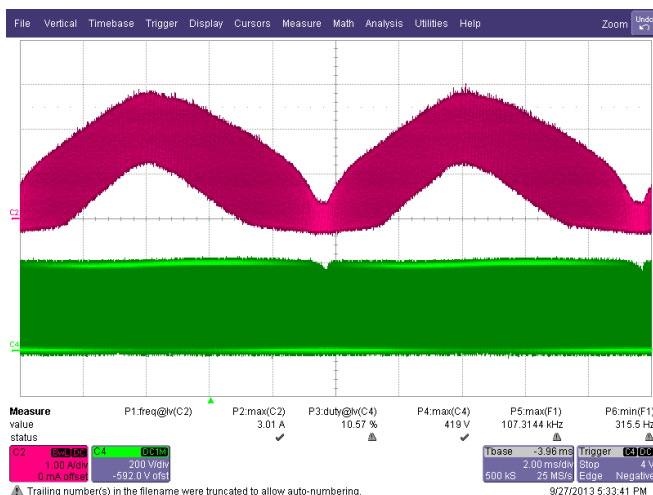


Figure 31 – PFC Stage Drain Voltage and Inductor Current, Full Load, 230 VAC.
Upper: $I_{INDUCTOR}$, 1 A / div.
Lower: V_{DRAIN} , 200 V, 2 ms / div.

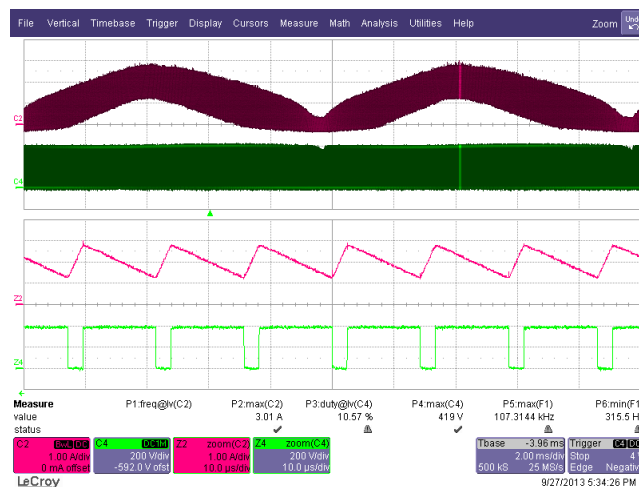


Figure 32 – PFC Stage Drain Voltage and Inductor Current, Full Load, 230 VAC.
Upper: $I_{INDUCTOR}$, 1 A / div.
Lower: V_{DRAIN} , 200 V, 10 μ s / div. (Zoom in on top of sine wave.)

14.4 AC Input Current and PFC Output Voltage During Start-up

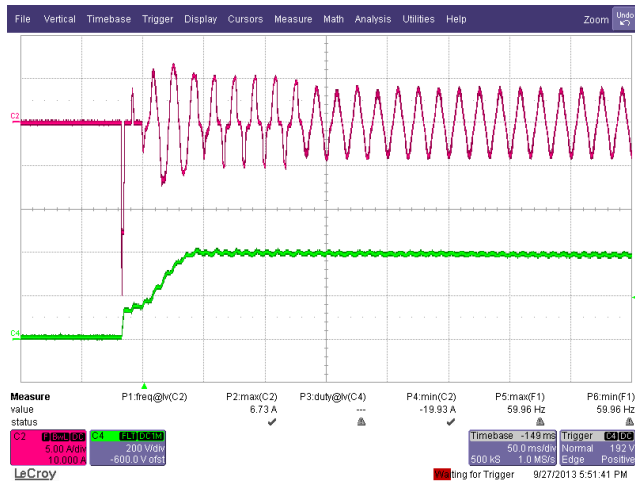


Figure 33 – AC Input Current vs. PFC Output Voltage at Start-up, Full Load, 115 VAC.

Upper: AC I_{IN} , 5 A / div.

Lower: PFC V_{OUT} , 200 V, 50 ms / div

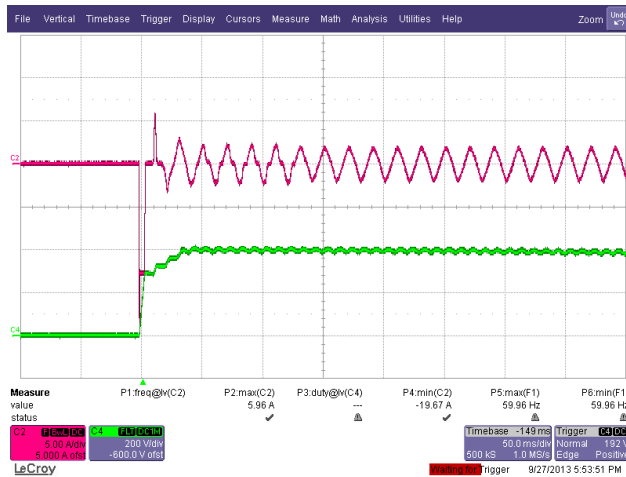


Figure 34 – AC Input Current vs. PFC Output Voltage at Start-up, Full Load, 230 VAC.

Upper: AC I_{IN} , 2 A / div.

Lower: PFC V_{OUT} , 200 V, 50 ms / div.

14.5 LLC Start-up (CR Mode)

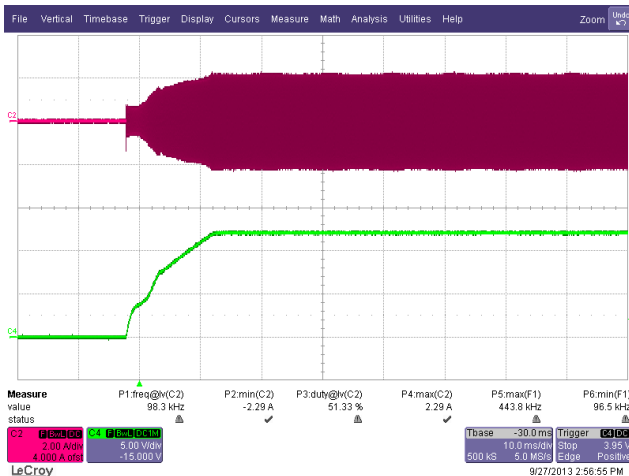


Figure 35 – LLC Start-up. 115 VAC, 100% Load.

Upper: LLC Primary Current, 2 A / div.

Lower: LLC V_{OUT} , 5 V, 10 ms / div.

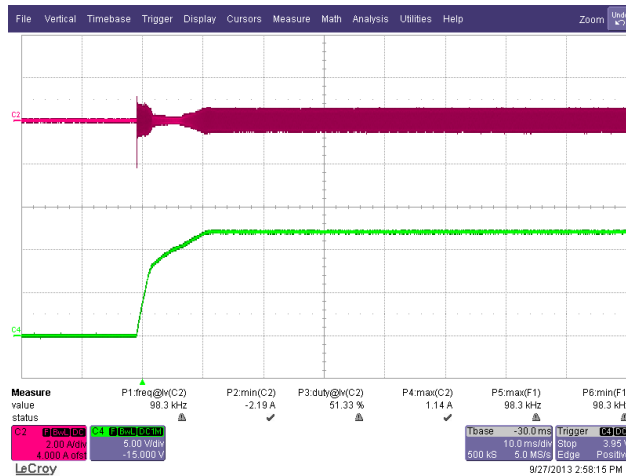


Figure 36 – LLC Start-up. 115 VAC, 0% Load.

Upper: LLC Primary Current, 2 A / div.

Lower: LLC V_{OUT} , 5 V, 10 ms / div.

14.6 LLC Brown-Out

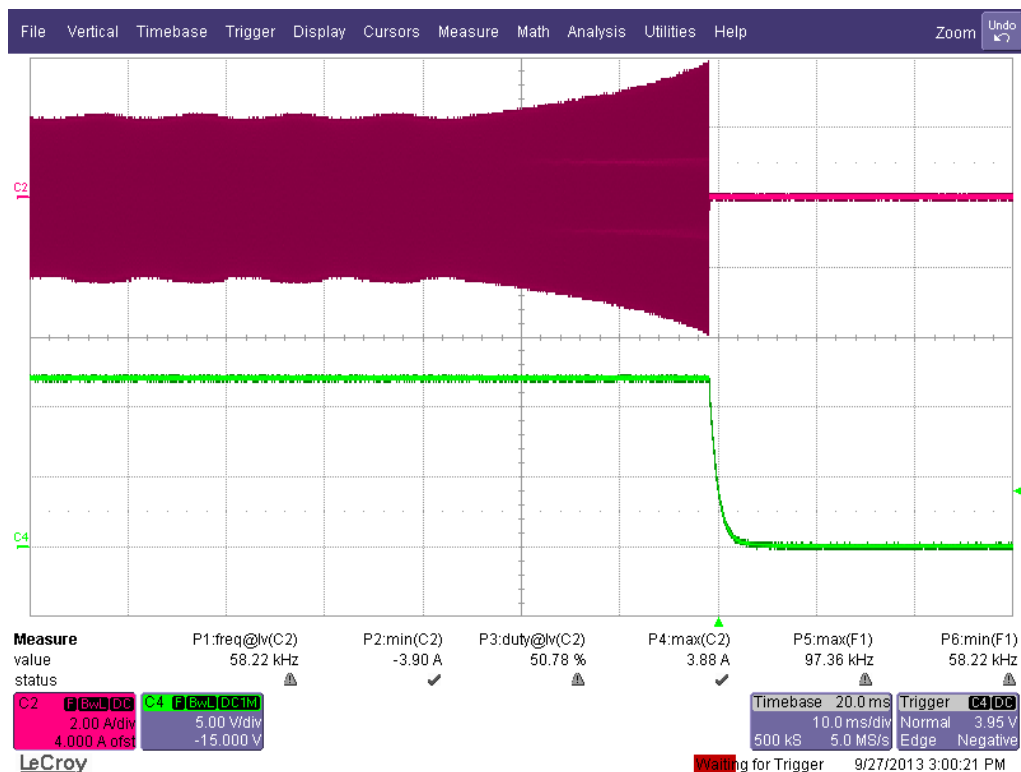


Figure 37 – LLC Brown-out.

Upper: Primary Current, 2 A / div.

Lower: Main V_{OUT}, 5 V / div.



14.7 LLC Output Short-Circuit

The figure below shows the effect of an output short circuit on the LLC primary current. A mercury displacement relay was used to short the output to get a fast, bounce-free connection.

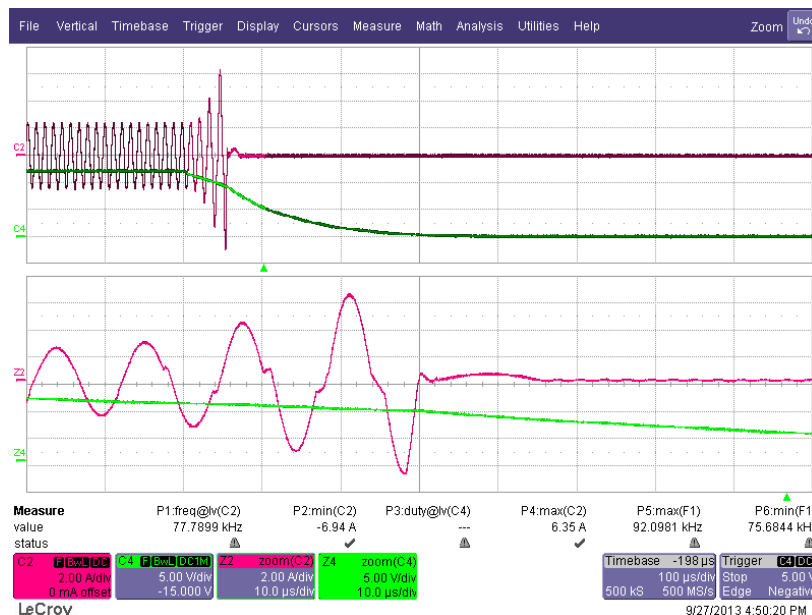


Figure 38 – Output Short Circuit Test.
Upper: LLC Primary Current, 2 A / div.
Lower: Main V_{OUT}, 5 V, 100 μs / div.

14.8 Main and Standby Start-up (CR Mode)

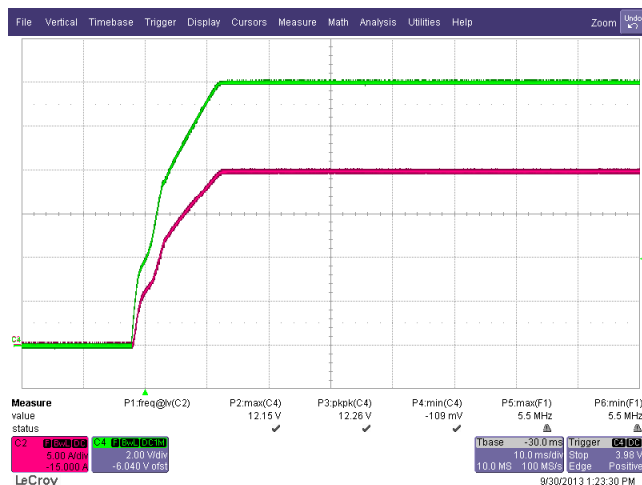


Figure 39 – LLC Start-up. 115 VAC, 100% Load.
Upper: LLC V_{OUT}, 2 V / div,
Lower: LLC I_{OUT}, 5 A / div. 10 ms / div.

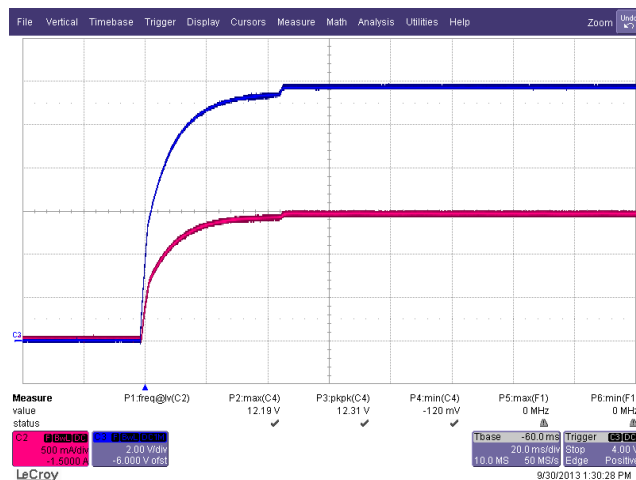


Figure 40 – LLC Start-up. 115 VAC, 0% Load.
Upper: Standby V_{OUT}, 2 V / div.
Lower: Standby I_{OUT}, 0.5 A / div, 10 ms / div.

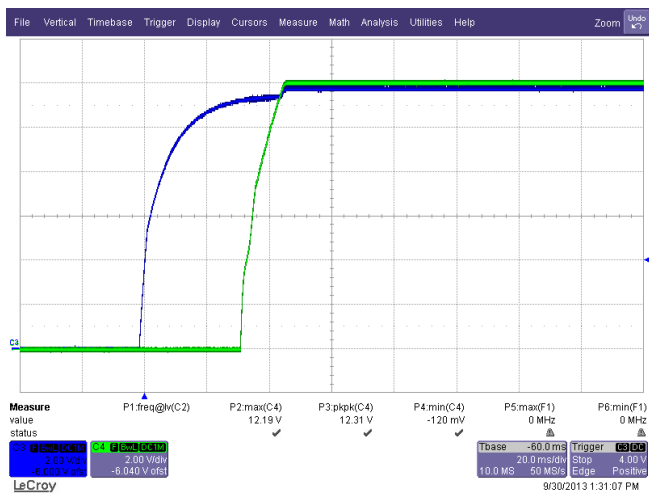


Figure 41 – LLC Start-up. 115 VAC, 100% Load.
Upper: LLC V_{OUT} , 2 V / div.
Lower: Standby V_{OUT} , 2 V, 20 ms / div.

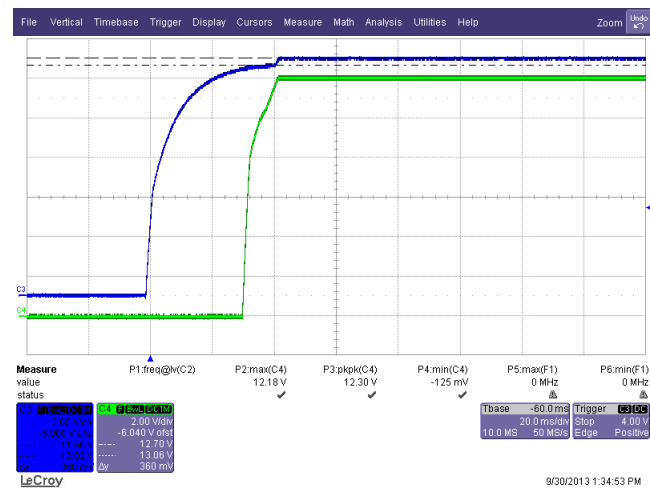


Figure 42 – LLC Start-up. 115 VAC, 0% Load.
Upper: Standby V_{OUT} , 2 V / div.
Lower: LLC V_{OUT} , 2 V, 20 ms / div.

14.9 Synchronous FET Drain and Gate Voltages

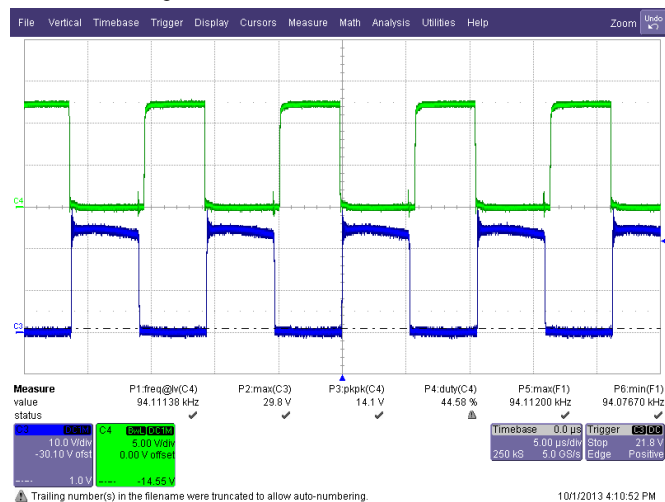


Figure 43 – LLC Sync Rect. Q1, 100% Load.
Upper: SR Gate Drive, 5 V / div.
Lower: SR V_{DRAIN} , 10 V, 10 ms / div.

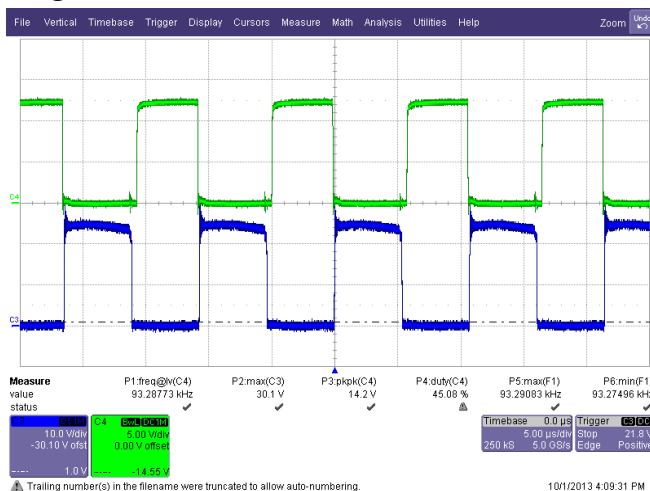


Figure 44 – LLC Sync Rect. Q2, 100% Load.
Upper: SR Gate Drive, 5 V / div.
Lower: SR V_{DRAIN} , 10 V, 10 ms / div.



14.10 Output Ripple Measurements

14.10.1 Ripple Measurement Technique

For DC output ripple measurements, use a modified oscilloscope test probe to reduce spurious signals. Details of the probe modification are provided in figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 μF / 50 V ceramic capacitor and 1.0 μF / 100 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

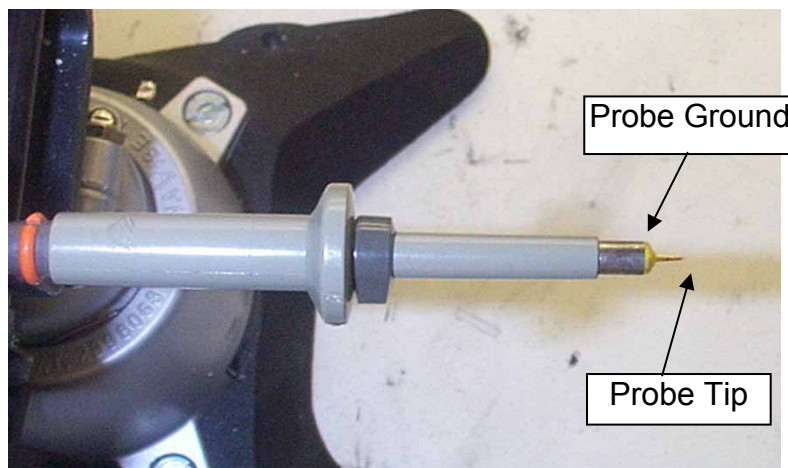


Figure 45 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

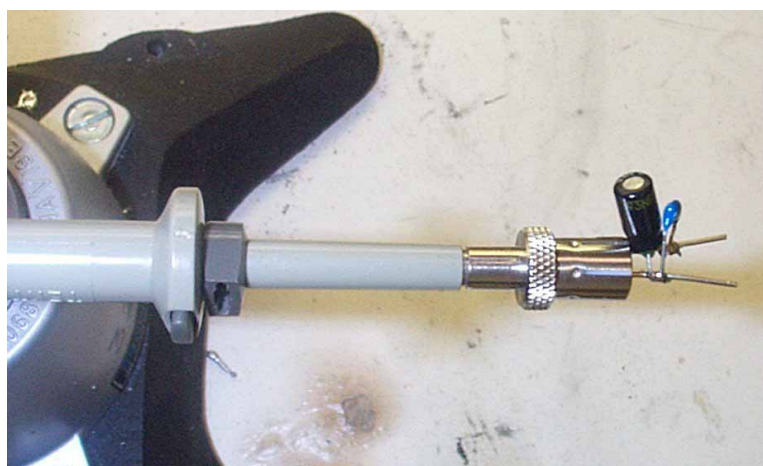


Figure 46 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

14.10.2 Full Load Output Ripple Results

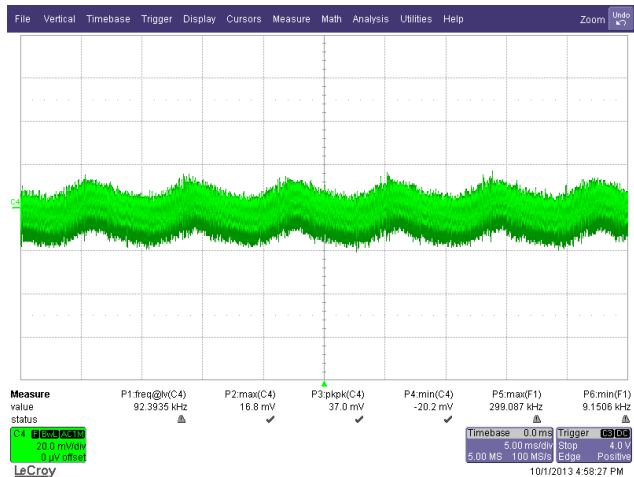


Figure 47 – 12 V Output Ripple, 20 mV, 5 ms / div.

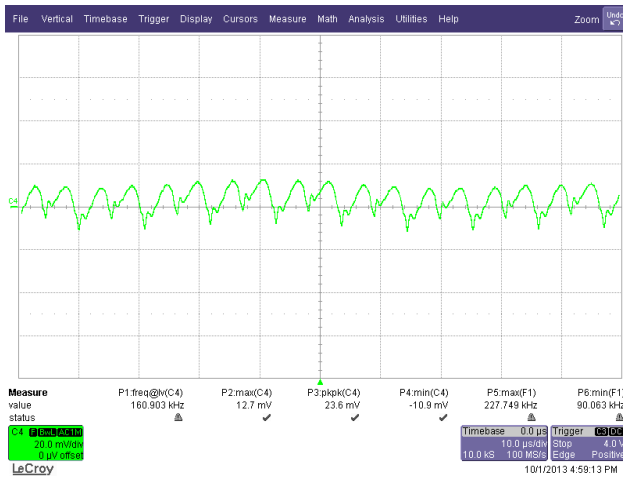


Figure 48 – 12 V Output Ripple, 20 mV, 10 μs / div.

14.10.3 No-Load Ripple Results

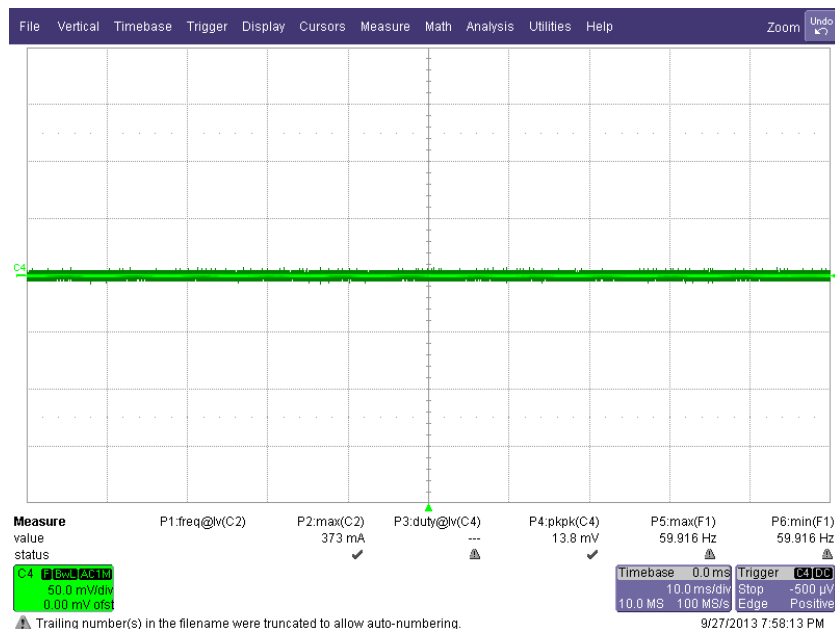


Figure 49 – 12 V No-Load Output Ripple, 50 mV, 10 ms / div.

14.11 Main Output Load Step Response

The figures below show transient response with a 10%-100%-10%, 50%-100%-50%, 75%-100%-75% and 0%-100%-0% load steps for the 12 V output. The oscilloscope was triggered using the rising edge of the load step, and averaging was used to cancel out ripple components asynchronous to the load step in order to better ascertain the load step response.

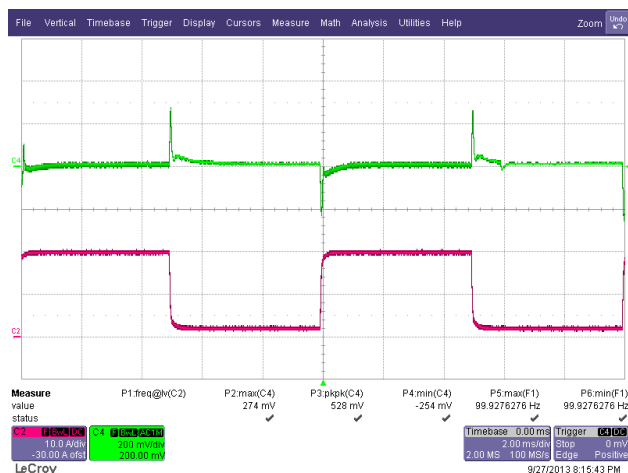


Figure 50 – Output Transient Response 10%-100%-10%, 2 ms / div.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{LOAD} , 10 A / div.

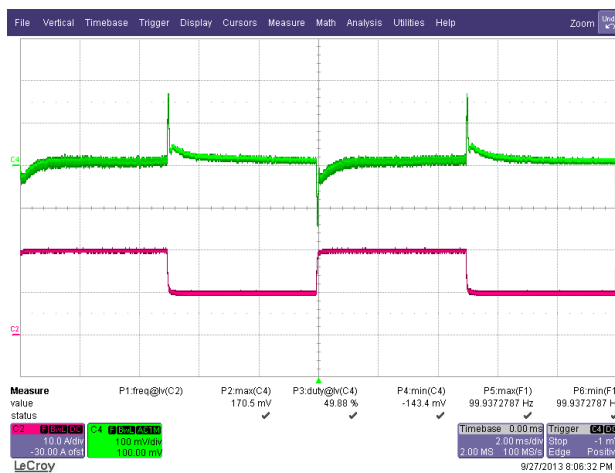


Figure 51 – Output Transient Response 50%-100%-50%, 2 ms / div.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{LOAD} , 10 A / div.

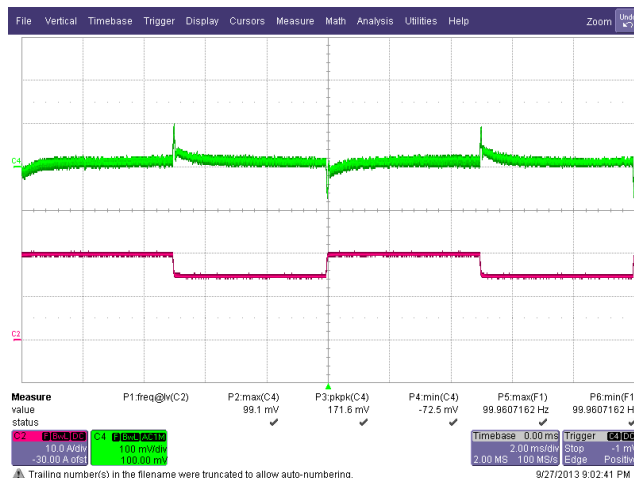


Figure 52 – Output Transient Response 75%-100%-75%, 2 ms / div.
Upper: V_{OUT} , 100 mV / div.
Lower: I_{LOAD} , 10 A / div.

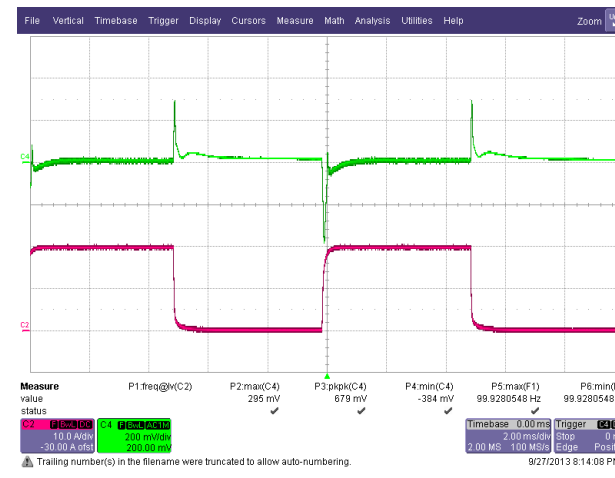


Figure 53 – Output Transient Response 0%-100%-0%, 2 ms / div.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{LOAD} , 10 A / div.

14.12 Standby Output Load Step Response

The figures below show transient response with a 10%-100%-10%, 50%-100%-50%, 75%-100%-75% and 0%-100%-0% load steps for the 12 V output. The oscilloscope was triggered using the rising edge of the load step, and averaging was used to cancel out ripple components asynchronous to the load step in order to better ascertain the load step response.



Figure 54 – Output Transient Response 10%-100%-10%, 5 ms / div.
Upper: V_{OUT} , 100 mV / div.
Lower: I_{LOAD} , 1 A / div.

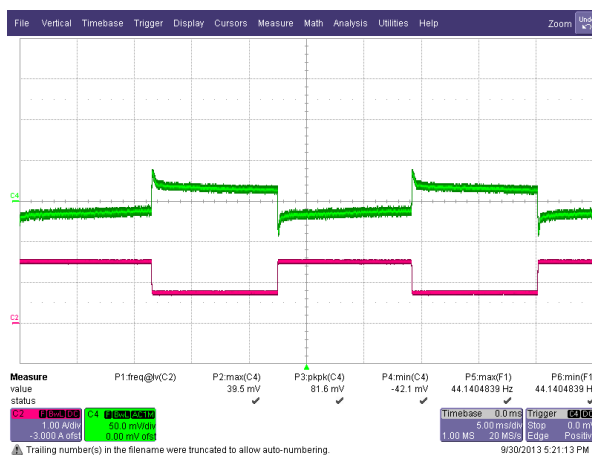


Figure 55 – Output Transient Response 50%-100%-50%, 5 ms / div.
Upper: V_{OUT} , 50 mV / div.
Lower: I_{LOAD} , 1 A / div.



Figure 56 – Output Transient Response 75%-100%-75%, 5 ms / div.
Upper: V_{OUT} , 20 mV / div.
Lower: I_{LOAD} , 1 A / div.



Figure 57 – Output Transient Response 0%-100%-0%, 5 ms / div.
Upper: V_{OUT} , 200 mV / div.
Lower: I_{LOAD} , 1 A / div.

15 Conducted EMI

15.1 EMI Set-up

15.1.1 Power Supply Preparation for EMI Test

The picture below shows the power supply set-up for EMI and surge testing. The power supply is enclosed in a metallic enclosure.



Figure 58 – DER-385 Set-up for EMI and Surge Testing.

15.1.2 EMI Test Set-up



Figure 59 – EMI Room Set-up.



15.2 EMI Scans

Conducted EMI tests were performed with a resistive load on the 12 V main and standby outputs. The secondary ground of the unit was connected to the metallic enclosure with the help of a screw, which in turn was hard wired to the AC cord ground. The resistive load was left floating.

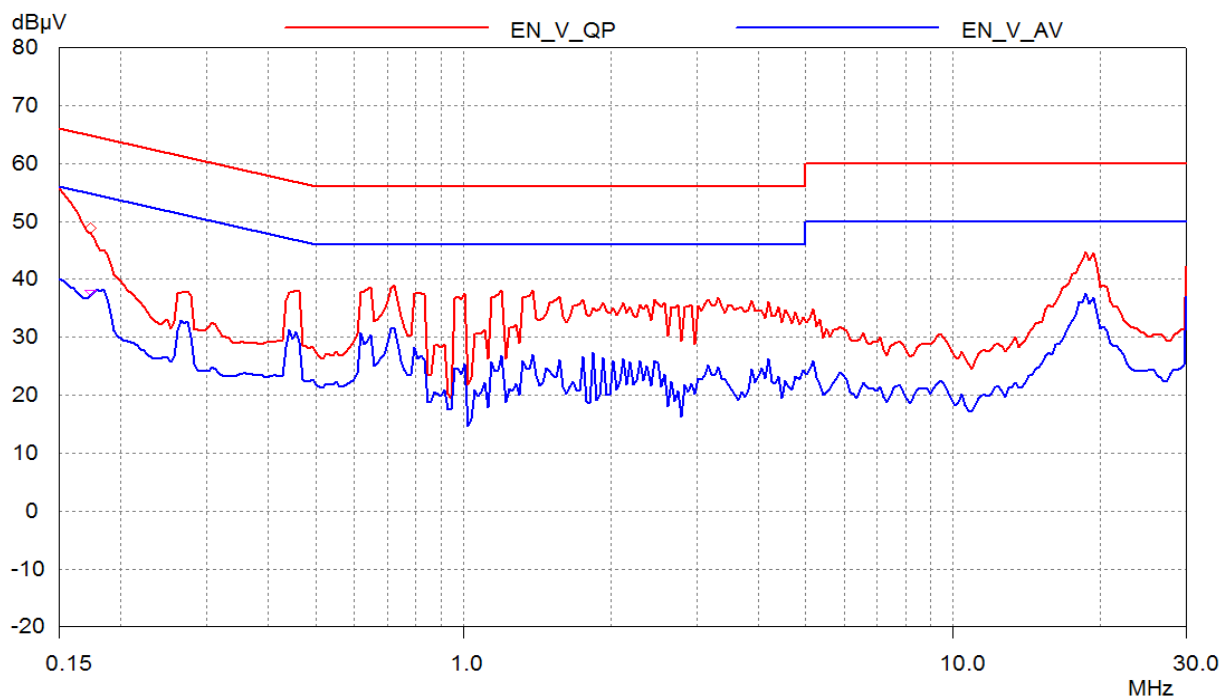


Figure 60 – Conducted EMI, 115 VAC.

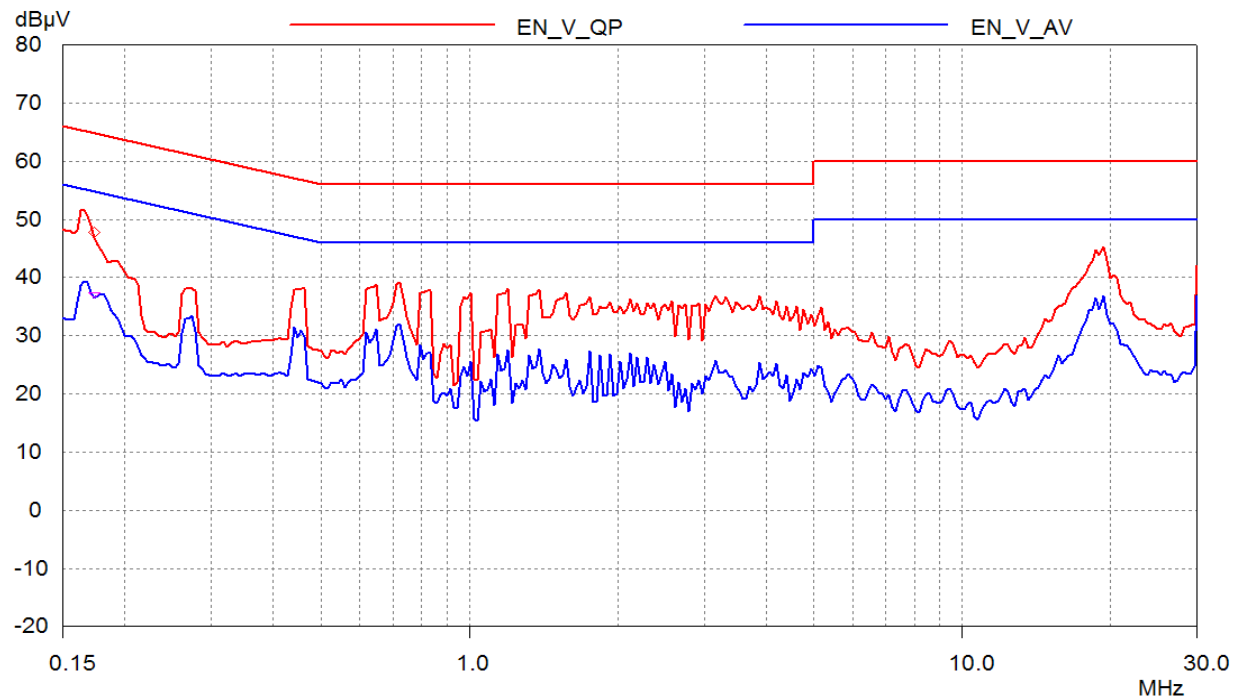


Figure 61 – Conducted EMI, 230 VAC.



16 Gain-Phase Measurement

Gain-phase measurements were carried out on DER-385 at 20%, 50% and 100% loads.

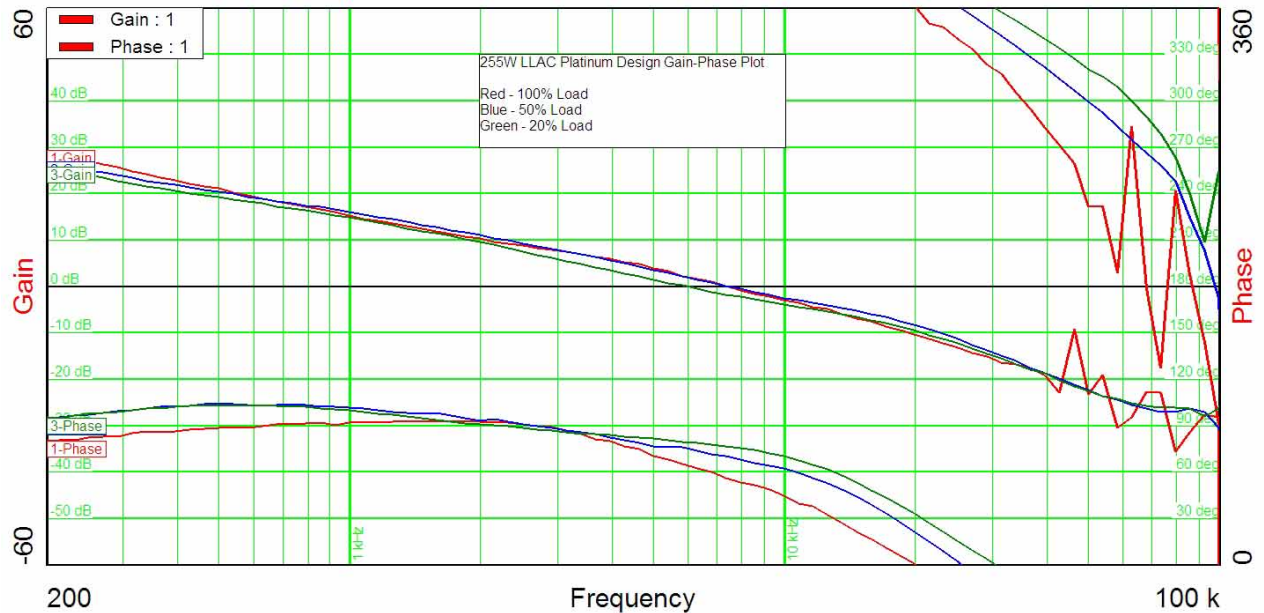


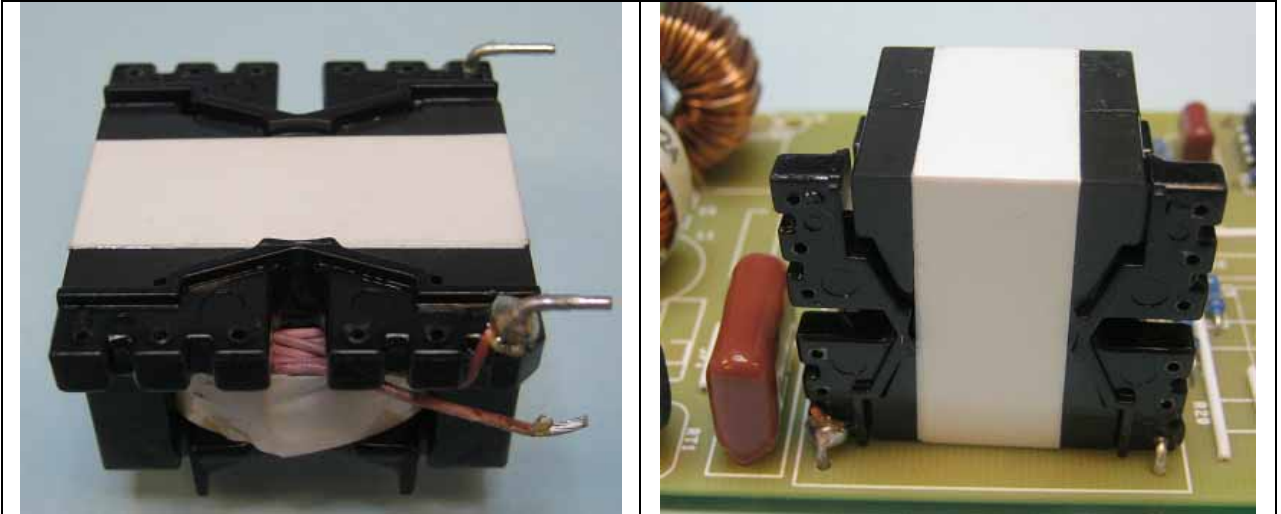
Figure 83 – DER-385 LLC Gain-Phase Measurement, Full Load Gain Crossover Frequency – ~7.5 kHz, Phase Margin, ~57°.

17 Appendix

17.1 Relay Cable Preparation



17.2 PFC Inductor Assembly



18 Revision History

Date	Author	Revision	Description and Changes	Reviewed
22-Jan-14	SS	2.1	Initial Release	Apps & Mktg



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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS

5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

GERMANY

Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@powerint.com

JAPAN

Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

TAIWAN

5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

CHINA (SHANGHAI)

Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@powerint.com

INDIA

#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@powerint.com

KOREA

RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

EUROPE HQ

1st Floor, St. James's House
East Street, Farnham
Surrey GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

CHINA (SHENZHEN)

3rd Floor, Block A,
Zhongtuo International Business
Center, No. 1061, Xiang Mei Rd,
FuTian District, ShenZhen,
China, 518040
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

ITALY

Via Milanese 20, 3rd Fl.
20099 Sesto San Giovanni
(MI) Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

SINGAPORE

51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

APPLICATIONS HOTLINE

World Wide +1-408-414-9660

APPLICATIONS FAX

World Wide +1-408-414-9760

