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TECHNICAL ARTICLE

DESIGNING SECOND STAGE OUTPUT FILTERS FOR SWITCHING POWER SUPPLIES

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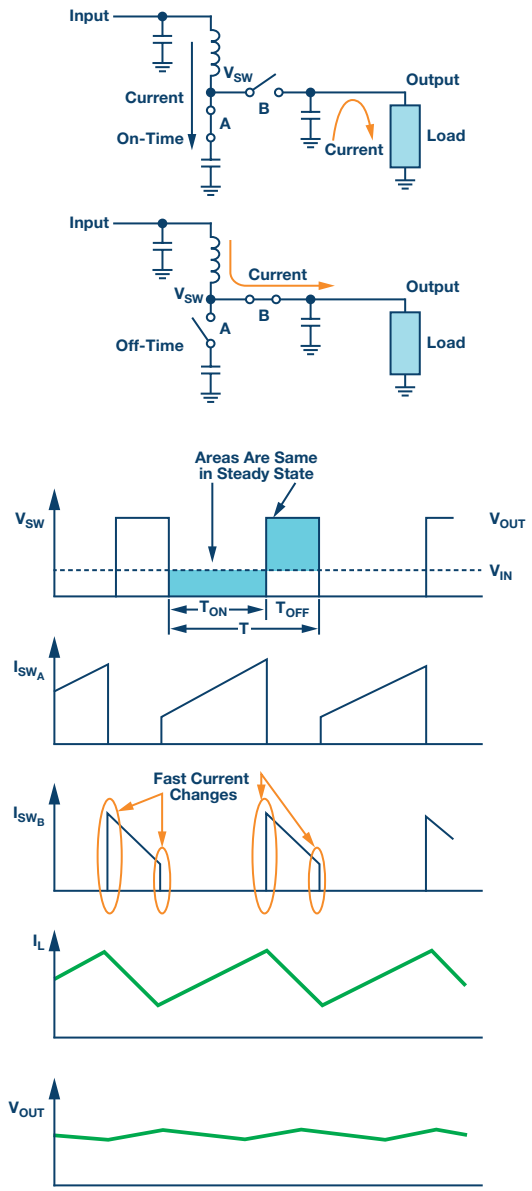

Figure 1. Basic voltage and current waveforms for a boost converter.

These days switching power supplies are nearly ubiquitous and used throughout every electronic device. They are valued for their small size, low cost, and efficiency. However, they have the major drawback in that their outputs can be noisy due to the high switching transients. This has kept them out of high performance analog circuits where linear regulators have ruled the roost. It has been shown that in many applications an appropriately filtered switching converter can replace a linear regulator for production of a low noise supply. Even in those demanding applications where an extremely low noise supply is required, there is probably a switching circuit somewhere upstream in the power tree. Therefore, there is a need to be able to design optimized, damped multistage filters to clean up the output from switching power converters. In addition, it is important to realize how the filter design will affect the compensation of the switching power converter.

In this article, boost circuits will be used for the example circuits, but the results will be directly applicable to any dc-to-dc converter. Shown in Figure 1 are the basic waveforms in a boost converter in constant-current mode (CCM).

The issue that makes an output filter so important for a boost or any of the other topologies with discontinuous current mode is the fast rise and fall in the current time in Switch B. This tends to excite parasitic inductances in the switch, the layout, and the output capacitors. The result is that in the real world the output waveforms look much more like Figure 2 rather than Figure 1, even with a good layout and ceramic output capacitors.

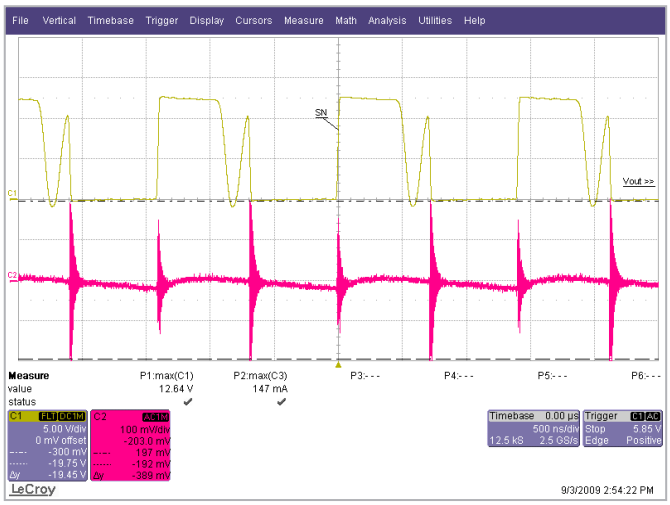

Figure 2. Typical measured waveforms of a boost converter in DCM.

The switching ripple (at the switching frequency) caused by the change in charge of the capacitor is very small compared to the undampened ringing of the output switch, which we will refer to as output noise. Generally, this output noise is in the 10 MHz to 100+ MHz range, well beyond the self-resonant frequency of most ceramic output capacitors. Therefore adding additional capacitors will do little to attenuate the noise.

There are a couple of reasonable choices for different types of filters to filter this output. This article will illustrate each type of filter and give a step-by-step process to a design. The equations are not rigorous and some reasonable assumptions are made to simplify them somewhat. There is still some iteration required since each component will affect the values of the others. The ADIsimPower design tools get around this problem by using linearized equations for component values, like cost or size, to do an optimization before actual components are selected, and then optimize the outputs once real components are chosen from the database of thousands of parts. However, for a first pass at a design, this level of complexity is not necessary. With the provided calculations and possibly using a SIMPLIS simulator like the free ADIsimPE,™ or some bench time in the lab, a satisfactory design can be found with a minimal amount of effort.

Before designing the filter, consider what is achievable with a single stage filter RC or LC filter. Typically with a second stage filter it is reasonable to get the ripple down to a few hundred µV p-p and the switching noise down below 1 mV p-p. A buck converter can be made somewhat quieter since the power inductor provides significant filtering. These limitations are because once the ripple is down in the µV the component parasitics, and noise coupling between filter stages starts to become the limiting factors. If even quieter supplies are required, then a third stage filter can be added. However, switching power supplies do not generally have the quietest references and also suffer from jitter noise. These both result in low frequency noise (1 Hz to 100 kHz) that cannot be easily filtered out. Therefore, for extremely low noise supplies it may be better to use a single second stage filter and then add an LDO to the output.

Before diving into a more detailed design process for each type of filter, some values that will get used in the design process for each of the types of filters are defined as follows:

ΔI_{PP}: The approximate peak-to-peak current coming into the output filter. For the calculations we assume that this is sinusoidal. The value will depend on the topology. For a buck it is the peak-to-peak current in the inductor. For a boost converter it is the peak current in Switch B (often a diode).

ΔV_{OUT}^{RIP}: The approximate out voltage ripple at the switching frequency of the converter.

R_{ESR}: The ESR of the chosen output capacitor.

F_{SW}: The switching frequency of the converter.

C_{RIP}: The output capacitor calculated assuming all of ΔI_{PP} rip flows into it.

ΔV_{OUT}^{TRAN}: The change in V_{OUT} when I_{STEP} applied to the output.

I_{STEP}: An instantaneous change of the output load.

T_{STEP}: The approximate response time of the converter to an instantaneous change in the output load.

F_u: The crossover frequency of the converter. For a buck it is generally $F_{SW}/10$. For a boost or buck boost type converter it is generally about a third of the location of the right half plane zero (RHPZ).

The simplest type of filter is just an RC filter as shown attached to the output of a low current ADP161x-based boost design shown in Figure 3. This filter has the advantage of low cost and will not need to be damped. However, due to power dissipation it is only useful for very low output current converters. For this article, ceramic capacitors with small ESR are assumed.

Design Process for an RC Second Stage Output Filter

Step 1: Choose C_1 based on assuming the value output ripple at C_1 is approximately ignoring the rest of the filter; 5 mV p-p to 20 mV p-p is a good place to start. C_1 can then be calculated using Equation 1.

$$C_1 = \frac{I_{PP}}{8F_{SW}\Delta V_{OUT}^{RIP} - \Delta I_{PP}R_{ESR}} \quad (1)$$

Step 2: R can be chosen based on power dissipation. R must be much larger than R_{ESR} for the capacitors and for this filter to be effective. This limits the range of output currents to something less that 50 mA or so.

Step 3: C_2 can then be calculated from Equation 2 through Equation 6. A, a, b, and c are just intermediate values to simplify calculation and have no physical meaning. These equations assumes $R << R_{LOAD}$ and the ESR for each capacitor is small. These are both very good assumptions and introduce little error. C_2 should be the same or larger than C_1. The ripple in Step 1 can be adjusted to make this possible.

$$A = \frac{\Delta V_{OUT}^{RIP}}{\Delta I_{PP}R_{LOAD}} \quad (2)$$

$$a = AR^2R_{LOAD}^2C_1^2\omega^4 + AR_{LOAD}^2\omega^2 \quad (3)$$

$$b = 2AR_{LOAD}^2\omega^2C_1 - 2AR_{LOAD}C_1\omega^2 \quad (4)$$

$$c = AR_{LOAD}\omega^2C_1 + A - 1 \quad (5)$$

$$C_2 = \frac{-b + \sqrt{b2 - 4ac}}{2a} \quad (6)$$

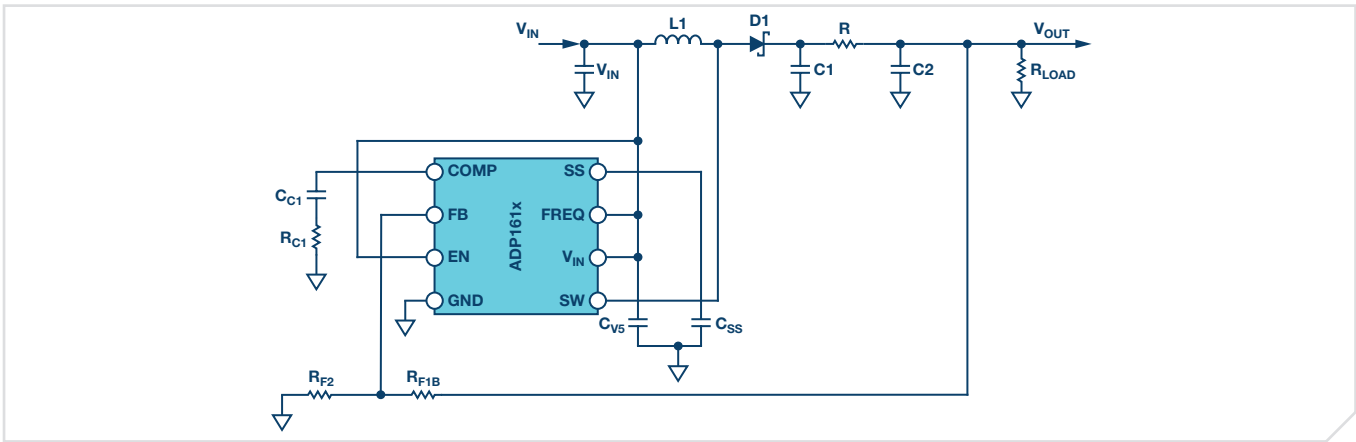

Figure 3. ADP161x low output current boost converter design with an added RC filter on the output.

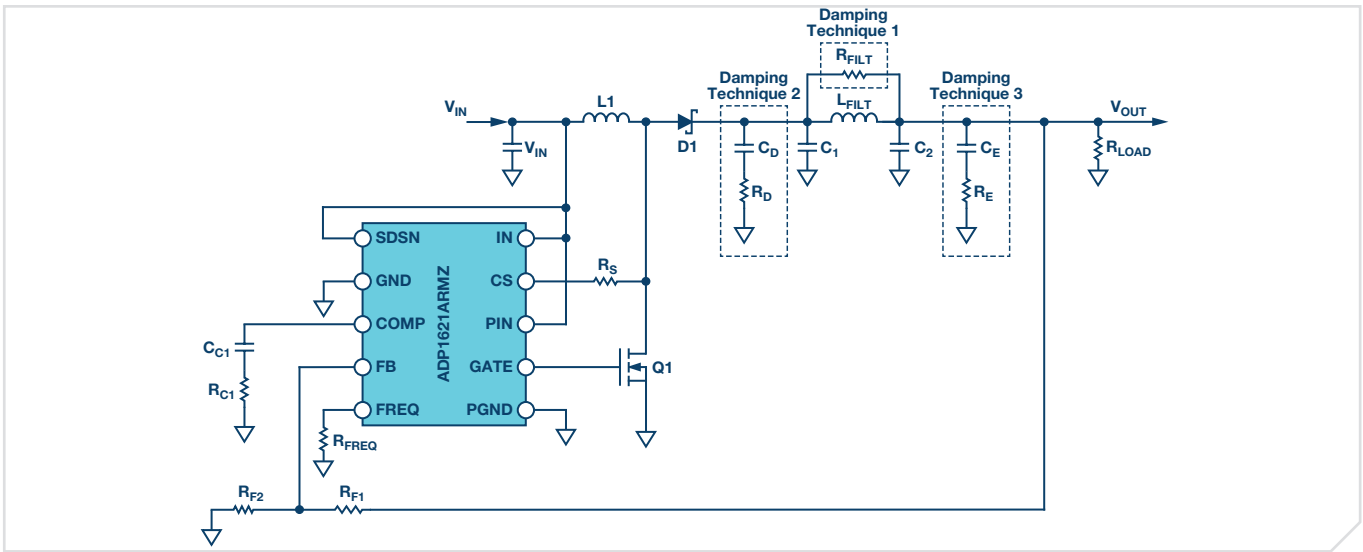

Figure 4. ADP1621 with an output filter with several different damping techniques highlighted.

For higher current supplies it is beneficial to replace the resistor in the pi filter with an inductor as shown in Figure 4. This configuration gives very good ripple and switching noise rejection in addition to low power loss. The issue is that we have now introduced an additional tank circuit that can resonate. This can result in oscillations and an unstable power supply. Therefore, the first step to designing this filter is to choose how to damp the filter. Figure 4 shows three viable damping techniques. Adding R_{FILT} has the advantage of adding little extra expense or size. The damping resistor typically has little to no loss and can be small for even large power supplies. The drawback is that it significantly reduces the effectiveness of the filter by reducing the parallel impedance with the inductor. Technique 2 has the advantage of maximizing filter performance. If an all ceramic design is desired, R_D can be a discrete resistor in series with a ceramic capacitor. Otherwise a physically large capacitor with a high ESR is required. This additional capacitance (C_D) can add significant cost and size to the design. Damping Technique 3 looks very advantageous since the dampening capacitor C_E is added to the output where it might help somewhat with transient response and output ripple. However, this is the most expensive technique since the amount of capacitance required is much larger. In addition, the relatively large amount of capacitance on the output will lower the frequency of the filter resonance, which will reduce the achievable bandwidth of the converter—therefore Technique 3 is not recommended. For the ADIsimPower design tools we use Technique 1 because of the low cost and relative ease of implementing it in an automated design process.

Another issue that needs to be dealt with is compensation. It may be counterintuitive, but it is almost always better to put the filter inside the feedback loop. This is because putting it in the feedback loop helps damp the filter somewhat, eliminates dc load shift and the series resistance of the filter, and gives a better transient response with less ringing. Figure 5 shows the Bode plot for a boost converter with an LC filter output added to the output.

The feedback is taken before or after the filter inductor. The thing that is most surprising to people is how much the open-loop Bode plot changes even when the filter is not "in" the feedback loop. Since the control loop is affected with or without the filter in the feedback loop, one might as well compensate for it appropriately. In general this will mean scaling back the target crossover frequency to a maximum of a fifth to a tenth of the filter resonant frequency (F_{RES}).

$$F_{RES} \approx \frac{1}{2\pi}\sqrt{\frac{(C_1 + C_2)}{L_{FILT}C_1C_2}} \qquad (7)$$

The design process for this type of filter is iterative in nature since each component selection drives the selection of the others.

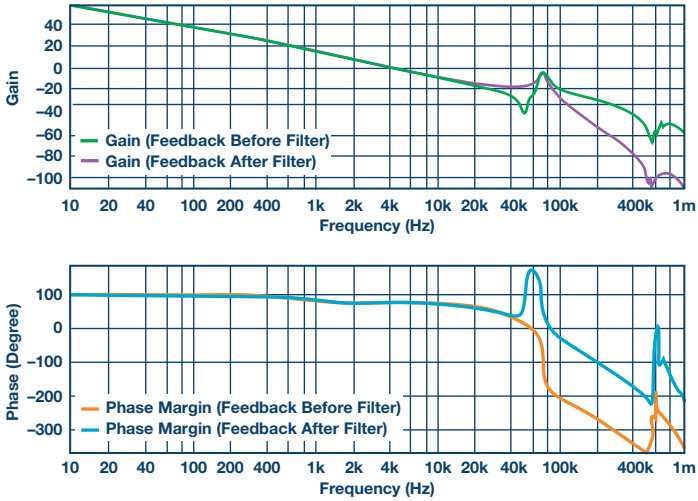

Figure 5. Phase and gain plots for a boost converter with an LC filter on the output.

Design Process for an LC Filter Using Parallel Resistor Damping (Technique 1 in Figure 4)

Step 1: Choose C_1 as if there was not going to be an output filter on the output. 5 mV to 20 mV p-p is a good place to start. C_1 can then be calculated using Equation 8.

$$C_1 = \frac{\Delta I_{PP}}{8F_{SW}\Delta V_{OUT}^{RIP} - \Delta I_{PP}R_{ESR}} \qquad (8)$$

Step 2: Select the inductor L_{FILT}. Based on experience, a good value is between 0.5 µF to 2.2 µF. The inductor should be chosen for a high self-resonant frequency (SRF). Larger inductors have larger SRFs, which means they are less effective for high frequency noise filtering. Smaller inductors will not have as much effect on ripple and will require more capacitance. The higher the switching frequency is the smaller the inductor can be. When comparing two inductors with the same inductance, the part with higher SRF will have lower interwinding capacitance. The interwinding capacitances acts like a short circuit around the filter for high frequency noise.

Step 3: As described previously, adding the filter will affect the compensation of the converter by reducing the achievable crossover frequency (F_u). For a current-mode conversion, the maximum achievable F_u is the lesser of 1/10 of the switch frequency, or 1/5 the F_{RES} of the filter as calculated in Equation 7. Fortunately, most analog loads do not require an exceptionally high transient response. Equation 9 calculates the approximate output capacitance (C_{BW}) required on the output of a converter to provide for a specified transient current step.

$$C_{BW} = \frac{I_{STEP}}{\pi F_u(\Delta V_{OUT}^{RIP} - I_{STEP}R_{ESR})} \quad (9)$$

Step 4: Set C_2 as the minimum of C_{BW} and C_1.

Step 5: Calculate the approximate damping filter resistance using Equation 10 and Equation 11. These equations are not absolutely accurate, but they are the closest thing to a closed form solution without the need to use extensive algebra. The ADIsimPower design tools calculate R_{FILT} by calculating the open-loop transfer function (OLTF) of the converter with the filter and with the inductor shorted out. R_{FILT} values are then guessed until the peak of the converter OLTF with the filter is only 10 dB above the OLTF of the converter with the inductor shorted. This technique can be used in a simulator like ADIsimPE or in the lab using a spectrum analyzer.

$$\omega_O = \sqrt{\frac{2(C_1 + C_2)}{(L_{FILT}C_1C_2)}} \quad (10)$$

$$R_{FILT} = \frac{\left(R_{LOAD}L_{FILT}(C_1 + C_2) - \frac{L_{FILT}}{\omega_O}\right)}{\frac{R_{LOAD}(C_1 + C_2)}{\omega_O} - L_{FILT}C_1} \quad (11)$$

Step 6: C_2 can now be calculated using Equation 12 through Equation 15. a, b, c, and d are used to simplify Equation 16.

$$a = \frac{L_{FILT}R_{LOAD}\omega I_{PP}}{\Delta V_{OUT}^{RIP}} - L_{FILT}\omega - R_{LOAD}C_1R_{FILT}\omega \quad (12)$$

$$b = \frac{R_{FILT}R_{LOAD}I_{PP}}{\Delta V_{OUT}^{RIP}} - R_{FILT} + R_{FILT}L_{FILT}C_1\omega^2, + R_{LOAD}C_1L_{FILT}\omega^2 \quad (13)$$

$$c = R_{FILT}R_{LOAD}\omega - R_{FILT}R_{LOAD}C_1L_{FILT}\omega^3 \quad (14)$$

$$d = -R_{LOAD}R_{FILT}\omega^2 \quad (15)$$

$$C_2 = \sqrt{\frac{a^2 + b^2}{c^2 + c^2}} \quad (16)$$

Step 7: Step 3 through Step 5 should be repeated until a well damped filter design is calculated that meets the required ripple and transient specifications. It should be noted that these equations ignore the dc series resistance of the filter inductor R_{DCR}. This resistance can be quite significant for lower current supplies. It improves filter performance by helping to dampen the filter, which increases the required R_{FILT} and increases the impedance of the filter. Both effects can significantly improve the performance of the filter. It can therefore be very helpful for low noise requirements to trade off a small amount of power loss in L_{FILT} for improved noise performance. Core loss in L_{FILT} also helps to attenuate some of the high frequency noise. Therefore, high current-powdered iron cores can be a good choice. They also tend to be smaller and cheaper for the same current capability. ADIsimPower of course factors in both the resistance of the filter inductor in addition to the ESR of the two capacitors for maximum accuracy.

Step 8: When choosing actual components to match the calculated values, remember to derate the capacitances of any ceramic capacitors to account for dc bias!

As stated previously, Figure 4 gives two viable techniques for damping the filter. If instead of choosing a parallel resistor, a capacitor C_D can be chosen to damp the filter. This will add some cost, but it provides the best filter performance of any technique.

Design Process for an LC filter Using an RC Damping Network (Technique 2 in Figure 4)

Step 1: As in the previous topology, choose C_1 as if there were not going to be an output filter. 10 mV p-p to 100 mV p-p is a good place to start, depending on the final target output ripple. C_1 can then be calculated using Equation 8. C_1 can be smaller in this topology than the previous topologies because the filter is more effective.

Step 2: As in the previous topology an inductor between 0.5 µH to 2.2 µH is chosen. 1 µH is a good value for converters between 500 kHz and 1200 kHz.

Step 3: As before, C_2 can be chosen from Equation 16, but with R_{FILT} set to something large like 1 MΩ since it will not be populated. The reason this is the same value despite C_1 having an additional capacitor is that in order to provide good damping, R_D will be made large enough that C_D will not significantly reduce the ripple. Set C_2 as the minimum of the calculated C_2 value, C_{BW} and C_1. It can be useful at this point to return to Step 1 and adjust the ripple assumed on C_1 to get a calculated C_2 that is closer to C_{BW} and C_1.

Step 4: C_D should be set to the same value as C_1. In theory you can achieve more damping of the filter using a larger capacitance, but it needlessly adds to the cost and size, and it can reduce converter bandwidth.

Step 5: R_D can be calculated from Equation 17. F_{RES} is calculated using Equation 7, ignoring the presence of C_D. This is a good approximation since Rd is typically large enough that C_D will have little effect on the location of the filter resonance.

$$R_D = \frac{1}{\pi C_1 F_{RES}} \quad (17)$$

Step 6: Now that both C_D and R_D have been calculated either a ceramic capacitor with a series resistance can be used, or a tantalum or similar capacitor with large ESR should be chosen that matches the calculated specifications.

Step 7: When choosing actual components to match the calculated values, remember to derate the capacitances of any ceramic capacitors to account for dc bias!

Another filter technique is to replace the L in the previous filter with a ferrite bead. However, this arrangement has many drawbacks that limit its effectiveness at filtering switching noise and does almost nothing for switching ripple. First is saturation. The ferrite bead will saturate at a very low level of bias current, meaning that the ferrite will give much lower impedance than shown in the zero bias curves shown in all data sheets. It may still need damping since it is still an inductor and therefore can resonate with the output capacitance. However, now the inductance is variable and poorly characterized in the very minimal data provided in most data sheets. For this reason ferrite beads are not recommended for use as a second stage filter, but can be used downstream from one to further reduce very high frequency noise.

Conclusion

This article has laid out several output filter techniques for switching power supplies. For each topology, a step-by-step design process has been devised to reduce the amount of guess and check required for filter design. The equations have been simplified somewhat so that they are useful to an engineer looking to do a quick design by understanding what is achievable from a second stage output filter.

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