Design Example Report

Title	***184 W LLC CV/CC Power Supply Using HiperLCS™ LCS705HG and LinkSwitch™-TN LNK302D***
Specification	90 VAC – 132 VAC Input; 184 W (23 V at 0.5 A - 8 A) Output
Application	Battery Charger
Author	Applications Engineering Department
Document Number	DER-447
Date	May 31, 2017
Revision	4.4

Summary and Features

- Integrated LLC stage for a very low component count design
- 90-132 VAC voltage doubler input (no PFC)
- 100 kHz LLC for wide input/output operating range
- >90% full load efficiency

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. All testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a 23 V (nominal), 184 W reference design for a power operating from 90 VAC to 132 VAC. The power supply is designed with a constant voltage / constant current output for use in battery charger applications.

The design is based on the LCS705HG operating from doubled mains, with no PFC input stage. This design poses special challenges in that the primary and secondary voltages of the LLC converter both vary over a wide range.

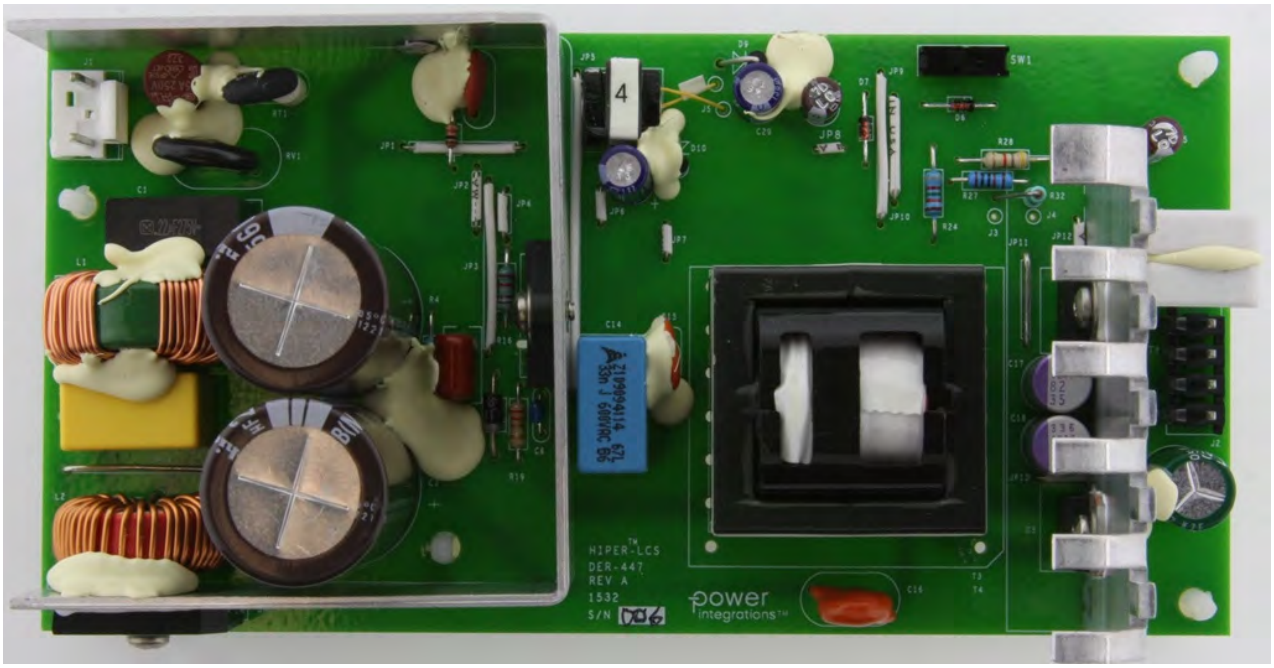

Figure 1 – Photograph, Top View.

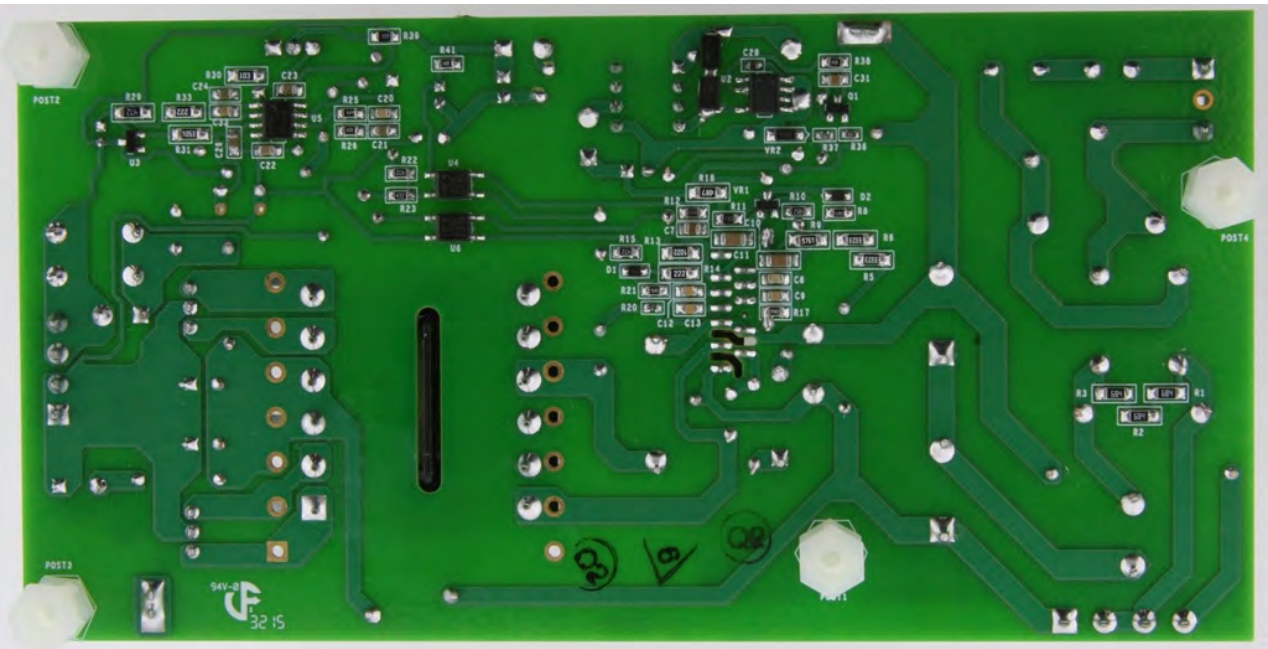

Figure 2 – Photograph, Bottom View.

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2 Power Supply Specification

The table below represents the specification for the design detailed in this report. Actual performance is listed in the results section. Detailed customer specification is shown below.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		132	VAC	3 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Main Converter Output						
Output Voltage	V_{OUT}	0		23	V	23 VDC (Nominal – Otherwise Defined by Battery Load).
Output Current	I_{OUT}	6		8	A	Nominal Current Limit Setting for Design.
Output Current Limit (optional)			0.5	1	A	Programmed Using Additional Resistor.
Total Output Power						
Continuous Output Power	P_{OUT}		184		W	23 V / 8 A
Peak Output Power	$P_{OUT(PK)}$			N/A	W	
Efficiency						
Total system at Full Load	η_{Main}		90		%	Measured at 115 VAC, Full Load.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950 / UL1950 Class II				
Surge						1.2/50 μs surge, IEC 1000-4-5,
Differential					kV	Differential Mode: 2 Ω
Common Mode					kV	Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	0		60	°C	See Thermal Section for Conditions.

2.1 Actual Customer Specification for Output Voltage / Current Limit

An actual customer specification for output voltage and current is shown below, and is considerably more complex than the simple implementation described in this report. The end application will incorporate a microcontroller that performs the function of battery recognition/authentication, and selection of output voltage and current limit depending on battery type and state of charge. Output voltage and current limit can be programmed by manipulating the reference voltages feeding the output voltage/current sensing amplifiers in the secondary control circuit.

The circuit shown in this report is designed to supply the maximum output voltage of 23 V with output current limit set to a nominal value of 8 A. A pair of holes is provided on the printed circuit board to allow inserting an extra resistor to program the output current limit down to 0.5 A in order to examine the behavior of the supply at this current limit.

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Output Voltage	V_O	0	12/14/18	23	VDC	Programmed by microcontroller depending on battery type
Output Current	I_{O1}	0.45	0.5	1	A	Programmed by microcontroller when V_{OUT} is 0-9 V
	I_{O2}	4.5		6	A	Programmed by microcontroller when battery voltage is 12-15 V for 18 V battery. Current limit is pulsed from 4.5 to 6 A.
	I_{O3}	6		8	A	Full current charging, when battery voltage is 15-18 V, set be microcontroller

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3 Schematic

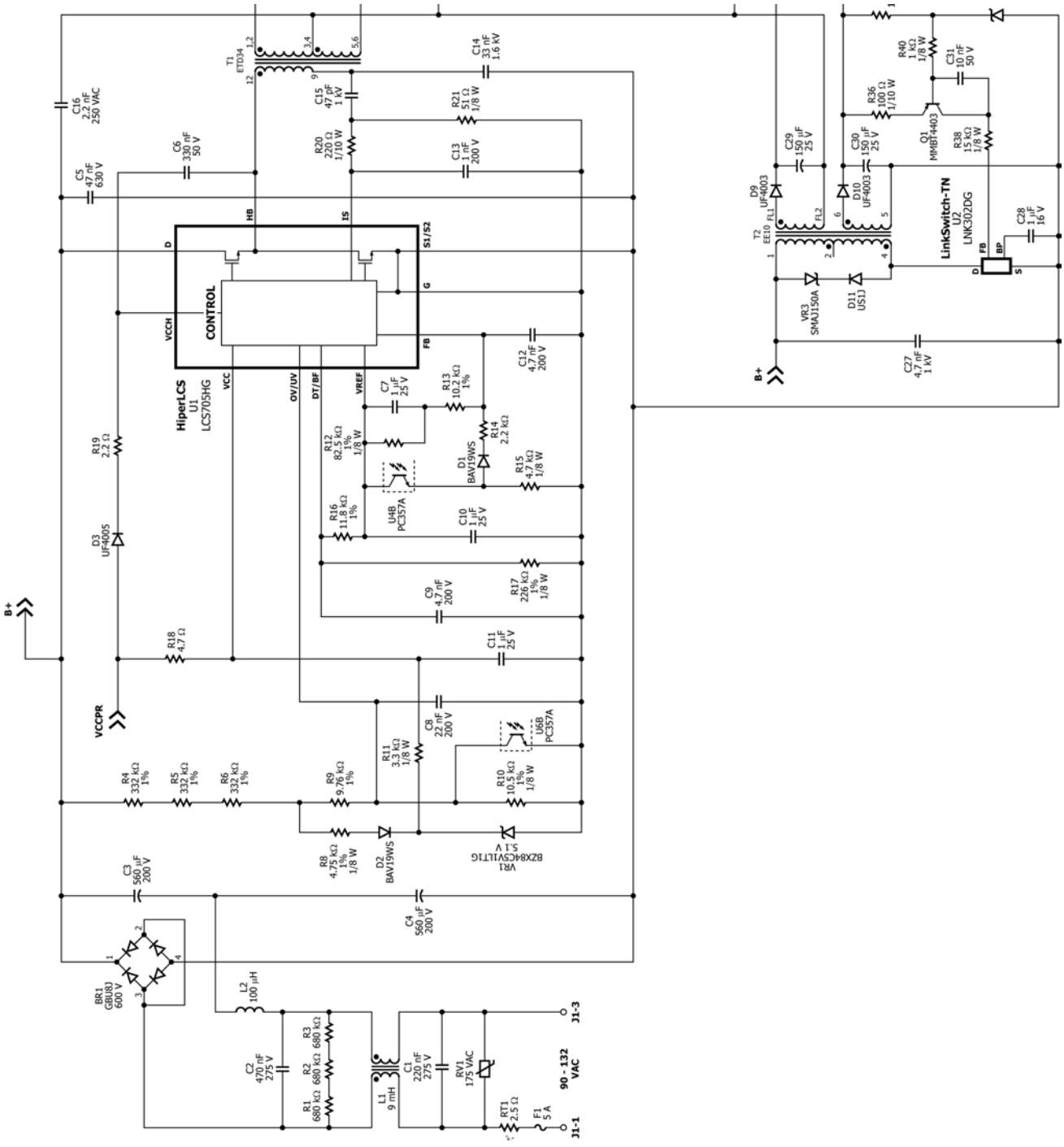

Figure 3a – Schematic. Battery Charger Application Circuit - Input Filter, LLC Stage, Bias Supplies.

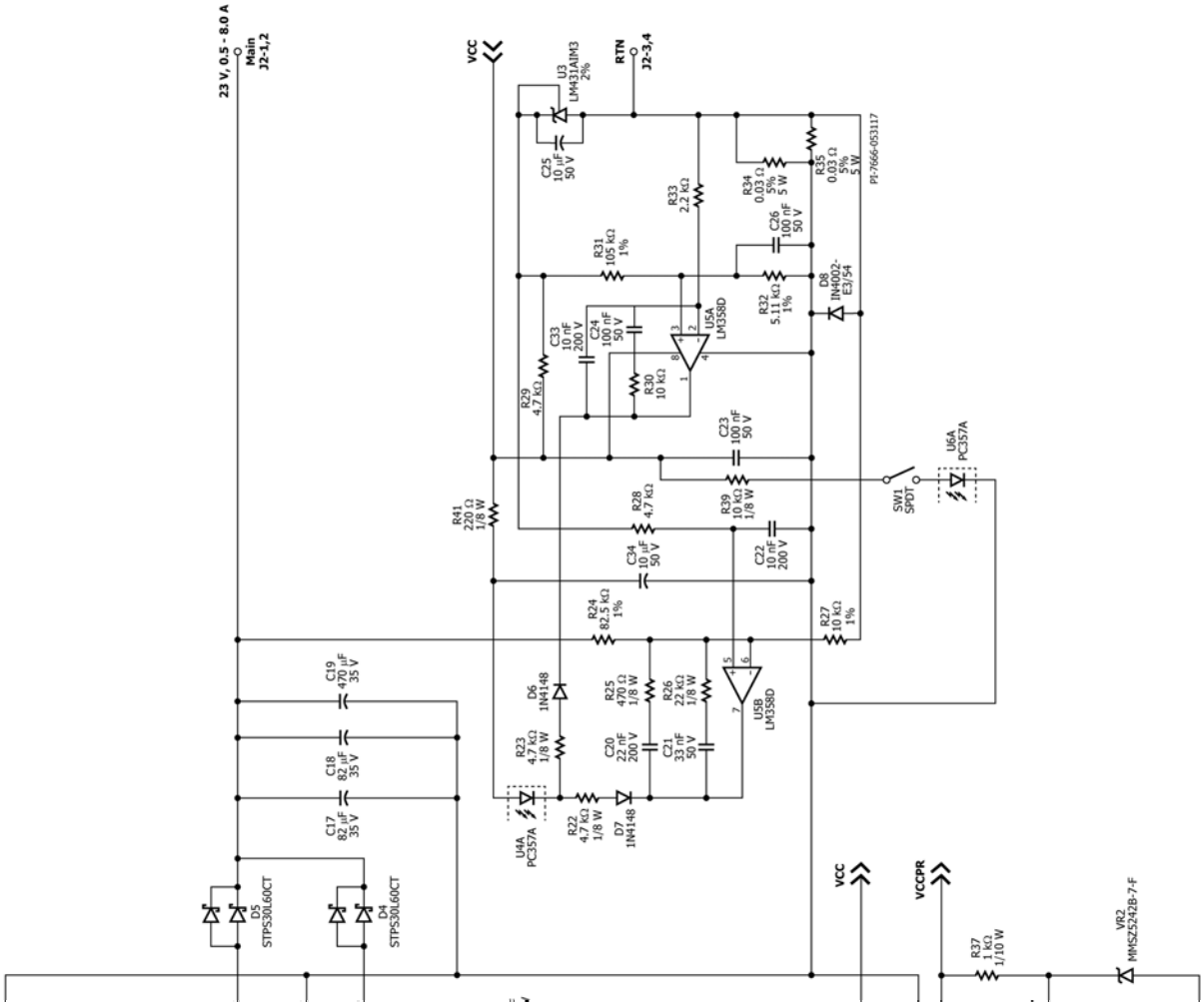

Figure 3b – Schematic. Output Voltage/Current Control.

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4 Circuit Description

4.1 General Topology

The schematic in Figure 3 shows an LLC power supply utilizing the LCS705HG, powered via a voltage doubler. The LNK302D is utilized in a flyback bias supply that provides power for both primary and secondary control circuitry. The secondary control circuitry provides CV/CC control for use in battery charger applications

4.2 EMI Filtering / Voltage Doubler

Capacitors C1 and C2 are used to control differential mode noise. Resistors R1-3 discharge C1 and C2 when AC power is removed. Inductor L1 controls common mode EMI. The heat sink for U1 and BR1 is connected to primary return to eliminate the heat sink as a source of radiated/capacitive coupled noise. Thermistor RT1 provides inrush limiting. Capacitor C16 filters common mode EMI. Inductor L2 filters differential mode EMI. Capacitors C3 and C4, along with BR1 form a voltage doubler to provide a ~250 - 380 VDC B+ supply from the 90-132 VAC input.

4.3 Primary Bias Supply

Components U2, T2 Q1, VR2-3, D11, C27-28, C30-31, R36-38 and R40 comprise a regulated 12V flyback bias supply for U1. Components D9 and C29 generate a 12 V bias supply for the secondary control circuitry via a triple insulated winding on T2 Vr3 and D11 protect the U2 drain from leakage spikes.

4.4 LLC Converter

The schematic in Figures 3 depicts a 23 V, 184 W LLC DC-DC converter with constant voltage/ constant current output implemented using the LCS705HG. **Two main transformers are shown in the schematic and layout, T1 (ETD34) and T3 (ETD39). Only the ETD34 transformer, T1, is used in this example.**

Integrated circuit U1 incorporates the control circuitry, drivers and output MOSFETs necessary for an LLC resonant half-bridge (HB) converter. The HB output of U1 drives output transformer T1 via a blocking/resonating capacitor (C14). This capacitor was rated for the operating ripple current and to withstand the high voltages present during fault conditions.

Transformer T1 was designed for a leakage inductance of ~70 μH. This, along with resonating capacitor C14, sets the primary series resonant frequency at ~105 kHz according to the equation:

$$f_R = \frac{1}{6.28\sqrt{L_L \times C_R}}$$

Where f_R is the series resonant frequency in Hertz, L_L is the transformer leakage inductance in Henries, and C_R is the value of the resonating capacitor (C14) in Farads.

The transformer turns ratio was set by adjusting the primary turns such that the operating frequency at nominal input voltage and full load is greater than, the previously described resonant frequency at the minimum B+ voltage (bottom of the ripple waveform) at 90 VAC.

An operating frequency of 100 kHz was found to be a good compromise between transformer size and operating frequency dynamic range, in view of the wide variation of input and output voltage encountered in this application.

The number of secondary winding turns was chosen to provide a compromise between core and copper losses. AWG #42 Litz wire was used for the primary and AWG #40 for the secondary windings,

The core material selected was Ferroxcube 3F3. This material provided good (low loss) performance.

Components D3, R19, and C6 comprise the bootstrap circuit to supply the internal high-side driver of U1.

Components R18 and C10 provide filtering and bypassing of the +12 V input and the V_{CC} supply for U1. *Note: V_{CC} voltage of >15 V may damage U3.*

Voltage divider resistors R4-10 set the high-voltage turn-on, turn-off, and overvoltage thresholds of U1. The voltage divider values are chosen to set the LLC turn-on point at ~232 VDC and the turn-off point at 184 VDC, with an input overvoltage turn-off point at 400 VDC. Built-in hysteresis sets the input under voltage turn-off point at 184 VDC. Components VR1, D2, R8, and R11 change the slope of the input voltage sensing network to allow U1 to operate over a wide range of input voltage without prematurely engaging the U1 OV shutdown. Without this clamp circuit, the supply would start at ~85 VAC, but would enter OV shutdown before the nominal 115 VAC operating voltage is reached.

Capacitor C5 is a high-frequency bypass capacitor for the U1 B+ supply, connected with short traces between the D and S1/S2 pins of U3.

Capacitor C15 forms a current divider with C14, and is used to sample a portion of the primary current. Resistor R21 senses this current, and the resulting signal is filtered by R20 and C13. Capacitor C15 should be rated for the peak voltage present during fault conditions, and should use a stable, low-loss dielectric such as metalized film, SL ceramic, or NPO/COG ceramic. The capacitor used in the DER-447 is a ceramic disc with

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"COG/NPO" temperature characteristic. The values chosen set the 1 cycle (fast) current limit at 12.2 A, and the 7-cycle (slow) current limit at 6.8 A, according to the equation:

$$I_{CL} = \frac{0.5}{\left(\frac{C15}{C15 + C14}\right) \times R21}$$

I_{CL} is the 7-cycle current limit in Amperes, R40 is the current limit resistor in Ohms, and C30 and C31 are the values of the resonating and current sampling capacitors in nanofarads, respectively. For the one-cycle current limit, substitute 0.9 V for 0.5 V in the above equation.

Resistor R20 and capacitor C13 filter primary current signal to the IS pin. Resistor R20 is set to 220 Ω, the minimum recommended value. The value of C13 is set to 1 nF to avoid nuisance tripping due to noise, but not so high as to substantially affect the current limit set values as calculated above. These components should be placed close to the IS pin for maximum effectiveness. The IS pin can tolerate negative currents, the current sense does not require a complicated rectification scheme.

The Thevenin equivalent combination of R16 and R17 sets the dead time at 500 ns and maximum operating frequency for U1 at 542 kHz. The DT/BF input of U1 is filtered by C9. The combination of R16 and R17 also selects burst mode "1" for U1. This sets the lower and upper burst threshold frequencies at 236 kHz and 270 kHz, respectively.

The FEEDBACK pin has an approximate characteristic of 2.6 kHz per μA into the FEEDBACK pin. As the current into the FEEDBACK pin increases so does the operating frequency of U1, reducing the output voltage. The series combination of R12 and R13 sets the minimum operating frequency for U1 at 83 kHz. This value was set to be slightly lower than the frequency required for regulation at full load and minimum bulk capacitor voltage. Resistor R12 is bypassed by C7 to provide output soft start during start-up by initially allowing a higher current to flow into the FEEDBACK pin when the feedback loop is open. This causes the switching frequency to start high and then decrease until the output voltage reaches regulation. Resistor R16 is typically set at the same value as the parallel combination of R12 and R13 so that the initial frequency at soft-start is equal to the maximum switching frequency as set by R16 and R17. If the value of R16 is less than this, it will cause a delay before switching occurs when the input voltage is applied.

Optocoupler U4 drives the U1 FEEDBACK pin through R14, which limits the maximum optocoupler current into the FEEDBACK pin. Capacitor C12 filters the FEEDBACK pin. Resistor R15 loads the optocoupler output to force it to run at a relatively high quiescent current, increasing its gain. Resistors R14 and R15 also improve large signal step response and burst mode output ripple. Diode D1 isolates R15 from the F_{MAX}/soft start network.

4.5 Output Rectification

The output of transformer T1 is rectified and filtered by D4-5 and C17-19. Capacitors C17-18 are aluminum polymer capacitors chosen for output ripple current rating. Capacitor C19 provides damping to make frequency compensation easier. Output rectifiers D4 and D5 are 60 V Schottky rectifiers chosen for high efficiency. Intertwining the transformer secondary halves (see transformer construction details in section 7) reduces leakage inductance between the two secondary halves, reducing the worst-case peak inverse voltage and allowing use of a 60 V Schottky diode with consequent higher efficiency.

4.6 Output Current and Voltage Control

Output current is sensed via resistors R34 and R35. These resistors are clamped by diode D8 to avoid damage to the current control circuitry during an output short circuit. Components R29 and U3 provide a voltage reference for current sense and voltage sense amplifiers U5A and U5B. The reference voltage for current sense amplifier U5A is divided down by R31-32, and filtered by C26. **The default current limit setting for DER-447 is 8 A, as programmed by R34-35 and R31-32. An extra resistor can be placed from J3-J4 (across R32) to program a lower current limit.** Voltage from the current sense resistors is applied to the inverting input of U5A via R33. Opamp U5A drives optocoupler U4 via D6 and R23. Components R30, R33, R23, C24, and C33 are used for frequency compensation of the current loop. Opamp U5B is used for output constant voltage control when the current limit is not engaged. Resistors R24 and R27 sense the output voltage. A reference voltage is applied to the non-inverting input of U5B from U3 via filter components R28 and C22. Opamp U5B drives optocoupler U4 via D7 and R22. Components R22, R24, R25-27, C20, and C21 all affect the frequency compensation of the voltage control loop.

Components R39, SW1, and U6 provide remote start. When SW1 is opened, the output transistor of U6 pulls down on the OV/UV pin of U1, activating undervoltage shutdown. Closing SW1 turns off U6, allowing a normal start-up sequence for U1.

4.7 Designing Input Undervoltage / Overvoltage Network for U1

The UV/OV threshold voltages for the HiperLCS are set to a fixed ratio of 131% (nominal), optimized for operation with a boost PFC front end. If this part is used with a voltage doubler input stage instead, the B+ voltage range is too wide to be accommodated by using a simple voltage divider to feed the OV/UV pin. If the voltage divider is set so that the HiperLCS starts properly at the low end of the operating range (~85 VAC), the HiperLCS B+ OV protection will cause the device to shut down before the nominal operating voltage of 115 VAC is reached.

There are two solutions to this problem – the first is to clamp the voltage at the UV/OV pin of the HiperLCS so as to disable the OV function. A more desirable solution is to use a “soft clamp” to shape the output of the UV/OV voltage divider so that OV protection is

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reached at a higher B+ voltage while still retaining the original UV set point. A circuit to accomplish this is shown in Figure 4.

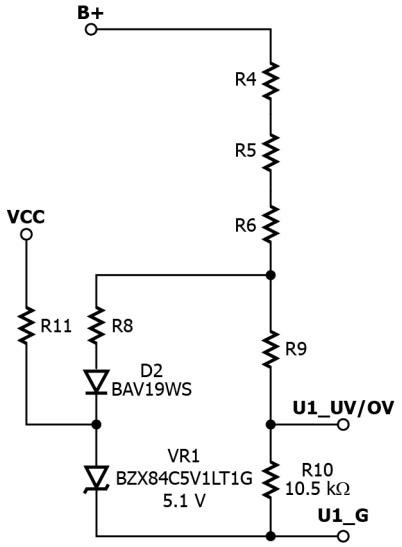

Figure 4 – UV/OV Divider Network.

Components R8, R9, R11, D2, and VR1 are used to shape the output voltage characteristics of the divider network as shown in Figure 5, introducing a change of slope that shifts the OV shutdown threshold to a higher B+ voltage.

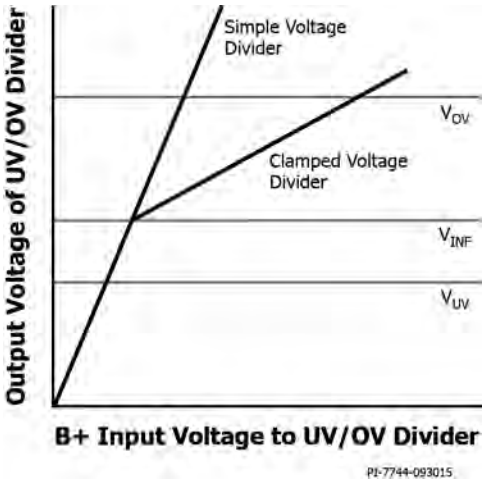

Figure 5 – Comparison of Clamped vs. Unclamped UV/OV Voltage Divider Network.

In Figure 5, a clamped voltage divider is compared to a simple unclamped version, showing the curve shaping that allows a higher B+ V_{OV} setting than an unclamped divider while keeping the same V_{UV} set point.

4.7.1 *Establishing Voltage Set Points*

In order to properly calculate the values needed for the clamped voltage divider network, five voltage set points are needed. These are: the internal V_{UV} and V_{OV} threshold voltages for the HiperLCS IC, the desired B+ low voltage turn-on and OV shutdown thresholds (V_{ON} and V_{OFF}), and the inflection voltage (V_{INF}) where the voltage divider curve changes slope.

4.7.1.1 V_{UV} and V_{OV}

Voltages V_{UV} and V_{OV} are preset inside the HiperLCS IC. The nominal V_{UV} threshold is set at 2.4 V. The nominal V_{OV} threshold is 131% of this value, or 3.14 V. This is covered in the HiperLCS data sheet.

4.7.1.2 V_{ON} and V_{OFF}

In this design example, the operating input voltage range is defined as 90-132 VAC. Since the AC input is feeding a voltage doubler, the B+ voltage will be 2.8 X V_{IN}, so the nominal B+ will vary from 252-370 VDC. For this exercise, the V_{OFF} point will be set at 400 VDC, sufficiently out of the way of normal operating range to prevent nuisance tripping, but low enough to protect against input voltage swells and surges.

To choose the V_{ON} or $V_{BROWNIN}$ point, PIXls was used. A V_{BULK_NOM} of 250 VDC was chosen in the PIXls input parameters – this yields a $V_{ON}/V_{BROWNIN}$ of 232 VDC, as shown in Figure 6.

1	HiperLCS_042413; Rev.1.3; Copyright Power Integrations 2013	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_042413_Rev1-3.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
2	▾ Enter Input Parameters					Design Title
3	Vbulk_nom	250		250	V	Nominal LLC input voltage
4	Vbrownout			184	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
5	Vbrownin			232	V	Startup threshold on bulk capacitor
6	VOV_shut			306	V	OV protection on bulk voltage
7	VOV_restart			295	V	Restart voltage after OV protection.
8	CBULK	235.00		235	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbrownout to change bulk cap value
9	tHOLDUP			17.3	ms	Bulk capacitor hold up time
10						
11						

Figure 6 – Using PIXls to Determine $V_{ON}/V_{BROWNIN}$.

4.7.1.3 Inflection Voltage (V_{INF})

The HiperLCS PIXls spreadsheet assumes that a normal unclamped voltage divider is used to feed the HiperLCS UV/OV pin. A $V_{BROWNIN}/V_{ON}$ voltage of 232 V, allowing the HiperLCS to turn on and run reliably at 90 VAC, will result in a overvoltage shutdown point (V_{OV_SHUT}) of 306 VDC, as shown on line 6 of Figure 6. For a nominal 115 VAC operating voltage, the B+ is already at 115 X 2.8 = 322 VDC, so the OV shutdown feature of the HiperLCS would cause the supply to shut down even before a normal AC

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operating voltage is reached. This is the reason for using a clamped voltage divider to push up the B+ voltage where OV shutdown occurs.

To design a clamped voltage divider a voltage V_{INF} is defined, which sets the B+ voltage at which the V_{OUT} vs. V_{IN} curve of the voltage divider changes slope. This should happen somewhat above the nominal low line operating B+ of 250 VDC, but comfortably below the unclamped V_{OV_SHUT} of 306 VDC as defined in Figure 6. **For this design example, a V_{INF} of 280 VDC was chosen.**

Table 1 summarizes the voltages necessary for calculating the clamped voltage divider in this design example.

Voltages for Calculating Clamped Voltage Divider				
V_{UV}	**V_{OV}**	**V_{ON} / $V_{BROWNIN}$**	**V_{OFF}**	**V_{INF}**
2.4 VDC	3.14 VDC	232 VDC	400 VDC	280 VDC

Table 1 – Voltages for Calculating Clamped Voltage Divider Network.Setting Initial Voltage Divider Values.

In order to set the total values for voltage divider string R4-R6, R9, and R10, an initial value for R10 is chosen. In this example, R10 = 10.5 kΩ was chosen. This yielded realizable 1% resistor values for the rest of the resistors in the network. Once R10 is chosen, the top half of the voltage divider (R4 + R5 + R6 + R9 = R_{SUM}) can be calculated using the values for V_{UV} and V_{ON}:

$R_{SUM} = [R10 (V_{ON}-V_{UV})]/V_{UV} = [10.5 (232 - 2.4)]/2.4 = 1004.5$ kΩ

This value for R_{SUM} can then be used with the Value for V_{INF} to calculate the value necessary for R9.

V_{INF} is defined as the point at which the slope of the voltage divider changes. This happens when the voltage drop across R9 and R10 is equal to the combined voltage drops of VR1 and D2. VR1 is pre-biased by R11 to its nominal voltage drop of 5.1 V. Diode D2 will barely start conducting at ~0.5 V. Given this, the combined voltage drops add up to 5.6 V, and the value for R9 can be calculated as:

$R9 = [5.6(R_{SUM} + R10)-(V_{INF} X R10)]/V_{INF} = [(5.6 X 1015)-(280 X 10.5)]/280 = 9.8$ kΩ

The closest 1% resistor value is 9.76 kΩ.

Resistor R11 is used to pre-bias Zener diode VR1. This bias current not only applies reverse bias to diode D2 to keep it from conducting before necessary, but also establishes a well-defined voltage drop across VR1. The value chosen for R11 results in a bias current of ~2 mA through VR1.

Since R9 and R_{SUM} are both defined, the rest of the resistors in the R_{SUM} chain can be calculated.

$R4\text{-}R6 = (R_{SUM} - R9)/3 = (1004.5 – 9.76)/3 = 331.58$ kΩ

The closest 1% value is 332 kΩ.

4.7.1.4 Setting Clamp Resistor R8

In order to set the proper value for clamp resistor R8, it first necessary to find the voltage V_{SD} across R9 and R10 that will result in OV shutdown for U1. This will be the voltage across R9 and R10 that will provide 3.14 V to the U1 UV/OV pin.

$V_{SD} = V_{OV} [1 + (R9/R10)] = 3.14 (1 + 0.9295) = 6.059$ V

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This is the voltage across R9 and R10 necessary to reach the OV threshold at the UV/OV pin of U1.

It is next necessary to calculate voltage V_{SD} at the junction of R6 and R9 at the B+ shutdown voltage V_{OFF} of 400 VDC**. This voltage is calculated as if R8 is open**.

$V_{SD} = 400[(R9 + R10)/(R4 + R5 + R6 + R9 + R10)] = 7.97$ V

Using V_{SD} and V_{SD}', we can now set up the calculation for R8.

The voltage divider of R4-6, R9, and R10 driven by the V_{OFF} value of 400 V can be re-expressed as a voltage source V_{SD} driving a Thevenin equivalent resistance. The Thevenin resistance R_{TH} is equivalent to the parallel combination of the top and bottom halves of the voltage divider:

$R_{TH} = (R4 + R5 + R6)$ II $(R9 + R10) = 19.6$ kΩ

Once this is determined, the voltage divider and clamp can be reduced to the schematic shown in Figure 7.

From the simple equivalent schematic of Figure 7, it is straightforward to calculate R8:

$R8 = R_{TH} (V_{SD} - 5.6)/(V_{SD} - V_{SD}) = (19.6(6.059 - 5.6))/(7.97 - 6.059) = 4.704$ kΩ

The nearest 1% value is 4.75 kΩ

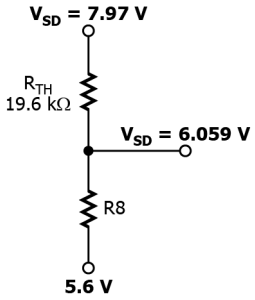

Figure 7 – Voltage Divider and Clamp Thevenin Equivalent for Calculating R8.

5 PCB Layout

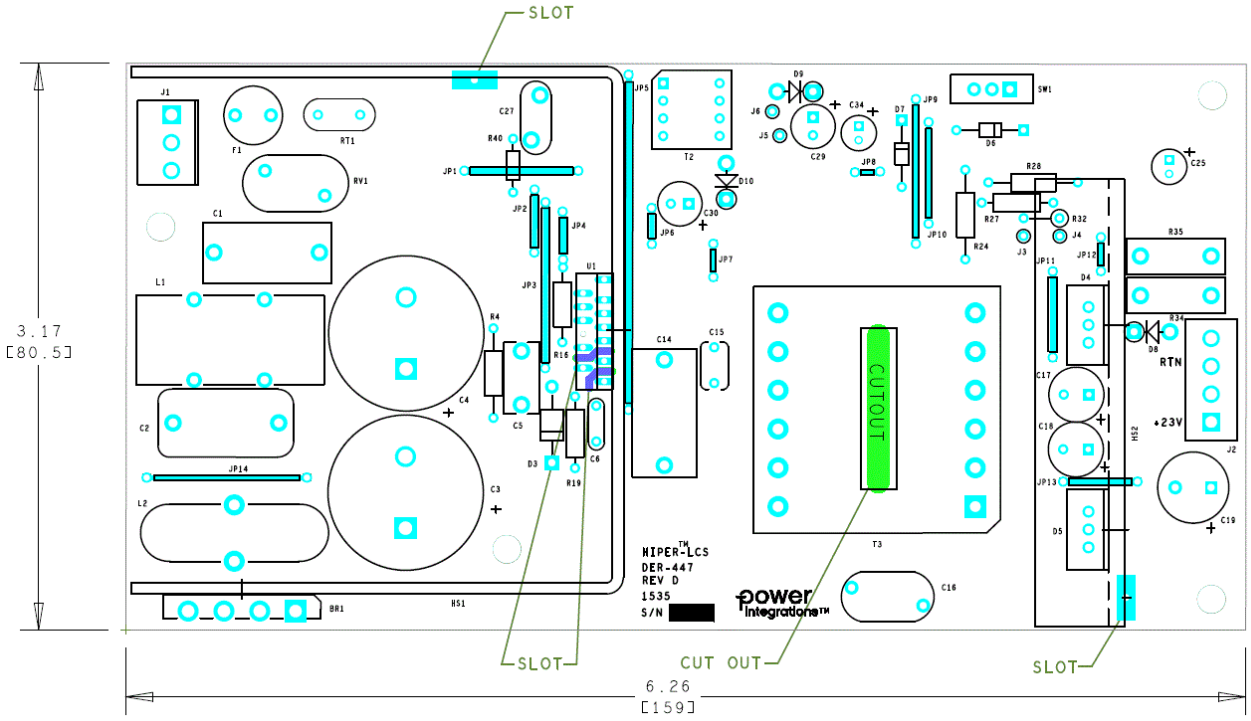

Figure 8 – Printed Circuit Layout, Top Side.

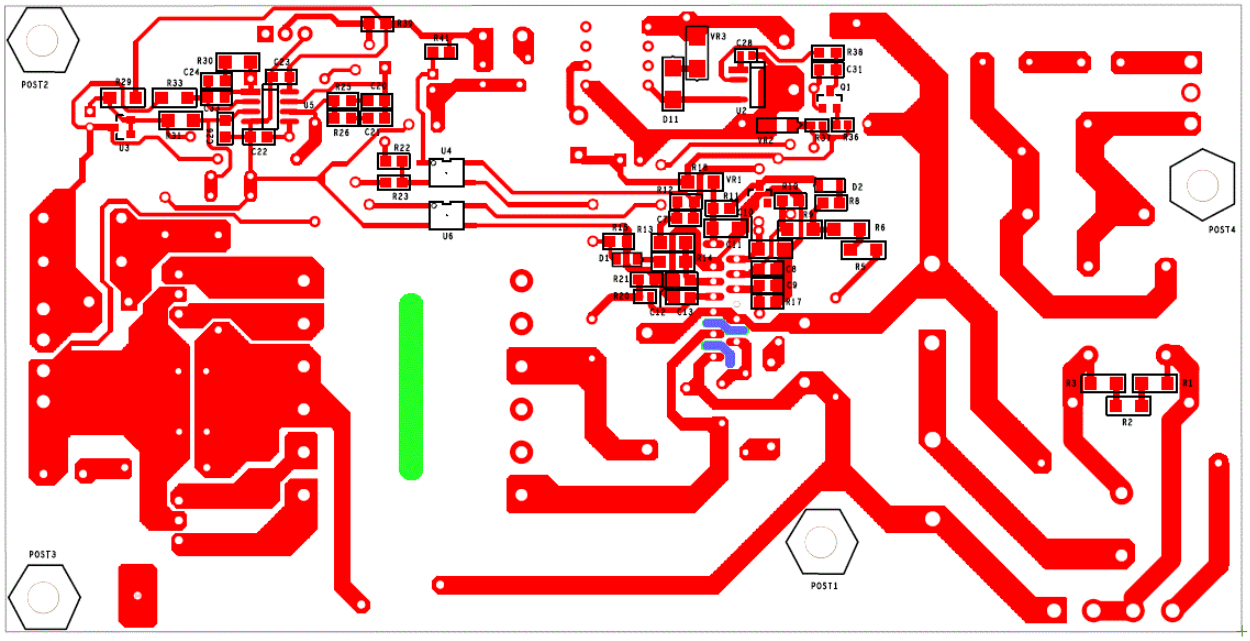

Figure 9 – Printed Circuit Layout, Bottom Side.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 8 A, Bridge Rectifier, GBU Case	GBU8J-BP	Micro Commercial
2	1	C1	220 nF, 275 VAC, Film, X2	ECQ-U2A224ML	Panasonic
3	1	C2	470 nF, 275 VAC, Film, X2	PX474K31D5	Carli
4	2	C3 C4	560 µF, 200 V, Electrolytic, 20 %, Gen. Purpose, (22 x 52 mm)	UPB2D561MRD	Nichicon
5	1	C5	47 nF, 630 V, Film	MEXPD24704JJ	Duratech
6	1	C6	330 nF, 50 V, Ceramic, X7R	FK24X7R1H334K	TDK
7	1	C7	1 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
8	2	C8 C20	22 nF, 200 V, Ceramic, X7R, 0805	08052C223KAT2A	AVX
9	2	C9 C12	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX
10	2	C10 C11	1 µF, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK
11	1	C13	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
12	1	C14	CAP FILM 33 nF 1.6 kV METALPOLYPRO	B32672L1333J000	Epcos
13	1	C15	47 pF, 1 kV, COG Disc Ceramic	561R10TCCQ47	Vishay
14	1	C16	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
15	2	C17 C18	82 µF, 35 V, l Organic Polymer, Gen. Purpose, (8 x 12)	35SEPF82M+TSS	Panasonic
16	1	C19	470 uF, 35 V, Electrolytic, Very Low ESR, 23 mΩ, (10 x 20)	EKZE350ELL471MJ20S	Nippon Chemi-Con
17	1	C21	33 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB333	Yageo
18	2	C22 C33	10 nF, 200 V, Ceramic, X7R, 0805	08052C103KAT2A	AVX
19	3	C23 C24 C26	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
20	2	C25 C34	10 µF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL100ME11D	Nippon Chemi-Con
21	1	C27	4.7 nF, 1 kV, Thru Hole, Disc Ceramic	562R5GAD47	Vishay
22	1	C28	1 µF, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
23	2	C29 C30	150 µF, 25 V, Electrolytic, Low ESR, 180 mΩ, (6.3 x 15)	ELXZ250ELL151MF15D	Nippon Chemi-Con
24	1	C31	10 nF, 50 V, Ceramic, X7R, 0805	C0805C103K5RACTU	Kemet
25	1	CLIP_LCS_PFS2	Heat sink Hardware, Clip LCS_II/PFS	EM-340V0B	Kang Yang
26	2	D1 D2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
27	1	D3	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
28	2	D4 D5	60 V, 30 A, Dual Schottky, TO-220AB	STPS30L60CT	ST
29	2	D6 D7	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
30	1	D8	100 V, 1 A, Rectifier, DO-41	1N4002-E3/54	Vishay
31	2	D9 D10	200 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4003-E3	Vishay
32	1	D11	DIODE ULTRA FAST, SW 600 V, 1 A, SMA	US1J-13-F	Diodes, Inc.
33	1	F1	5 A, 250 V, Slow, TR5	37215000411	Wickman
34	1	HOTMELT	Adhesive, Hot Melt, VO	3748 VO-TC	3M
35	1	HS1	FAB, HEAT SINK, BRIDGE_Esip, DER447		Custom
36	1	HS2	FAB, HEAT SINK, Diodes, DER447		Custom
37	1	J1	3 Position (1 x 3) header, 0.156 pitch, Vertical	B3P-VH	JST
38	1	J2	4 Position (1 x 4) header, 0.156 pitch, Vertical	26-48-1045	Molex
39	4	J3 J4 J5 J6	PCB Terminal Hole, #30 AWG	N/A	N/A
40	1	JP1	Wire Jumper, Insulated, #24 AWG, 0.7 in	C2003A-12-02	Gen Cable
41	1	JP2	Wire Jumper, Insulated, #24 AWG, 0.4 in	C2003A-12-02	Gen Cable
42	1	JP3	Wire Jumper, Insulated, #24 AWG, 1.0 in	C2003A-12-02	Gen Cable
43	2	JP4 JP6	Wire Jumper, Insulated, #24 AWG, 0.3 in	C2003A-12-02	Gen Cable
44	1	JP5	Wire Jumper, Insulated, TFE, #22 AWG, 1.9 in	C2004-12-02	Alpha
45	3	JP7 JP8 JP12	Wire Jumper, Insulated, #24 AWG, 0.2 in	C2003A-12-02	Gen Cable
46	1	JP9	Wire Jumper, Insulated, #24 AWG, 0.9 in	C2003A-12-02	Gen Cable

47	1	JP10	Wire Jumper, Insulated, TFE, #22 AWG, 0.6 in	C2004-12-02	Alpha
48	1	JP11	Wire Jumper, Non Insulated, #18 AWG, 0.5 in	296 SV001	Alpha
49	1	JP13	Wire Jumper, Non insulated, #22 AWG, 0.5 in	298	Alpha
50	1	JP14	Wire Jumper, Non insulated, #20 AWG, 0.9 in	8020 000100	Belden
51	1	L1	9 mH, 5 A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine Tech
52	1	L2	100 µH, 5 A, INDUCTOR TORD HI AMP 100 µH VERT	7447070	Wurth Elect
53	4	POST1 POST2 POST3 POST4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	561-0375A	Eagle Hardware
54	1	Q1	PNP, Small Signal BJT, 40 V, 0.6 A, SOT-23	MMBT4403-7-F	Diodes, Inc.
55	3	R1 R2 R3	680 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic
56	1	R4	332 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-332K	Yageo
57	2	R5 R6	332 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3323V	Panasonic
58	1	R8	4.75 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4751V	Panasonic
59	1	R9	9.76 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF9761V	Panasonic
60	1	R10	10.5 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1052V	Panasonic
61	1	R11	3.3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ332V	Panasonic
62	1	R12	82.5 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF8252V	Panasonic
63	1	R13	10.2 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1022V	Panasonic
64	2	R14 R33	2.2 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ222V	Panasonic
65	3	R15 R22 R23	4.7 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
66	1	R16	11.8 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-11K8	Yageo
67	1	R17	226 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2263V	Panasonic
68	1	R18	4.7 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ4R7V	Panasonic
69	1	R19	2.2 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-2R2	Yageo
70	1	R20	220 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ221V	Panasonic
71	1	R21	51 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ510V	Panasonic
72	1	R24	82.5 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-82K5	Yageo
73	1	R25	470 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ471V	Panasonic
74	1	R26	22 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ223V	Panasonic
75	1	R27	10.0 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-10K0	Yageo
76	1	R28	4.7 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-4K7	Yageo
77	1	R29	4.7 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ472V	Panasonic
78	1	R30	10 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ103V	Panasonic
79	1	R31	105 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1053V	Panasonic
80	1	R32	5.11 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-5K11	Yageo
81	2	R34 R35	0.03 Ω, 5 W, 5%, Current Sense	MPR5JB30L0	Stackpole
82	1	R36	100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
83	1	R37	1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
84	1	R38	15 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ153V	Panasonic
85	1	R39	10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
86	1	R40	1 kΩ, 5%, 1/8 W, Carbon Film	CF18JT1K00	Stackpole
87	1	R41	220 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ221V	Panasonic
88	1	RT1	NTC Thermistor, 2.5 Ohms, 5 A	SL10 2R505	Ametherm
89	3	RTV1 RTV2 RTV4	Thermally conductive Silicone Grease	120-SA	Wakefield
90	1	RV1	175 V, 70 J, 14 mm, RADIAL	ERZ-V14D271	Panasonic
91	4	SCREW1 SCREW2 SCREW3 SCREW4	SCREW MACHINE PHIL 4-40 X 1/4 SS	PMSSS 440 0025 PH	Building Fasteners
92	2	SPACER_CER1	SPACER RND, Steatite C220 Ceramic	CER-2	Richco

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		SPACER_CER2			
93	1	SW1	SWITCH SLIDE SPDT 30 V, 2 A PC MNT	EG1218	E-Switch
94	1	T2	Transformer, EE10, Vertical, 8 pins	101	Hical Magnetics
95	1	T3	Transformer, ETD34, Horizontal, 12 pins	WS-53404	Win Shine Tech
96	1	U1	HiperLCS, ESIP16/13	LCS705HG	Power Integrations
97	1	U2	LinkSwitch-TN, SO-8	LNK302DN	Power Integrations
98	1	U3	IC, REG ZENER SHUNT ADJ SOT-23	LM431AIM3/NOPB	National Semi
99	2	U4 U6	Optocoupler, 80 V, CTR 80-160%, 4-Mini Flat	PC357N1TJ00F	Sharp
100	1	U5	DUAL Op Amp, Single Supply, SOIC-8	LM358D	Texas Instruments
101	1	VR1	5.1 V, 5%, 250 mW, SOT23	BZX84C5V1LT1G	On Semi
102	1	VR2	Diode Zener 12 V 500 mW SOD123	MMSZ5242B-7-F	Diodes, Inc.
103	1	VR3	150 V, 400 W, SMA	SMAJ150A-13-F	Diodes, Inc.
104	4	WASHER1 WASHER2 WASHER3 WASHER4	WASHER FLAT #4 SS	FWSS 004	Building Fasteners

7 Magnetics

7.1 LLC Transformer (T1) Specification

7.1.1 *Electrical Diagram*

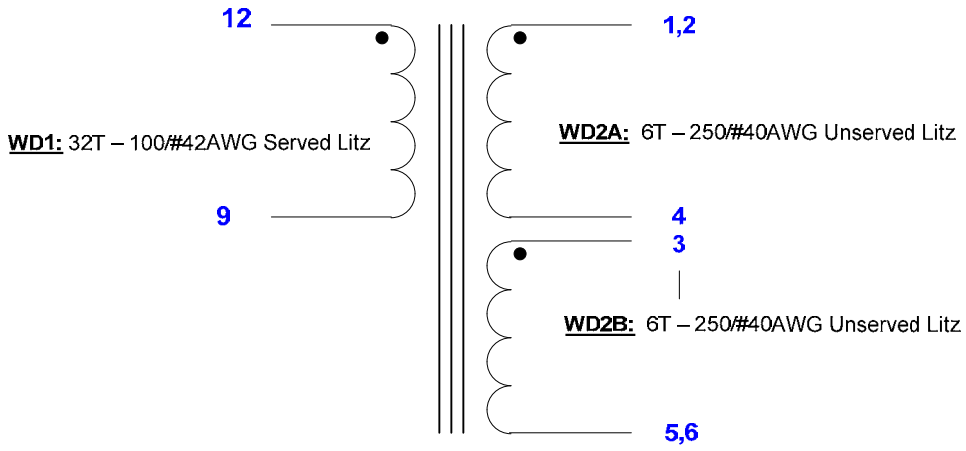

Figure 10 – LLC Transformer Schematic.

7.1.2 *Electrical Specifications*

Electrical Strength	1 second, 60 Hz, from pins 1-6 to pins 7-12.	3000 VAC
Primary Inductance	Pins 9-12, all other windings open, measured at 100 kHz, 0.4 $V_{RMS.}$	250 µH ±10%
Resonant Frequency	Pins 9-12, all other windings open.	2,400 kHz (Min)
Primary Leakage Inductance	Pins 9-12, with pins 1-6 shorted, measured at 100 kHz, 0.4 $V_{RMS.}$	67 µH ±5%

7.1.3 *Material List*

Item	Description
[1]	Core Pair ETD34: Ferroxcube 3F3 or equivalent, gap for A_{LG} of 244 nH/T^2.
[2]	Bobbin: Winshine WS-53404; PI#: 25-01048-00.
[3]	Bobbin Cover, Winshine WS-53404-1.
[4]	Litz wire: 250/#40 Single Coated, Unserved.
[5]	Litz wire: 100/#42 Single Coated, Served.
[6]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 6.0 mm wide.
[7]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 10.0 mm wide.
[8]	Varnish: Dolph BC-359, or equivalent.

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7.1.4 *Build Diagram*

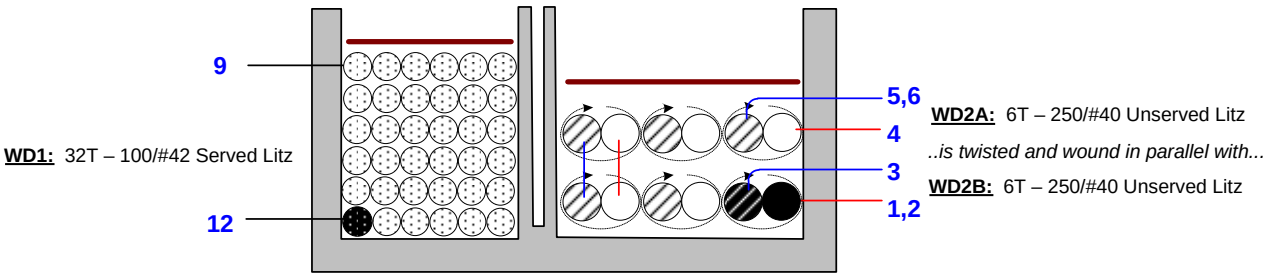
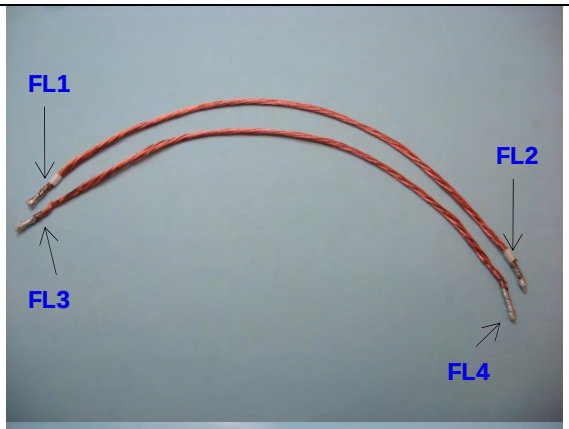
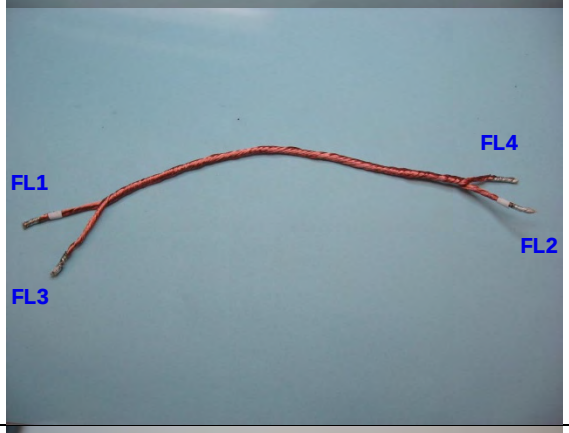
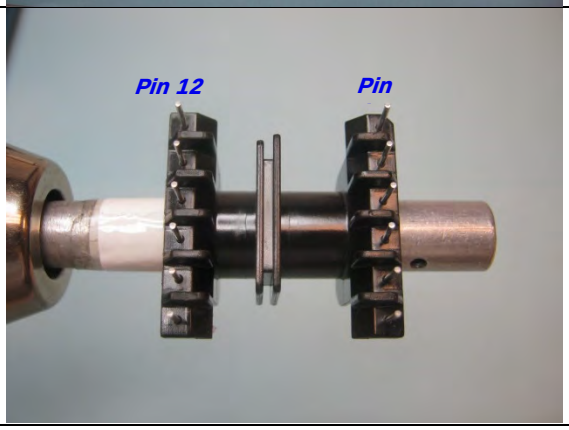


Figure 11 – LLC Transformer Build Diagram.

7.1.5 *Winding Instructions*

Secondary Wire Preparation	Prepare 2 strands of wire item [4] 14" length, tin ends. Label one strand to distinguish from other and designate it as FL1, FL2. Other strand will be designated as FL3 and FL4. Twist these 2 strands together ~20 twists evenly along length leaving 1" free at each end. See winding illustrations.
WD1 (Primary)	Place the bobbin item [2] on the mandrel with small chamber on the left side. Note: chamber used for primary winding is narrower than chamber used for secondary. Pins 7-12 will be on left side Starting on pin 12, wind 32 turns of served Litz wire item [5] in ~6 layers, and finish on pin 9. Secure this winding with 1 layer of tape item [6].
WD2A & WD2B (Secondary)	Using unserved Litz assembly prepared in step 1, start with FL1 on pins 1-2 and FL3 on pin 3, tightly wind 6 turns in secondary chamber. Finish with FL2 on pin 4 and FL4 on pins 5-6. Secure this winding with 1 layer of tape item [7].
Bobbin Cover	Slide bobbin cover [3] into grooves in bobbin flanges as shown. Make sure the cover is securely seated.
Finish	Remove pins 7 and 8 of bobbin. Grind core halves [1] for specified inductance. Assemble and secure core halves using circumferential turn of tape [6] as shown, Dip varnish [8].

7.1.6 *Winding Illustrations*

Secondary Wire Preparation	 	Prepare 2 strands of wire item [7] 12” length, tin ends. Label one strand to distinguish from other and designate it as FL1, FL2. Other strand will be designated as FL3 and FL4. Twist these 2 strands together ~20 twists evenly along length leaving 1” free at each end. See pictures below. Video 1.wmv
WD1 (Primary)		Place the bobbin item [2] on the mandrel with small chamber on the left side. Note: chamber used for primary winding is narrower than chamber used for secondary. Pins 7-12 will be on left side. Starting on pin 12, wind 32 turns of served Litz wire item [6] in ~ 6 layers, and finish on pin 9.

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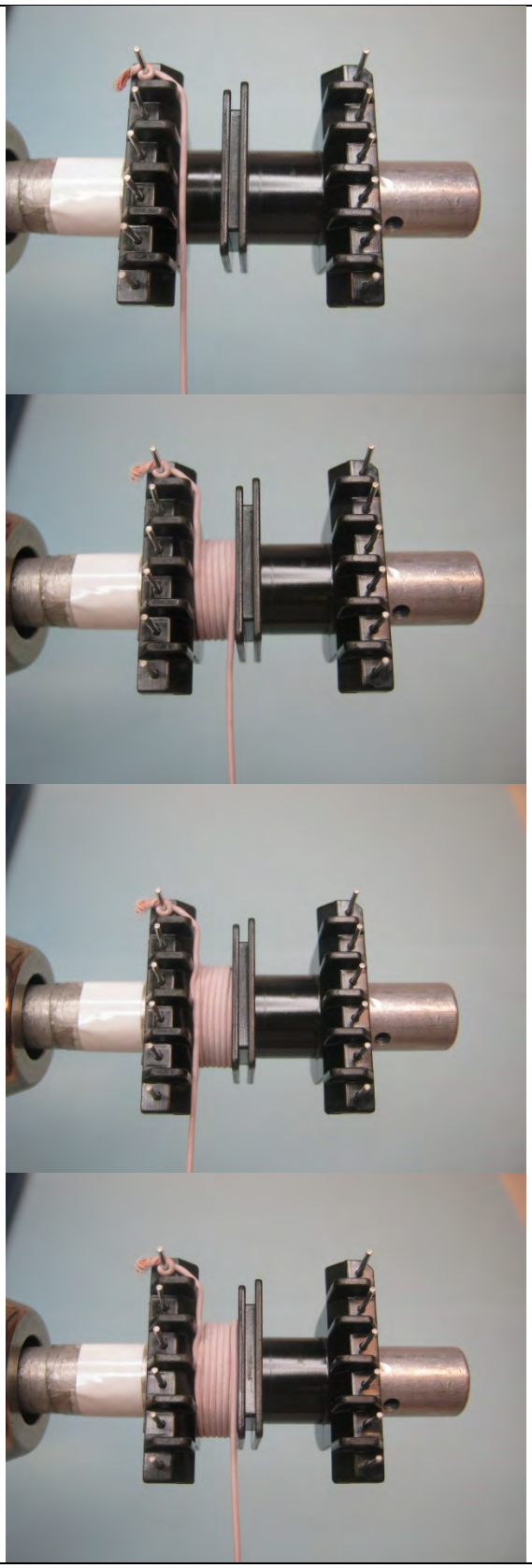
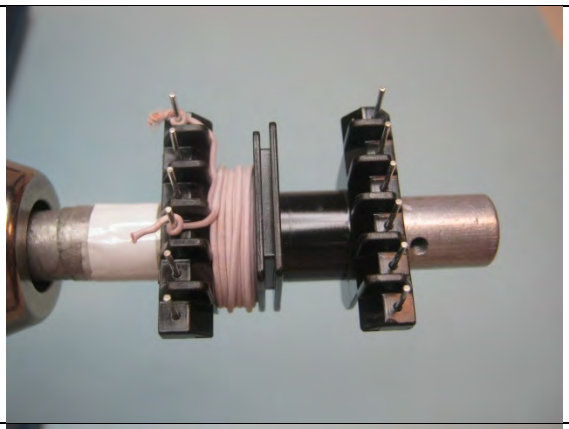
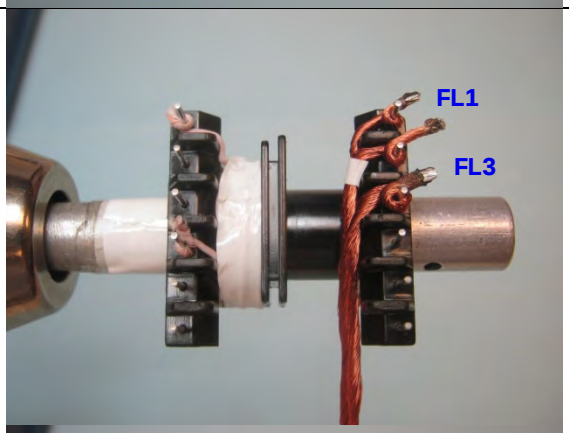
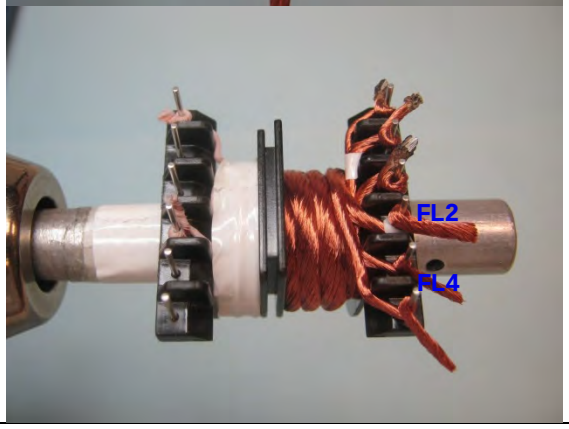


		
WD1 (Primary) (Cont'd)	  	Using unserved Litz assembly prepared in step 1, start with FL1 on pins 1-2 and FL3 on pin 3, tightly wind 6 turns in secondary chamber. Finish with FL2 on pin 4 and FL4 on pins 5-6. Secure this winding with 1 layer of tape item [7].

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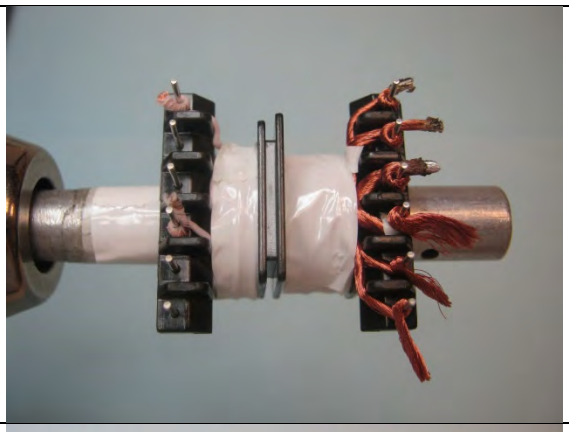
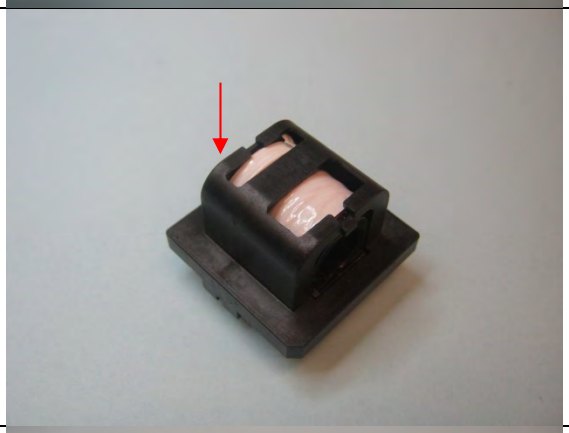
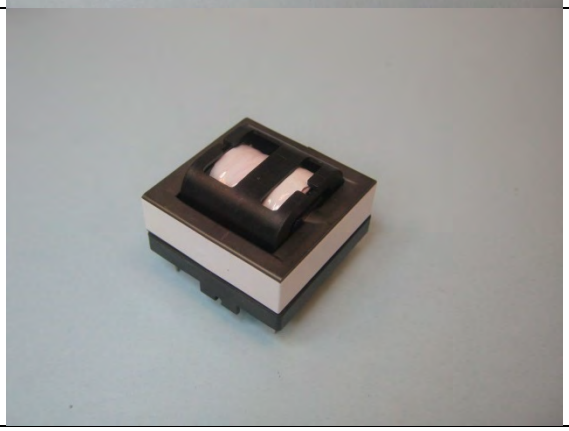
		
Bobbin Cover		Slide bobbin cover [3] into grooves in bobbin flanges as shown. Make sure cover is securely seated.
Finish		Remove pins 7 & 8 of bobbin. Grind core halves [1] for specified inductance. Assemble and secure core halves using circumferential turn of tape [6] as shown. Dip varnish [8].

7.2 Standby Transformer (T2) Specification

7.2.1 Electrical Diagram

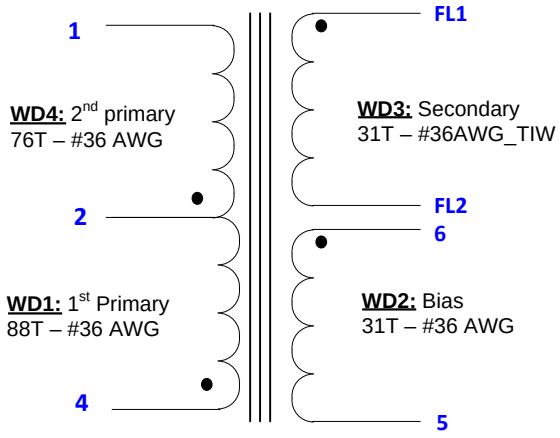


Figure 12 – Transformer Electrical Diagram.

7.2.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-4 to FL1-2.	3000 V
Primary Inductance	Pins 1-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	3.2 mH ±10%
Resonant Frequency	Pins 1-4, all other windings open.	600 kHz (Min.)
Primary Leakage Inductance	Pins 1-4, with pins 5-8, FL1, FL2 shorted, measured at 100 kHz, 0.4 V_{RMS}.	20 µH (Max.)

7.2.3 Material List

Item	Description
[1]	Core: EE10, TDK PC40 material, (PI#: 99-00037-00) or equivalent. gap for inductance coefficient (A_L) of 119 nH/T².
[2]	Bobbin, EE10, vertical, 8 Pins (4/4). TDK BE10-118CPSFR, Taiwan Shulin TF-10 (PI#: 25-00877-00) or equivalent.
[3]	Tape, Polyester film, 3M 1350F-1 or equivalent, 6.5 mm wide.
[4]	Wire, Magnet #36 AWG, solderable double coated.
[5]	Wire, Triple Insulated, Furukawa TEX-E or equivalent, #36 AWG.
[6]	Transformer Varnish, Dolph BC-359 or equivalent.

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7.2.4 *Build Diagram*

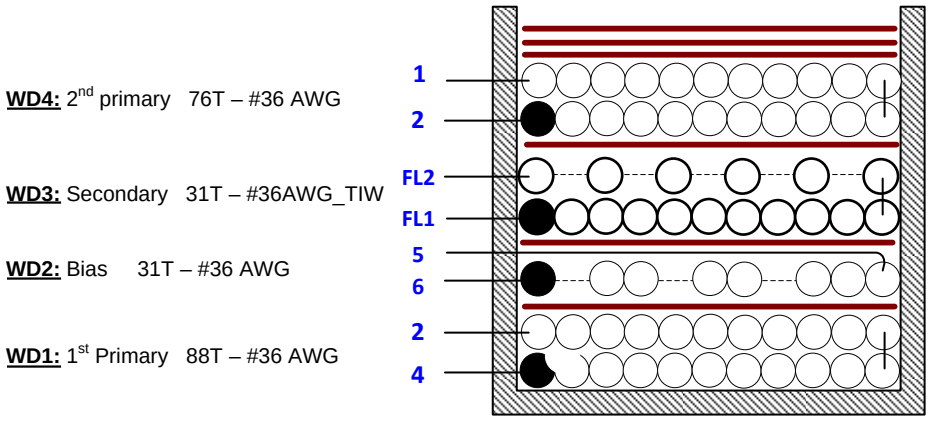
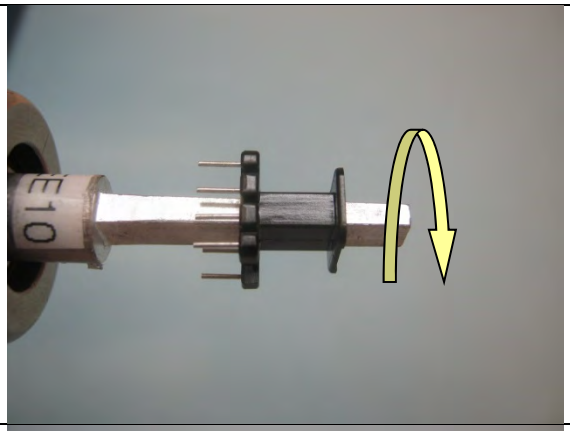
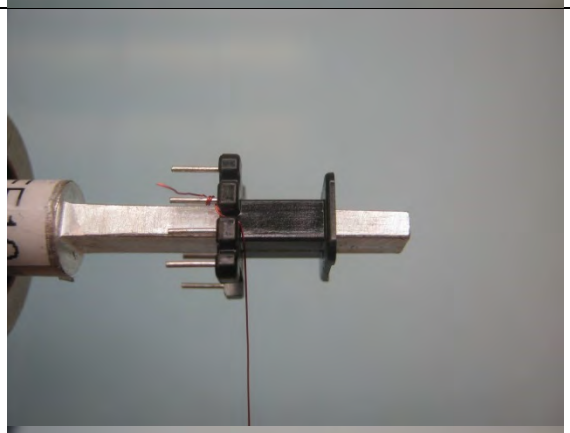
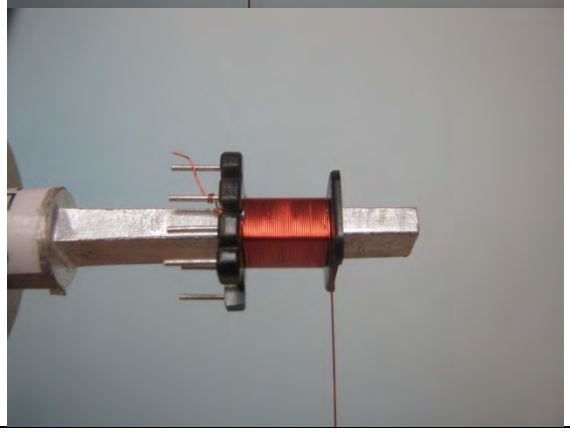


Figure 13 – Transformer Build Diagram.

7.2.5 *Winding Instructions*

General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side (see illustration). Winding direction as shown is clockwise.
WD1: 1st Primary	Starting at pin 4, wind 88 turns of wire item [4] in 2 layers. Finish at pin 2.
Insulation	Use 1 layer of tape item [3] for insulation.
WD2: Bias	Starting at pin 6, wind 31 turns of wire item [4] in one layer. Finish at pin 5.
Insulation	Use 1 layer of tape item [3] for insulation.
WD3: Secondary	Using wire items [5], leave ~1” floating, and mark as FL1 for start lead. Wind 31 turns and also leave ~1” for end lead and mark as FL2.
Insulation	Use 1 layer of tape item [3] for insulation.
WD4: 2nd Primary	Starting at pin 2, wind 76 turns of wire item [4] in ~2 layers. Finish at pin 1.
Insulation	Use 3 layers of tape item [3] to secure the windings.
Assembly	Grind core halves for specified primary inductance, and secure core halves with tape. Remove pins 3, 7, 8. Dip varnish item [6].

7.2.6 ***Transformer Illustrations***

General Note		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side (see illustration). Winding direction as shown is clockwise.
WD1: 1st Primary	 	Starting at pin 4, wind 88 turns of wire item [4] in 2 layers. Finish at pin 2.

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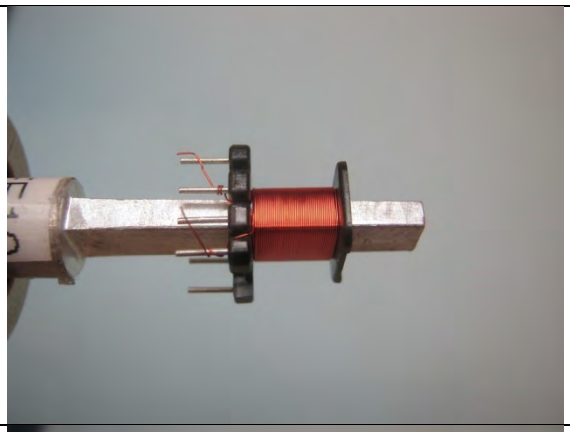
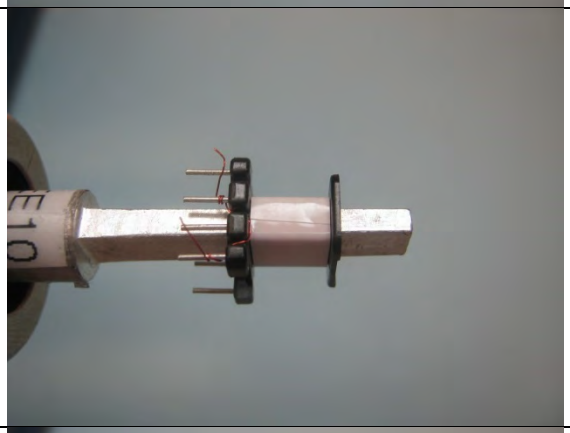
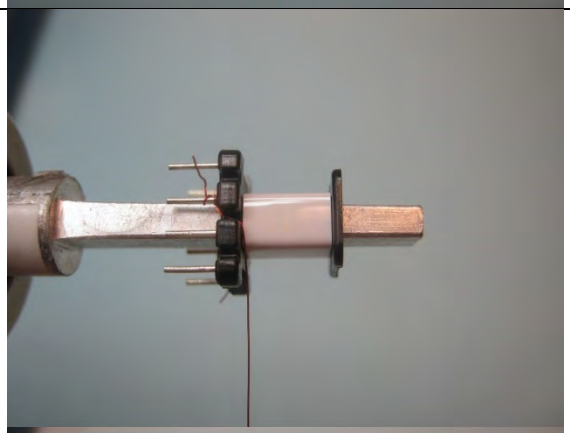
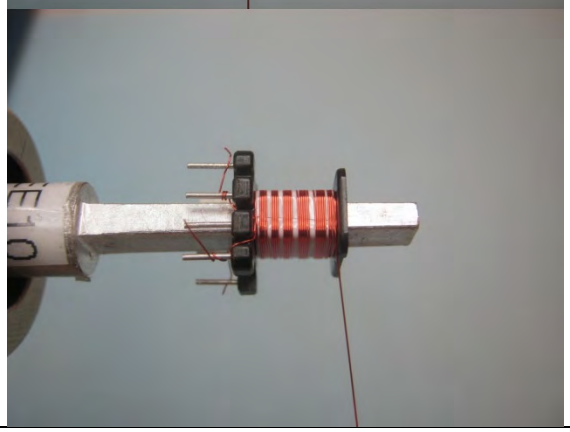
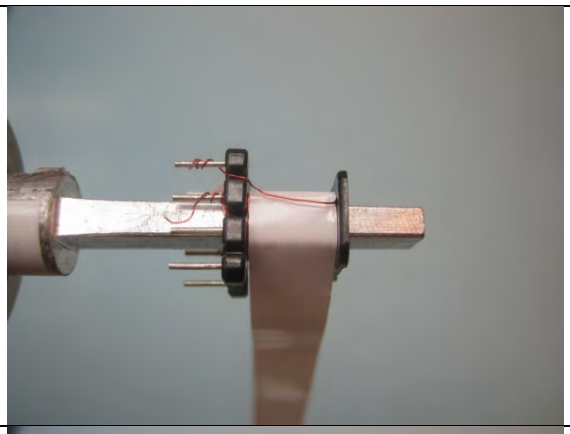
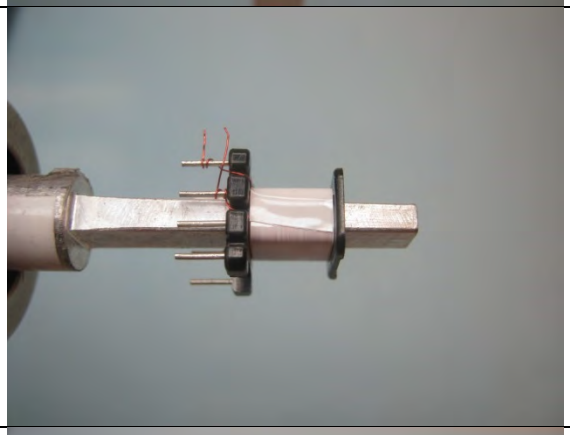
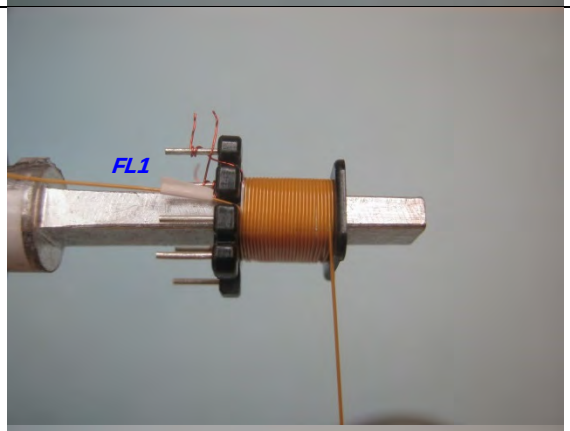
		
Insulation		Use 1 layer of tape item [3] for insulation.
WD2: Bias	 	Starting at pin 6, wind 31 turns of wire item [4] in one layer. Finish at pin 5.

		
Insulation		Use 1 layer of tape item [3] for insulation.
WD3: Secondary	 	Using wire items [5], leave ~ 1" floating, and mark as FL1 for start lead. Wind 31 turns and also leave ~1" for end lead and mark as FL2.

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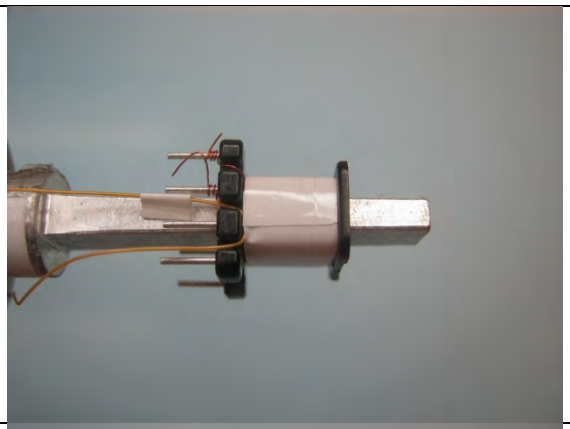
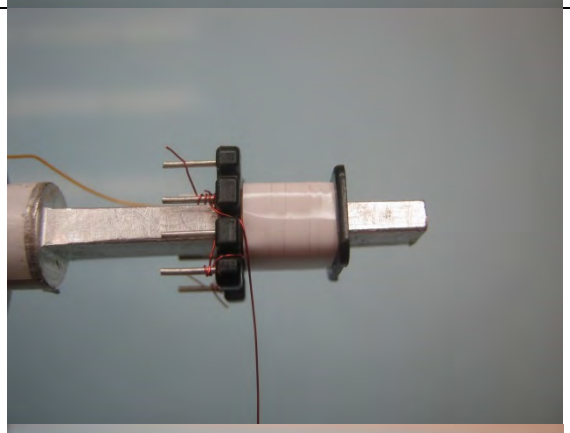
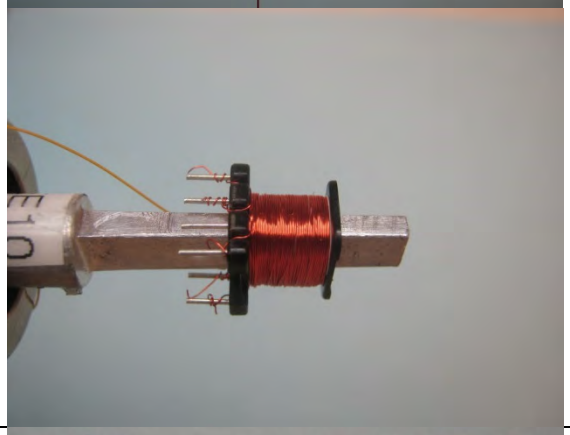
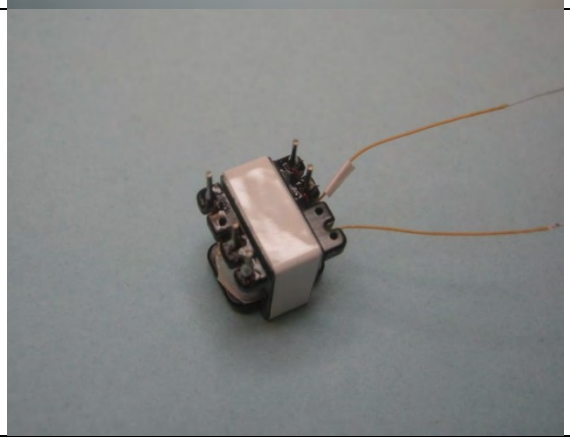
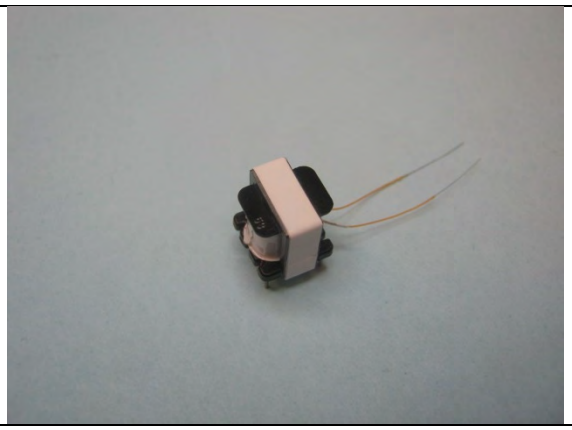
Insulation		Use 1 layer of tape item [3] for insulation.
WD4: 2nd Primary	 	Starting at pin 2, wind 76 turns of wire item [4] in ~2 layers. Finish at pin 1.
Assembly		Grind core halves for specified primary inductance, and secure core halves with tape. Remove pins 3, 7, 8. Dip varnish item [6].

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8 LLC Transformer Design Spreadsheet

HiperLCS_042413; Rev.1.3; Copyright Power Integrations 2013	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_042413_Rev1-3.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					
Vbulk_nom	220		220	V	Nominal LLC input voltage
Vbrownout			162	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
Vbrownin			204	V	Startup threshold on bulk capacitor
VOV_shut			269	V	OV protection on bulk voltage
VOV_restart			259	V	Restart voltage after OV protection.
CBULK	280.00	Warning	280	uF	!!! Warning. CBULK is too small. Recommended value should be greater than 0.7 uF/W
tHOLDUP			15.9	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs					**The spreadsheet assumes AC stacking of the secondaries**
VO1	23.00		23.0	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	8.00		8.0	A	Main output maximum current
VD1			0.50	V	Forward voltage of diode in Main output
PO1			184	W	Output Power from first LLC output
VO2			0.0	V	Second Output Voltage
IO2			0.0	A	Second output current
VD2			0.70	V	Forward voltage of diode used in second output
PO2			0.00	W	Output Power from second LLC output
P_LLC			184	W	Specified LLC output power
LCS Device Selection					
Device	**LCS705**	Warning	**LCS705**		!!! Warning. Device may be too large. Select smaller device
RDS-ON (MAX)			0.74	ohms	RDS-ON (max) of selected device
Coss			468	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
Pcond_loss			3.5	W	Conduction loss at nominal line and full load
Tmax-hs			90	deg C	Maximum heatsink temperature
Theta J-HS			8.4	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			120	deg C	Expectd Junction temperature
Ta max	80.00		80	deg C	Expected max ambient temperature
Theta HS-A			3	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)					
Vres_target	220.00		220	V	Desired Input voltage at which power train operates at resonance. If greater than Vbulk_nom, LLC operates below resonance at VBULK.
Po			188	W	LLC output power including diode loss
Vo			23.50	V	Main Output voltage (includes diode drop) for calculating Nsec and turns ratio
f_target	100.00		100	kHz	Desired switching frequency at Vbulk_nom. 66 kHz to 300 kHz, recommended 180-250 kHz
Lpar			183	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri	250.00		250	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for slight loss of ZVS at ~80% of Vnom
Lres	67.00		67.0	uH	Series inductance or primary leakage inductance of

					integrated transformer; if left blank auto-calculation is for K=4
Kratio			2.7		Ratio of Lpar to Lres. Maintain value of K such that 2.1 < K < 11. Preferred Lres is such that K<7.
Cres	33.00		33.0	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec			8.789	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
m			50	%	Leakage distribution factor (primary to secondary). >50% signifies most of the leakage is in primary side. Gap physically under secondary yields >50%, requiring fewer primary turns.
n_eq			4.56		Turns ratio of LLC equivalent circuit ideal transformer
Npri	32.0		32.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target and m=50%
Nsec	6.0		6.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=200 mT, using selected core (below)
f_predicted			107	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_eq and primary turns
f_res			107	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout			83	kHz	Expected switching frequency at Vbrownout, full load. Set HiperLCS minimum frequency to this value.
f_par			55	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion			81	kHz	LLC full load gain inversion frequency. Operation below this frequency results in operation in gain inversion region.
Vinversion			157	V	LLC full load gain inversion point input voltage
Vres_expected			214	V	Expected value of input voltage at which LLC operates at resonance.
RMS Currents and Voltages					
IRMS_LLC_Primary			2.19	A	Primary winding RMS current at full load, Vbulk_nom and f_predicted
Winding 1 (Lower secondary Voltage) RMS current			6.2	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current			3.7	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			0.0	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms			98	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)					
New primary turns			32.0		Trial transformer primary turns; default value is from resonant section
New secondary turns			6.0		Trial transformer secondary turns; default value is from resonant section
New Lpri			250	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres			33.0	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res same as in main resonant section above
New estimated Lres			67.0	uH	Trial transformer estimated Lres

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New estimated Lpar			183	uH	Estimated value of Lpar for trial transformer
New estimated Lsec			8.789	uH	Estimated value of secondary leakage inductance
New Kratio			2.7		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio			4.56		Estimated effective transformer turns ratio
V powertrain inversion new			157	V	Input voltage at LLC full load gain inversion point
f_res_trial			107	kHz	New Series resonant frequency
f_predicted_trial			107	kHz	New nominal operating frequency
IRMS_LLC_Primary			2.19	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current			6.4	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Lower Secondary Voltage Capacitor RMS current			4.1	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			6.4	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Vres_expected_trial			214	V	Expected value of input voltage at which LLC operates at resonance.
Transformer Core Calculations (Calculates From Resonant Parameter Section)					
Transformer Core	**Auto**		**EER28L**		**Transformer Core**
Ae	0.97		0.97	cm^2	Enter transformer core cross-sectional area
Ve	7.63		7.63	cm^3	Enter the volume of core
Aw	120.00		120.0	mm^2	Area of window
Bw	20.90		20.9	mm	Total Width of Bobbin
Loss density			200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT			4.0	cm	Mean length per turn
Nchambers			2		Number of Bobbin chambers
Wsep			3.0	mm	Winding separator distance (will result in loss of winding area)
Ploss			1.5	W	Estimated core loss
Bpkfmin			122	mT	First Quadrant peak flux density at minimum frequency.
BAC			188	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
Primary Winding					
Npri			32.0		Number of primary turns; determined in LLC resonant section
Primary gauge	42		42	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge			0.060	mm	Equivalent diameter of wire in metric units
Primary litz strands	100		100		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor			50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P			51	mm^2	Winding window area for primary
Fill Factor			29%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary			59.29	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C			74.98	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C			100.48	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current			2.19	A	Measured RMS current through the primary winding
ACR_Trf_Primary			122.81	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss			0.59	W	Total primary winding copper loss at 85 C

Primary Layers			2.78		Number of layers in primary Winding
Secondary Winding 1 (Lower secondary voltage OR Single output)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			23.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns			6.00		Secondary winding turns (each phase)
Sec 1 RMS current (total, AC+DC)			6.2	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Winding current (DC component)			4.00	A	DC component of winding current
Winding current (AC RMS component)			4.78	A	AC component of winding current
Sec 1 Wire gauge	40		40	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	250		250		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1			14.92	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1			3.54	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1			4.74	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.61	W	Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1			4.80	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1			0.22	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses			0.83	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current			3.7	A	Output capacitor RMS current
Co1	634.00		634.0	uF	Secondary 1 output capacitor
Capacitor ripple voltage			0.1	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			6.2	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 1 Layers			1.10		Number of layers in secondary 1 Winding
Secondary Winding 2 (Higher secondary voltage)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			0.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns			0.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)			6.2	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)			0.0	A	DC component of winding current
Winding current (AC RMS component)			0.0	A	AC component of winding current
Sec 2 Wire gauge			40	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands			0		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec2			37290.65	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT			3.95	cm	Mean length per turn
DCR_25C_Sec2			0.00	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2			0.00	m-ohm	Estimated resistance per phase at 100 C

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					(approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2			0.00	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2			0.00	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses			0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Capacitor RMS current			0.0	A	Output capacitor RMS current
Co2			N/A	uF	Secondary 2 output capacitor
Capacitor ripple voltage			N/A	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			0.0	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 2 Layers			1.00		Number of layers in secondary 2 Winding
Transformer Loss Calculations					**Does not include fringing flux loss from gap**
Primary copper loss (from Primary section)			0.59	W	Total primary winding copper loss at 85 C
Secondary copper Loss			0.83	W	Total copper loss in secondary winding
Transformer total copper loss			1.41	W	Total copper loss in transformer (primary + secondary)
AW_S			51.39	mm^2	Area of window for secondary winding
Secondary Fill Factor			49%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz
Signal Pins Resistor Values					
f_min			83	kHz	Minimum frequency when optocoupler is cut-off. Only change this variable based on actual bench measurements
Dead Time	500		500	ns	Dead time
Burst Mode	**1**		**1**		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max			542	kHz	Max internal clock frequency, dependent on dead-time setting. Is also start-up frequency
f_burst_start			236	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop			270	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor			11.78	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor			224	k-ohms	Resistor from DT/BF pin to G pin
Rstart			10.24	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup. Use default value unless additional start-up delay is desired.
Start up delay			0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin			92.1	k-ohms	Resistor from VREF pin to FB pin, to set min operating frequency; This resistor plus Rstart determine f_MIN. Includes 7% HiperLCS frequency tolerance to ensure f_min is below f_brownout
C_softstart			0.33	uF	Softstart capacitor. Recommended values are between 0.1 uF and 0.47 uF
Ropto			1.9	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor	10.50		10.5	k-ohm	!!! Warning. OV/UV resistor must be between 18 and 25 k-ohms. Too low value results in increased standby losses; Too large value can affect accuracy

					if OV/UV function
OV/UV pin upper resistor			0.88	M-ohm	Total upper resistance in OV/UV pin divider
LLC Capacitive Divider Current Sense Circuit					
Slow current limit	6.80		6.80	A	8-cycle current limit - check positive half-cycles during brownout and startup
Fast current limit			12.24	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor			47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor			51.7	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor			220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor			1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency			724	kHz	This pole attenuates IS pin signal
Loss Budget					
LCS device Conduction loss			3.5	W	Conduction loss at nominal line and full load
Output diode Loss			4.0	W	Estimated diode losses
Transformer estimated total copper loss			1.41	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss			1.5	W	Estimated core loss
Total transformer losses			2.9	W	Total transformer losses
Total estimated losses			10.5	W	Total losses in LLC stage
Estimated Efficiency			95%	%	Estimated efficiency
PIN			194	W	LLC input power
Secondary Turns and Voltage Centering Calculator					**This is to help you choose the secondary turns - Outputs not connected to any other part of spreadsheet**
V1			23.00	V	Target regulated output voltage Vo1. Change to see effect on slave output
V1d1			0.50	V	Diode drop voltage for Vo1
N1			7.00		Total number of turns for Vo1
V1_Actaul			23.00	V	Expected output
V2			0.00	V	Target output voltage Vo2
V2d2			0.70	V	Diode drop voltage for Vo2
N2			1.00		Total number of turns for Vo2
V2_Actual			2.66	V	Expected output voltage
Separate Series Inductor (For Non-Integrated Transformer Only)					**Not applicable if using integrated magnetics - not connected to any other part of spreadsheet**
Lsep			67.00	uH	Desired inductance of separate inductor
Ae_Ind			0.53	cm^2	Inductor core cross-sectional area
Inductor turns			29		Number of primary turns
BP_fnom			144	mT	AC flux for core loss calculations (at f_predicted and full load)
Expected peak primary current			6.8	A	Expected peak primary current
BP_fmin			299	mT	Peak flux density, calculated at minimum frequency fmin
Inductor Litz gauge			40	AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Inductor litz strands			125.00		Number of strands used in Litz wire
Inductor parallel wires			1		Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Sep_Ind			29.8	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT			7.00	cm	Mean length per turn
Inductor DCR 25 C			60.6	m-ohm	Estimated resistance at 25 C (for reference)

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Inductor DCR 100 C			81.2	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor			129.8	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss			0.62	W	Total primary winding copper loss at 85 C
Feedback section					
VMAIN	**Auto**		23.0		Output voltage rail that optocoupler LED is connected to
ITL431_BIAS			1.0	mA	Minimum operating current in TL431 cathode
VF			1.0	V	Typical Optocoupler LED forward voltage at IOPTO_BJTMAX (max current)
VCE_SAT			0.3	V	Optocoupler transistor saturation voltage
CTR_MIN			0.8		Optocoupler minimum CTR at VCE_SAT and at IOPTO_BJT_MAX
VTL431_SAT			2.5	V	TL431 minimum cathode voltage when saturated
RLED_SHUNT			1.0	k-ohms	Resistor across optocoupler LED to ensure minimum TL431 bias current is met
ROPTO_LOAD			4.70	k-ohms	Resistor from optocoupler emitter to ground, sets load current
IFMAX			222.13	uA	FB pin current when switching at FMAX (e.g. startup)
IOPTO_BJT_MAX			0.85	mA	Optocoupler transistor maximum current - when bursting at FMAX (e.g. startup)
RLED_SERIES_MAX			8.52	k-ohms	Maximum value of gain setting resistor, in series with optocoupler LED, to ensure optocoupler can deliver IOPTO_BJT_MAX. Includes -10% tolerance factor.

Note:

This transformer design was adjusted so the LLC converter will run above resonance over its entire operating range, in order to make the control loop easier to stabilize by avoiding the change in gain/phase characteristics that happens near resonance. This is accomplished by finding the minimum B+ voltage at 90 VAC (the bottom of the ripple waveform, using that voltage both as the nominal operating voltage and Vres

9 Standby Transformer Design Spreadsheet

ACDC_LinkSwitch-TN_Flyback_042413; Rev.1.10; Copyright Power Integrations 2007	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-TN Flyback_042413; Copyright Power Integrations 2007
ENTER APPLICATION VARIABLES					
VACMIN	180			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	60			Hertz	AC Mains Frequency
VO	12.00			Volts	Output Voltage (main) (For CC designs enter upper CV tolerance limit)
IO	0.09			Amps	Power Supply Output Current (For CC designs enter upper CC tolerance limit)
CC Threshold Voltage	0.00			Volts	Voltage drop across sense resistor.
Output Cable Resistance			0.17	Ohms	Enter the resistance of the output cable (if used)
PO			1.08	Watts	Output Power (VO x IO + CC dissipation)
Feedback Type	BIAS		Bias Winding		Choose 'BIAS' for Bias winding feedback and 'OPTO' for Optocoupler feedback from the 'Feedback Type' drop down box at the top of this spreadsheet
Add Bias Winding	YES		Yes		Choose 'YES' in the 'Bias Winding' drop down box at the top of this spreadsheet to add a Bias winding. Choose 'NO' to continue design without a Bias winding. Addition of Bias winding can lower no load consumption
n			0.6		Efficiency Estimate at output terminals.
Z			0.5		Loss Allocation Factor (suggest 0.5 for CC=0 V, 0.75 for CC=1 V)
tC	2.90			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	9.40			uFarads	Input Capacitance
Input Rectification Type	F		**F**		Choose H for Half Wave Rectifier and F for Full Wave Rectification from the 'Rectification' drop down box at the top of this spreadsheet
ENTER LinkSwitch-TN VARIABLES					
LinkSwitch-TN	**LNK302**		**LNK302**		User selection for LinkSwitch-TN. Ordering info - Suffix P/G indicates DIP 8 package; suffix D indicates SO8 package; second suffix N indicates lead free RoHS compliance
Chosen Device		LNK302			
ILIMITMIN			0.126	Amps	Minimum Current Limit
ILIMITMAX			0.146	Amps	Maximum Current Limit
fSmin			62000	Hertz	Minimum Device Switching Frequency
I^2fmin			984.312	A^2Hz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR			80	Volts	Reflected Output Voltage
VDS			10	Volts	LinkSwitch-TN on-state Drain to Source Voltage
VD			0.7	Volts	Output Winding Diode Forward Voltage Drop
KP			2.81		Ripple to Peak Current Ratio (0.6 < KP < 6.0).
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EE10**		**EE10**		User-Selected transformer core
Core		EE10		P/N:	PC40EE10-Z

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Bobbin		EE10_BOBBIN		P/N:	EE10_BOBBIN
AE	0.12		0.12	cm^2	Core Effective Cross Sectional Area
LE	2.61		2.61	cm	Core Effective Path Length
AL	850.00		850	nH/T^2	Ungapped Core Effective Inductance
BW	7.00		7	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4.00		4		Number of Primary Layers
NS	31		31		Number of Secondary Turns
NB	31		31		Number of Bias winding turns
VB			12.70	Volts	Bias Winding voltage
PIVB			59	Volts	Bias Diode Maximum Peak Inverse Voltage
DC INPUT VOLTAGE PARAMETERS					
VMIN			250	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.11		Maximum Duty Cycle
IAVG			0.01	Amps	Average Primary Current
IP			0.13	Amps	Minimum Peak Primary Current
IR			0.13	Amps	Primary Ripple Current
IRMS			0.02	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			3255	uHenries	Typical Primary Inductance. +/- 10%
LP_TOLERANCE			10	%	Primary inductance tolerance
NP			195		Primary Winding Number of Turns
ALG			85	nH/T^2	Gapped Core Effective Inductance
BM		**Info**	2028	Gauss	!!! Info. Flux densities above ~ 1500 Gauss may produce audible noise. Verify with dip varnished sample transformers. Increase NS to greater than or equal to 44 turns or increase VOR
BAC			1014	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1471		Relative Permeability of Ungapped Core
LG			0.16	mm	Gap Length (Lg > 0.1 mm)
BWE			28	mm	Effective Bobbin Width
OD			0.14	mm	Maximum Primary Wire Diameter including insulation
INS			0.03	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.11	mm	Bare conductor diameter
AWG			38	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			16	Cmils	Bare conductor effective area in circular mils
CMA		Info	651	Cmils/Amp	!!! Info. Can decrease CMA < 500 (decrease L(primary layers),increase NS,use smaller Core)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			0.79	Amps	Peak Secondary Current
ISRMS			0.27	Amps	Secondary RMS Current
IRIPPLE			0.25	Amps	Output Capacitor RMS Ripple Current
CMS			54	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			32	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.20	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.23	mm	Secondary Maximum Outside Diameter

					for Triple Insulated Wire
INSS			0.01	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			563	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			71	Volts	Output Rectifier Maximum Peak Inverse Voltage
FEEDBACK COMPONENTS					
Recommended Bias Diode			1N4003 - 1N4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI. See LinkSwitch-TN Design Guide
R1			#########	ohms	CV bias resistor for CV/CC circuit. See LinkSwitch-TN Design Guide
R2			3000	ohms	Resistor to set CC linearity for CV/CC circuit. See LinkSwitch-TN Design Guide
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			12.00	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			0.09	Amps	Output DC Current
PO1			1.08	Watts	Output Power
VD1			0.70	Volts	Output Diode Forward Voltage Drop
NS1			31.00		Output Winding Number of Turns
ISRMS1			0.27	Amps	Output Winding RMS Current
IRIPPLE1			0.25	Amps	Output Capacitor RMS Ripple Current
PIVS1			71.49	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			MUR110, UF4002, SB1100		Recommended Diodes for this output
Pre-Load Resistor			4	k-Ohms	Recommended value of pre-load resistor
CMS1			53.77	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			32.00	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.20	mm	Minimum Bare Conductor Diameter
ODS1			0.23	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2				Amps	Output DC Current
PO2			0.00	Watts	Output Power
VD2			0.70	Volts	Output Diode Forward Voltage Drop
NS2			1.71		Output Winding Number of Turns
ISRMS2			0.00	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			3.28	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS2			0.00	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3				Amps	Output DC Current
PO3			0.00	Watts	Output Power

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VD3			0.70	Volts	Output Diode Forward Voltage Drop
NS3			1.71		Output Winding Number of Turns
ISRMS3			0.00	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			3.28	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS3			0.00	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			1.08	Watts	Total Output Power
Negative Output	N/A		N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

10 Heat Sinks

10.1 Primary Heat Sink

10.1.1 *Primary Heat Sink Sheet Metal*

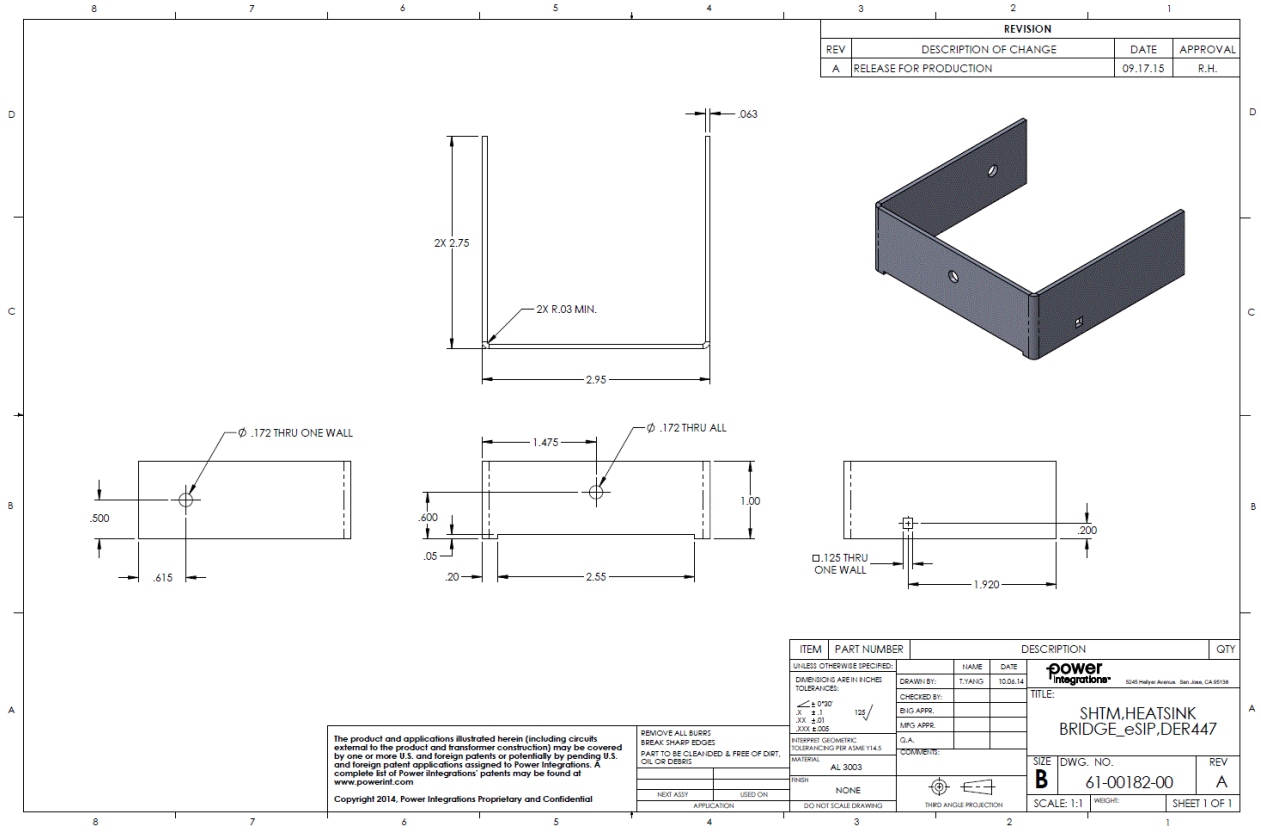

Figure 14 – Primary Heat Sink Sheet Metal Drawing.

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10.1.2 ***Primary Heat Sink with Fasteners***

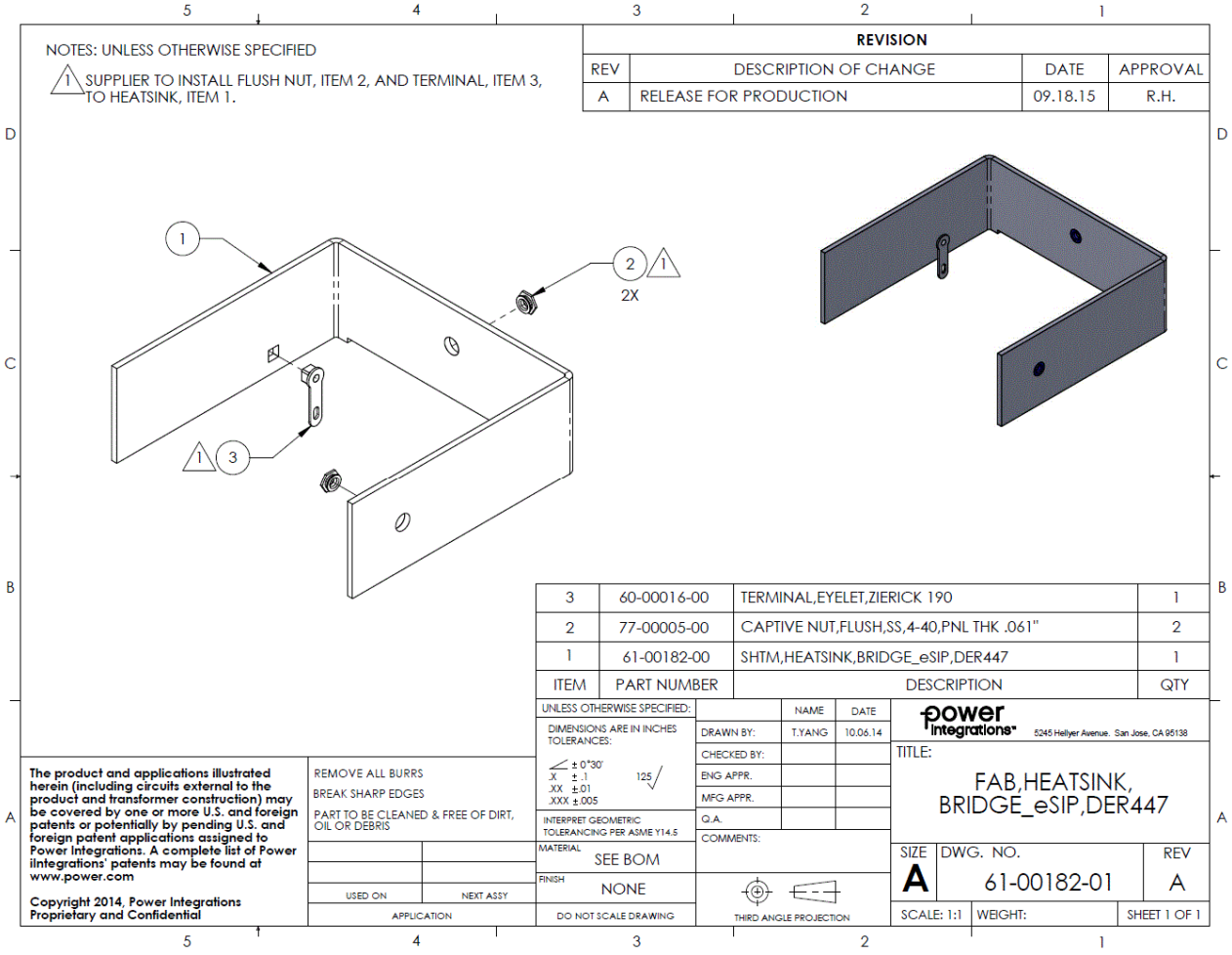

Figure 15 – Finished Primary Heat Sink Drawing with Installed Fasteners.

10.1.3 ***Primary Heat Sink Assembly***

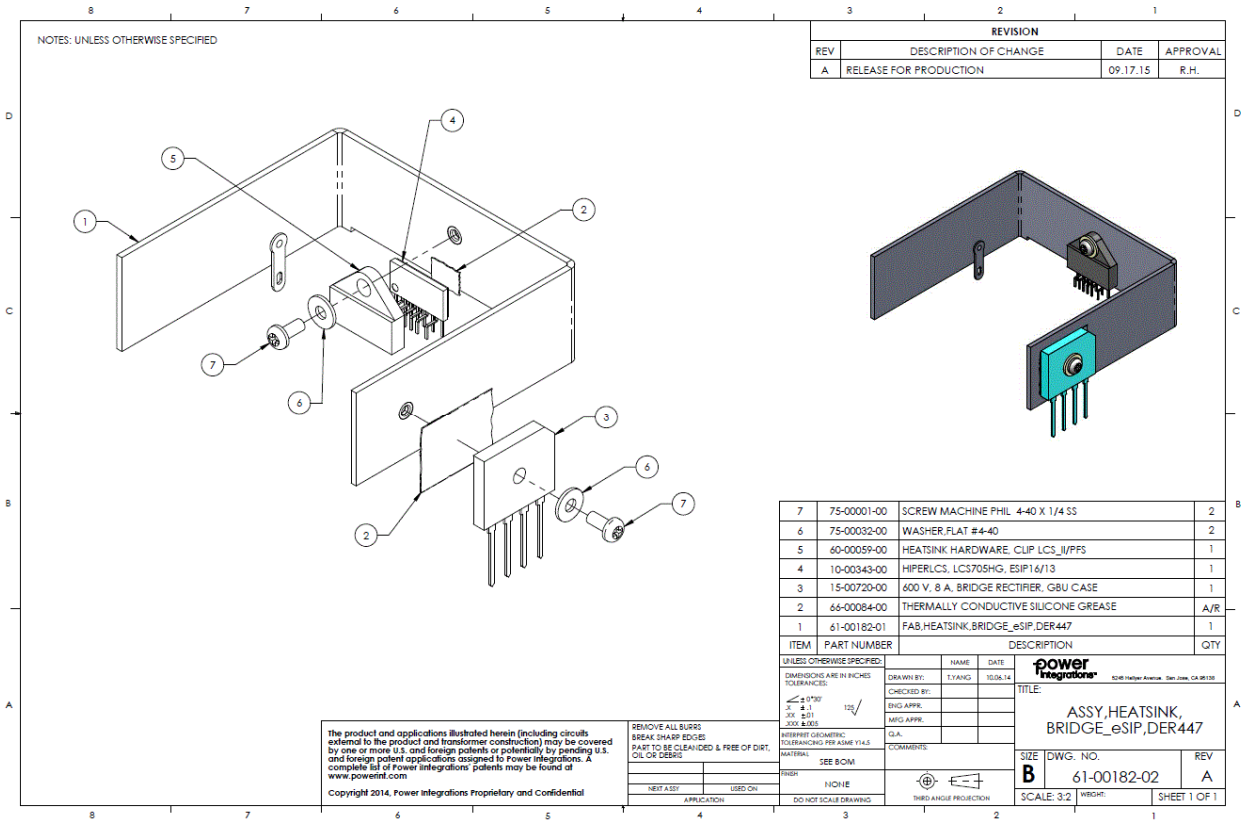

Figure 16 – Primary Heat Sink Assembly.

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10.2 Secondary Heat Sink

10.2.1 *Secondary Heat Sink Sheet Metal*

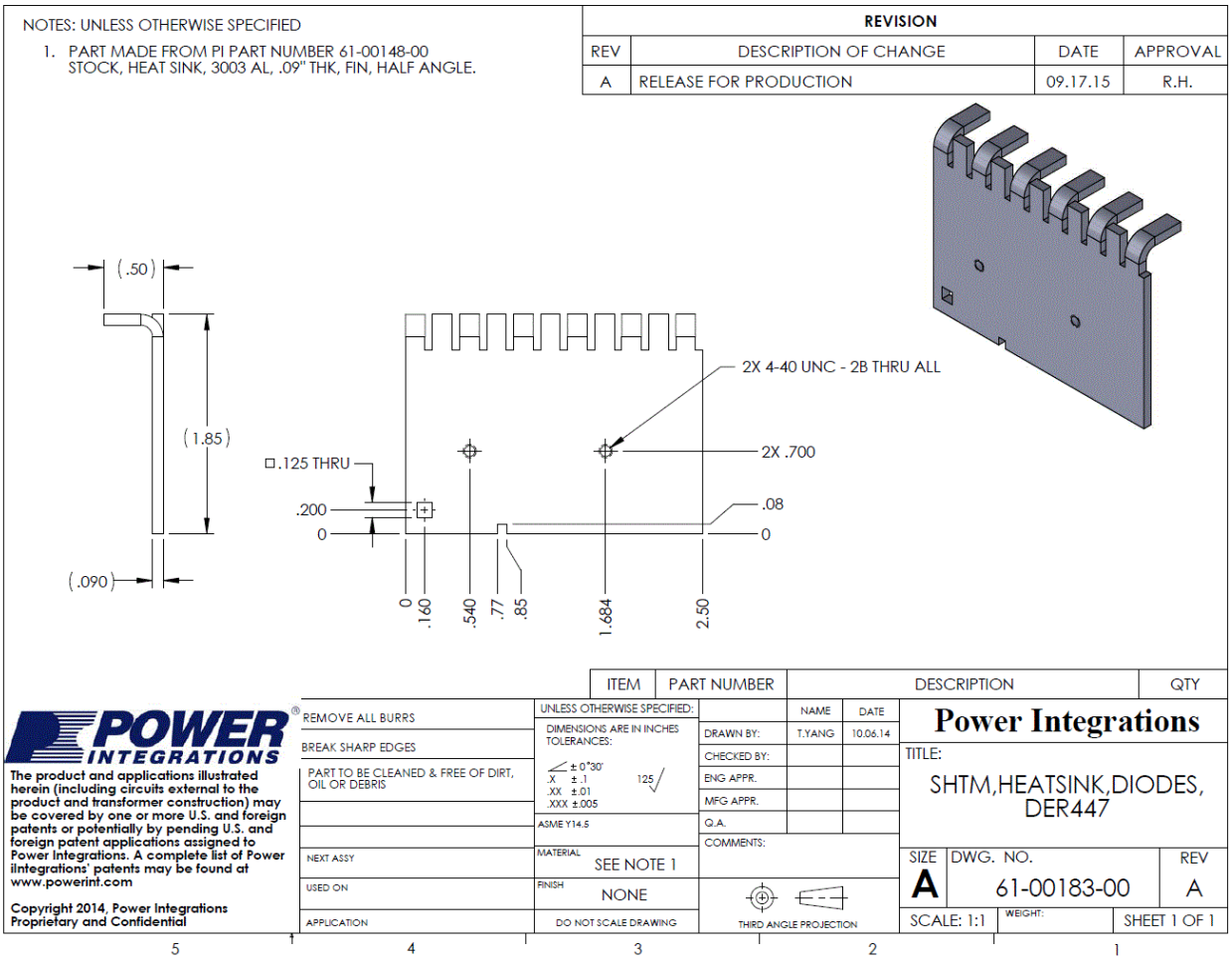

Figure 17 – Secondary Heat Sink Sheet Metal Drawing.

10.2.2 ***Secondary Heat Sink with Fasteners***

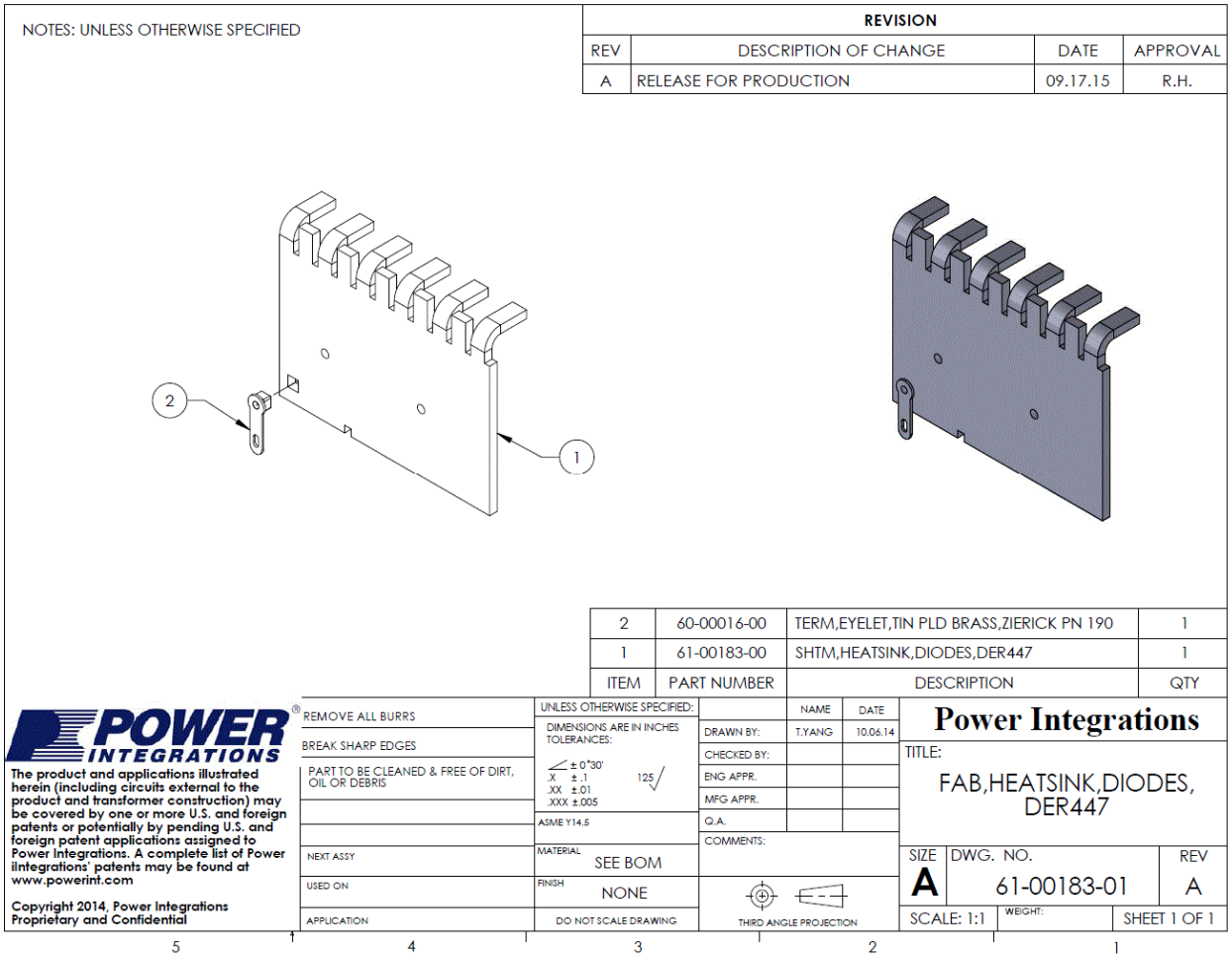

Figure 18 – Finished Secondary Heat Sink with Installed Fasteners.

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10.2.3 ***Secondary Heat Sink Assembly***

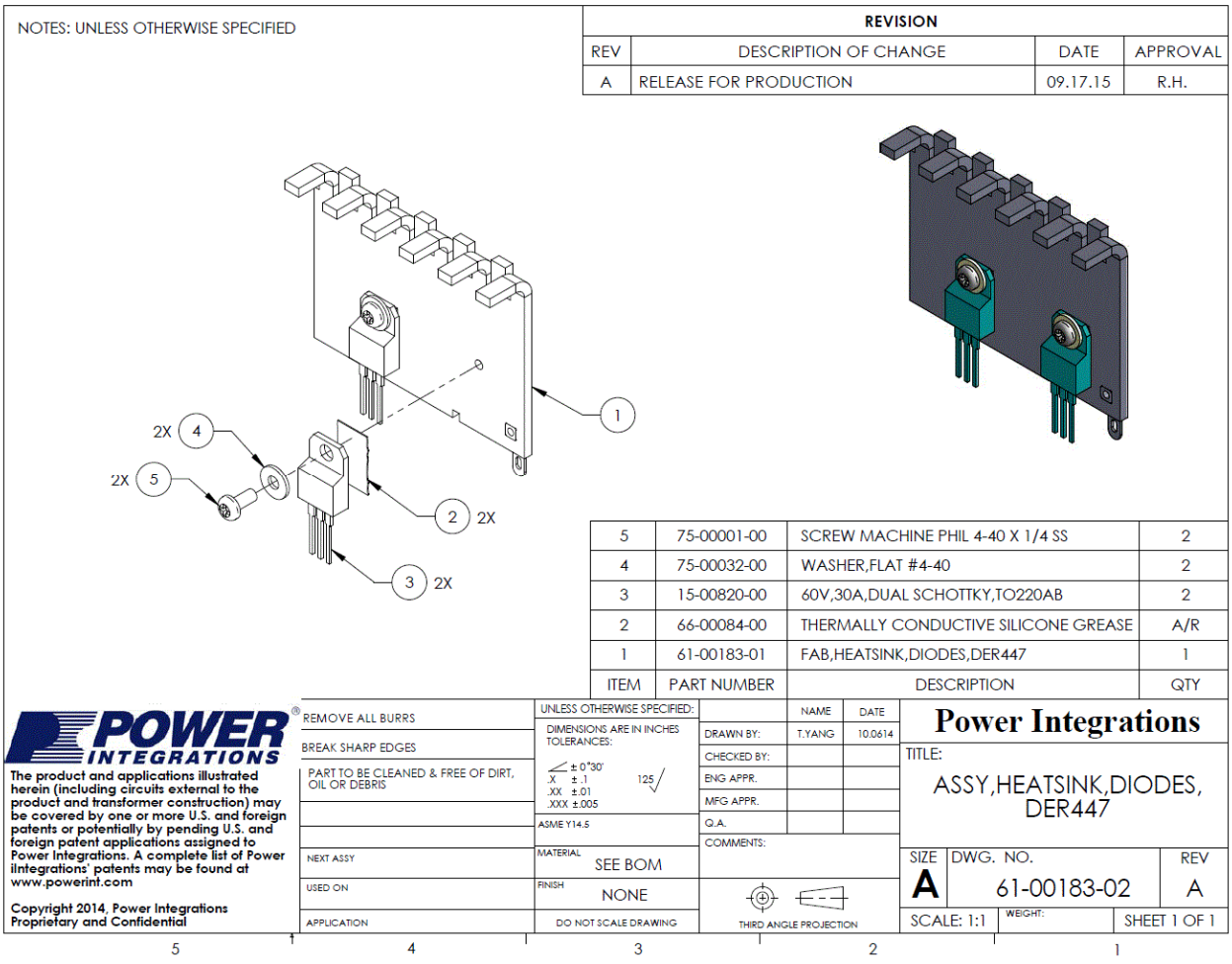

Figure 19 – Secondary Heat Sink Assembly.

11 Performance Data

All measurements were taken at room temperature and 60 Hz (input frequency) unless otherwise specified. Output voltage measurements were taken at the output connectors.

11.1 Output Load Considerations for Testing a CV/CC Supply in Battery Charger Applications

Since this power supply has a constant voltage/constant current output and normally operates in CC mode in its intended application (battery charging), some care must be taken in selecting the type/s of output load for testing.

The default setting for most electronic loads is constant current. This setting can be used in testing a CV/CC supply in the CV portion of its load range below the power supply current limit set point. Once the current limit of the DUT is reached, a constant current load will cause the output voltage of the DUT to immediately collapse to the minimum voltage capability of the electronic load.

To test a CV/CC supply in both its CV and CC regions (an example - obtaining a V-I characteristic curve that spans both the CV and CC regions of operation), an electronic load set for constant resistance can be used. However, in an application such as an LLC converter where the control loop is strongly affected by the output impedance, use of a CR load will give results for loop compensation that are overly optimistic and will likely oscillate when tested with an actual low impedance battery load, especially at low input voltage where the LLC converter is operating closest to resonance.
For final characterization and tuning the output control loops, a constant voltage load should be used.

Having said this, many electronic loads incorporate a constant voltage setting, but the output impedance of the load in this setting may not be sufficiently low to successfully emulate a real-world battery (impedance on the order of tens of milliohms). Simulating this impedance can be crucial in properly setting the compensation of the current control loop in order to prevent oscillation at low AC input voltage in a real-life application.

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11.2 Efficiency

To make this measurement, the supply was powered with an AC source. The figure shown includes the efficiency of the LLC stage combined with that of the standby/bias flyback supply.

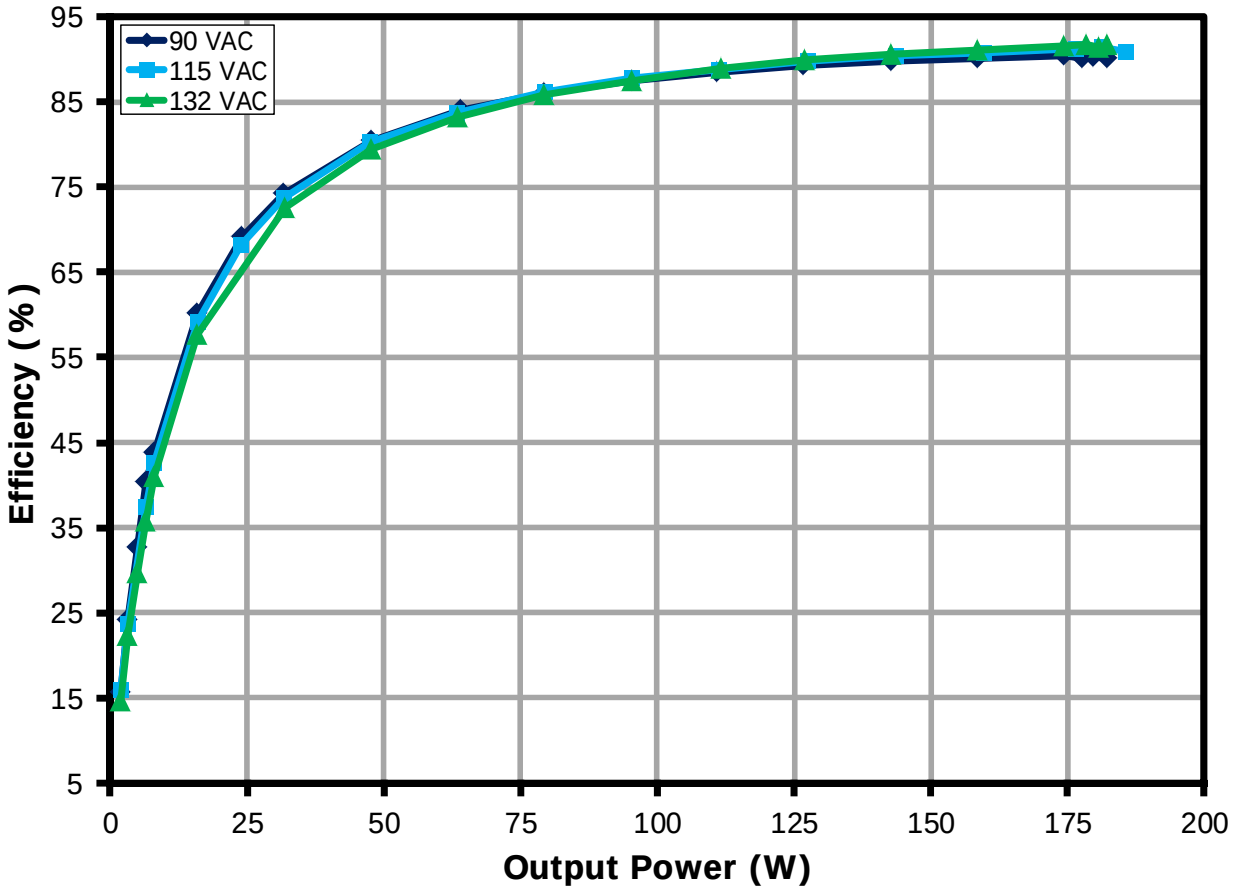

Figure 20 – Efficiency vs. Load, AC Input.

11.3 V-I Characteristic

The V-I characteristic showing the transition from constant voltage mode to constant current mode was measured using an electronic load set for constant resistance to allow proper operation of the DUT in both CV and CC mode. The measurements cut off a ~5 V, as this is the minimum load voltage attainable by the electronic load in CR mode.

11.3.1 *V-I Characteristic, Constant Resistance Load, I Limit = 8 A*

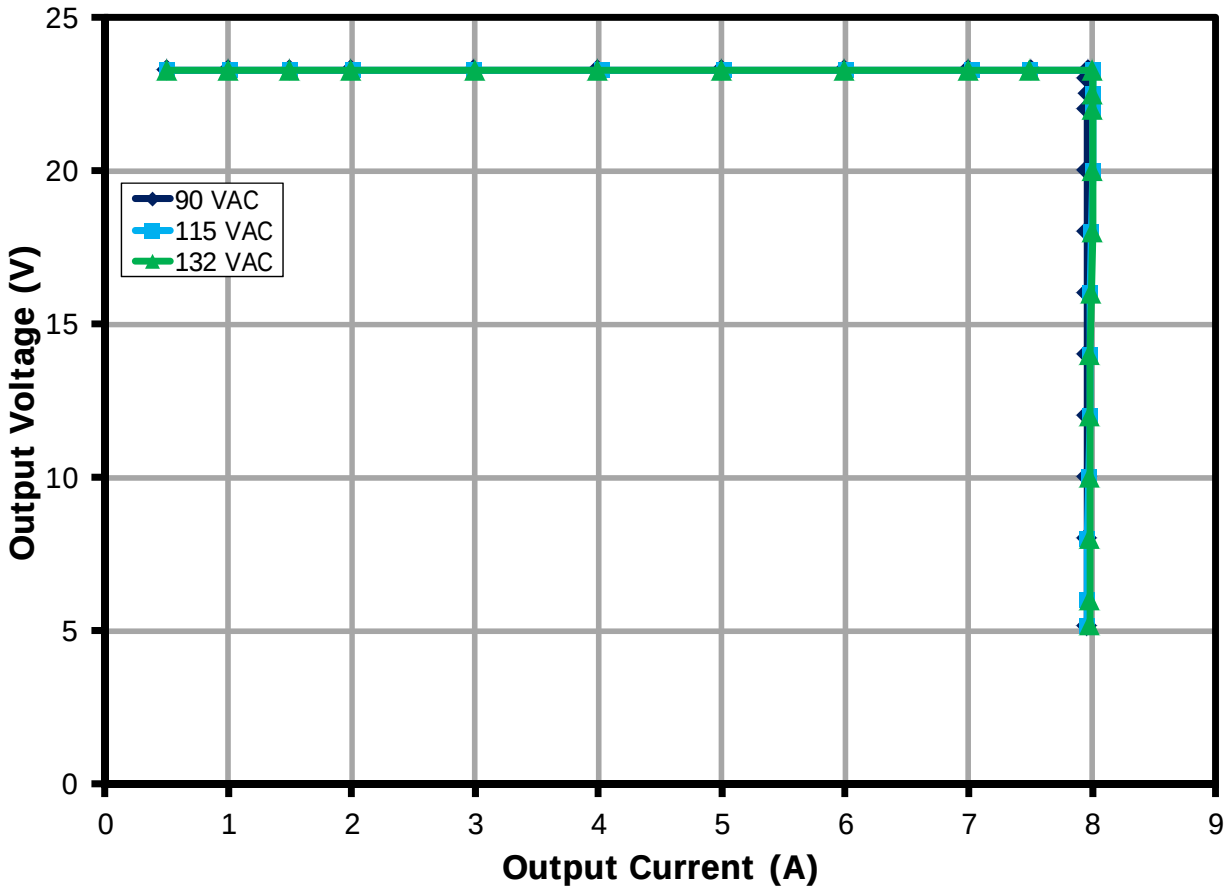

Figure 21 – V-I Characteristic with CR load, Ilim set for 8 A.

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11.3.2 *Output V-I Characteristic, Constant Voltage Load*

The V-I characteristic in constant current mode was measured using an electronic load set for constant voltage, as the electronic load used had a wider operating range in CV mode than in CR mode. In Figure 22, the output was set for a nominal default current limit value of 8 A. The output current was measured using a 1 milliohm shunt and Fluke 67 DVM, as the current readings were not steady on the metering of the electronic load. The actual reading was 7.9 A, which is within 1.25% of the nominal set point of 8 A.

The output current limit for the readings in Figure 23 was set to 0.5 A by placing a resistor in parallel with R32 in the current limit reference divider chain. The value of this resistor was tweaked to obtain an exact result. In a real world application, some variance of output current limit could be expected due to the extremely low value of reference voltage necessary for this current limit setting (7.5 mV), combined with variation in offset voltage for current limit sense amplifier U5A. Output current was measured using a Fluke 87 DVM, using its internal shunt.
Since the power supply is operating in burst mode, there can be some variance in the average output current as interpreted by the meter.

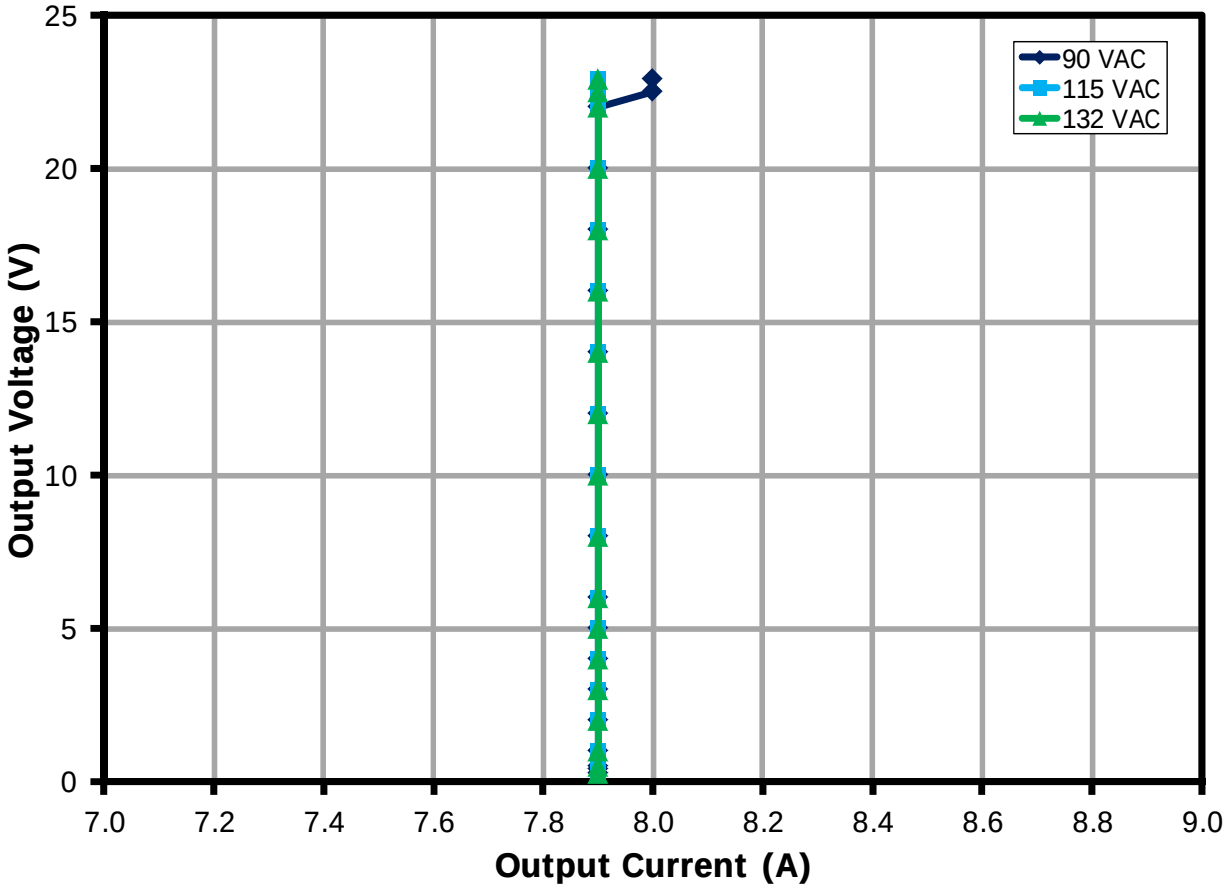

Figure 22 – V-I Characteristic with CV load, I_{LIM} Set for 8 A.

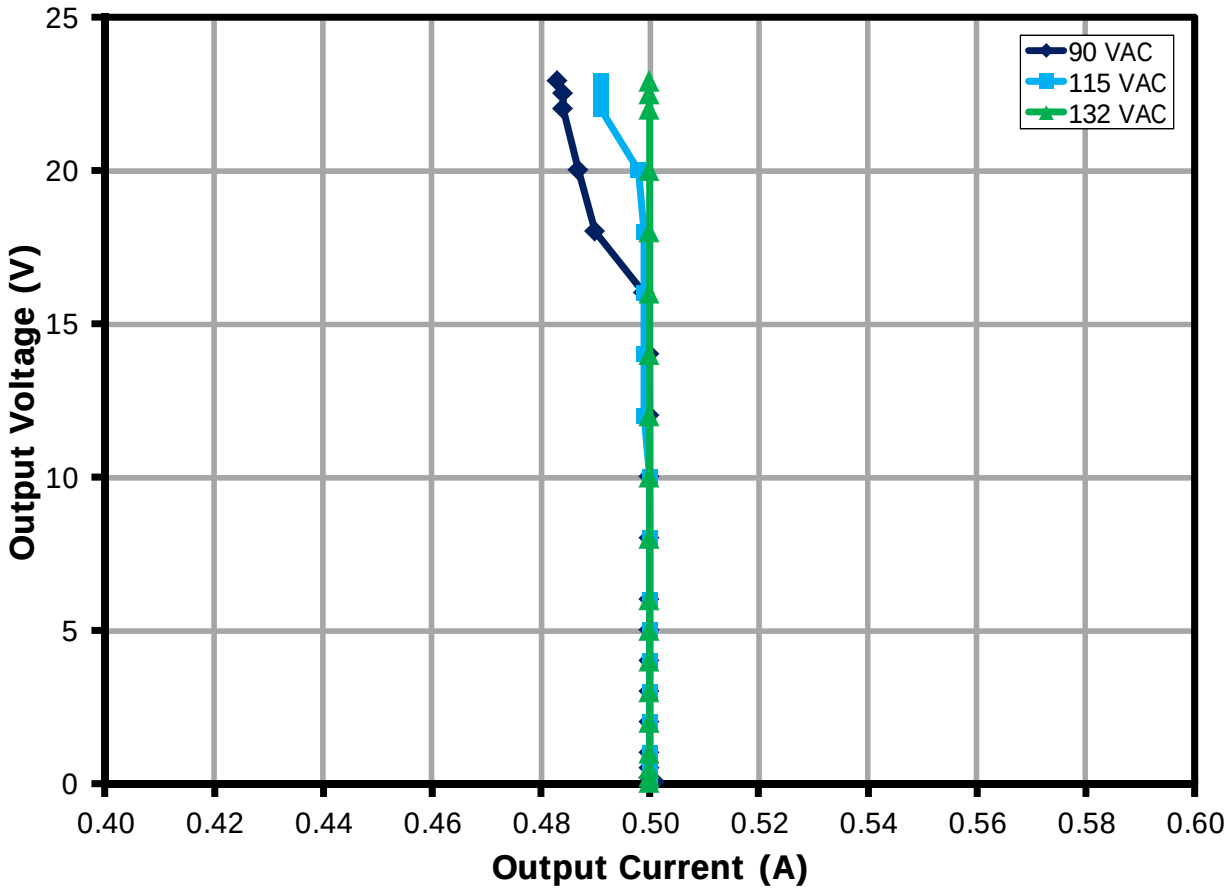

Figure 23 – V-I Characteristic with CV load, I_{LIM} Set for 0.5 A.

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12 Waveforms

12.1 LLC Primary Voltage and Current

12.1.1 *Results for 8 A Current Limit Setting*

The LLC stage current was measured by inserting a current sensing loop in series with the ground side of resonating capacitor C14 that measures the LLC transformer (T1) primary current. The output was loaded with an electronic load set for constant voltage, with the current limit of the supply under test at the nominal set point of 8 A. Waveforms were gathered for output voltages of 22.5 V, 16 V, and 8 V. The waveforms show the behavior of the supply in the upper portion of the constant current operation.

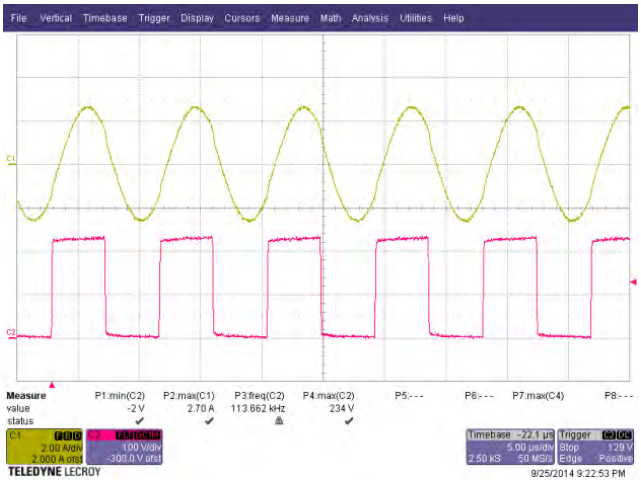

Figure 24 – LLC Stage Primary Voltage and Current, 90 VAC Input, CV Load, 8 A Current Limit, 22.5 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μs / div

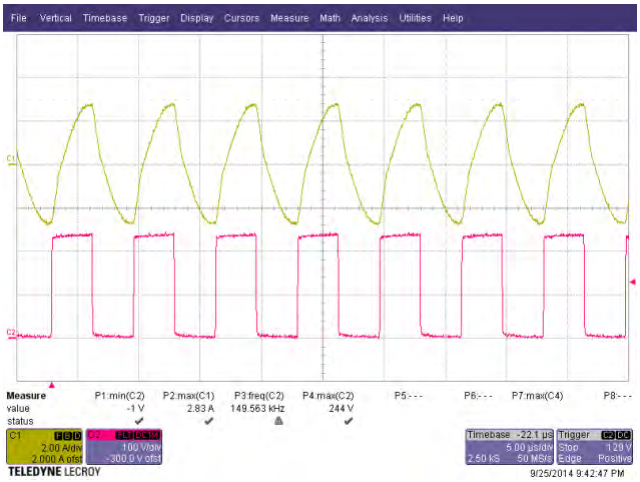

Figure 25 – LLC Stage Primary Voltage and Current, 90 VAC Input, CV Load, 8 A Current Limit, 16 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μs / div.

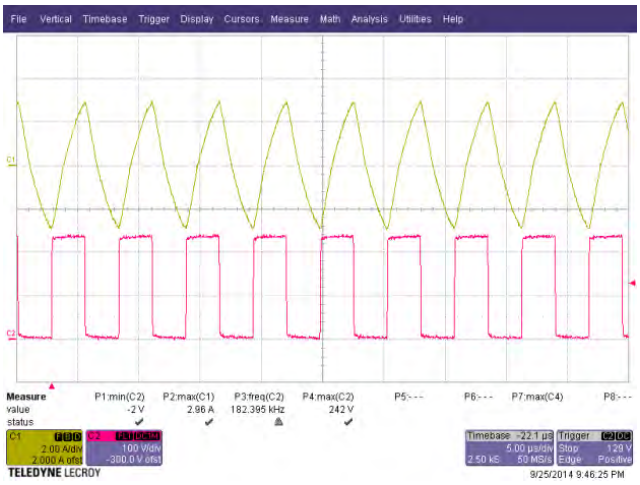

Figure 26 – LLC Stage Primary Voltage and Current, 90 VAC Input, CV Load, 8 A Current Limit, 8 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μs / div.

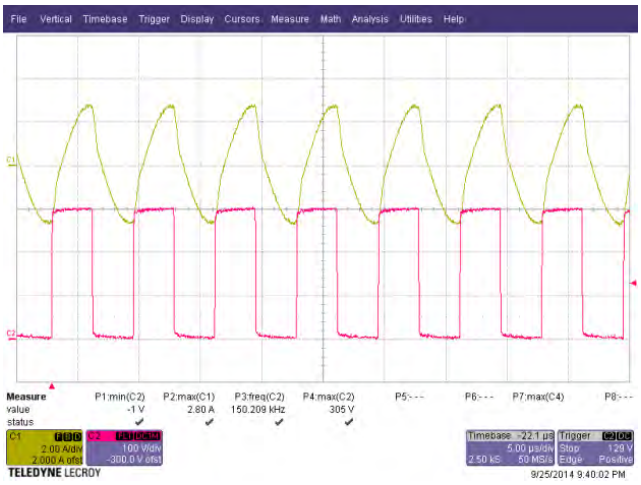

Figure 27 – LLC Stage Primary Voltage and Current, 115 VAC Input, CV Load, 8 A Current Limit, 22.5 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μs / div.

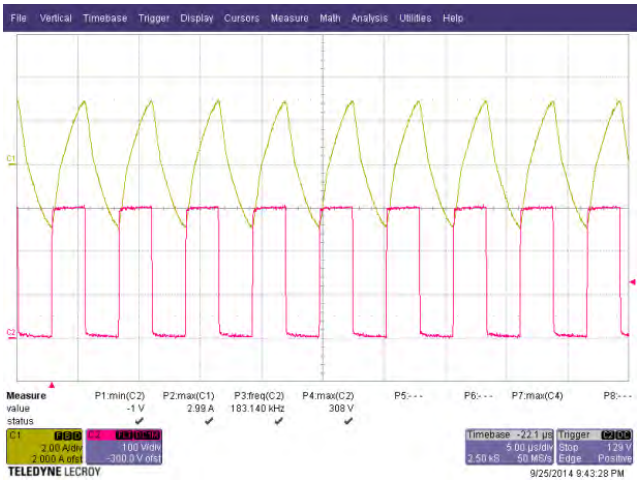

Figure 28 – LLC Stage Primary Voltage and Current, 115 VAC Input, CV Load, 8 A Current Limit, 16 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μs / div.

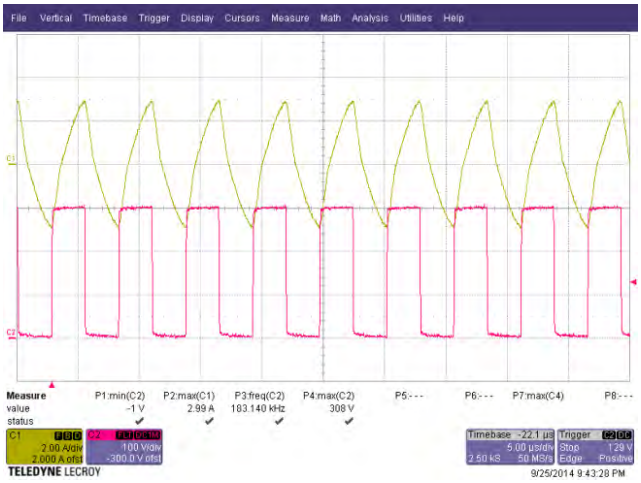

Figure 29 – LLC Stage Primary Voltage and Current, 115 VAC Input, CV Load, 8 A Current Limit, 8 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μs / div.

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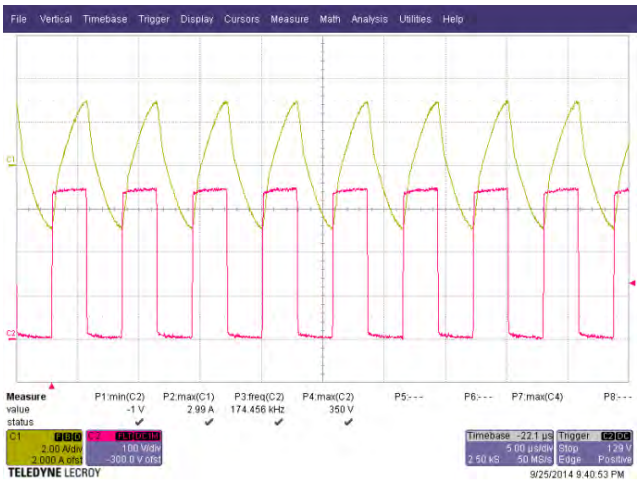

Figure 30 – LLC Stage Primary Voltage and Current, 132 VAC Input, CV Load, 8 A Current Limit, 22.5 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μs / div.

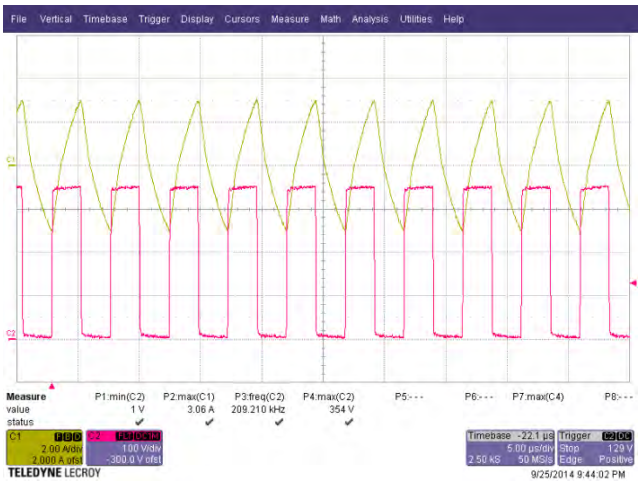

Figure 31 – LLC Stage Primary Voltage and Current, 132 VAC Input, CV Load, 8 A Current Limit, 16 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μs / div.

Figure 30 – LLC Stage Primary Voltage and Current, 132 VAC Input, CV Load, 8 A Current Limit, 8 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μs / div.

12.2 Results for 0.5 A Output Current Limit Setting

The LLC stage current was measured by inserting a current sensing loop in series with the ground side of resonating capacitor C14 that measures the LLC transformer (T1) primary current. The output was loaded with an electronic load set for constant voltage, with the current limit of the supply under test set at 0.5 A using an outboard resistor placed across R32. Waveforms were gathered for output voltages of 8 V, 4 V, 2 V, and 0.5 V. The waveforms show the behavior of the supply in the lower voltage portion of constant current operation. **At this current limit setting, the LLC converter operates in burst mode.**

Figure 31 – LLC Stage Primary Voltage and Current, 90 VAC Input, CV Load, 0.5 A Current Limit, 8 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 100 V, 500 μs / div.

Figure 32 – LLC Stage Primary Voltage and Current, 90 VAC Input, CV Load, 0.5 A Current Limit, 4 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 100 V, 500 μs / div.

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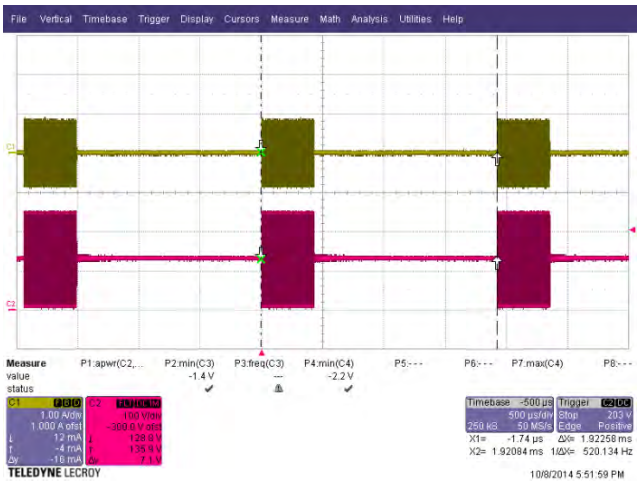

Figure 33 – LLC Stage Primary Voltage and Current, 90 VAC Input, CV Load, 0.5 A Current Limit, 2 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 100 V, 500 μs / div.

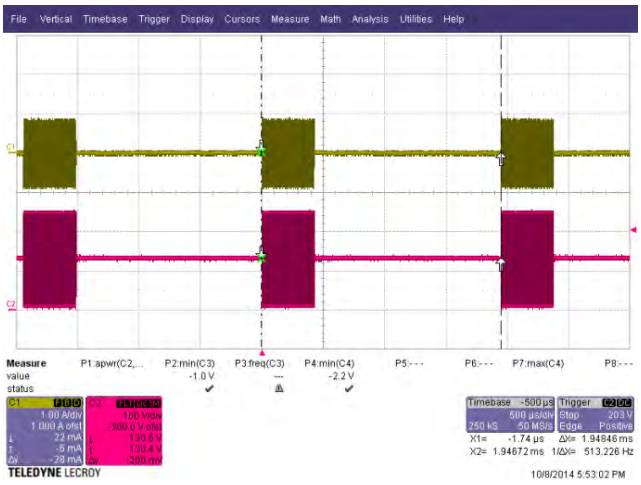

Figure 34 – LLC Stage Primary Voltage and Current, 90 VAC Input, CV Load, 0.5 A Current Limit, 0.5 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 100 V, 500 μs / div.

Figure 35 – LLC Stage Primary Voltage and Current, 115 VAC Input, CV Load, 0.5 A Current Limit, 8 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 100 V, 500 μs / div.

Figure 36 – LLC Stage Primary Voltage and Current, 115 VAC Input, CV Load, 0.5 A Current Limit, 4 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 100 V, 500 μs / div.

Figure 37 – LLC Stage Primary Voltage and Current, 115 VAC Input, CV Load, 0.5 A Current Limit, 2 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 100 V, 500 µs / div.

Figure 38 – LLC Stage Primary Voltage and Current, 115 VAC Input, CV Load, 0.5 A Current Limit, 0.5 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 100 V, 500 µs / div.

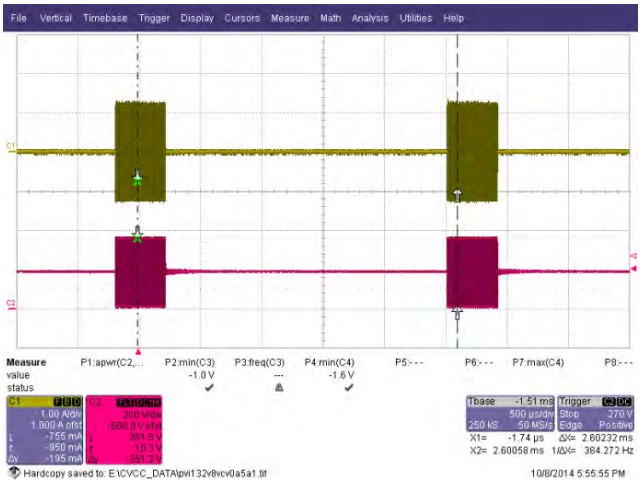

Figure 39 – LLC Stage Primary Voltage and Current, 132 VAC Input, CV Load, 0.5 A Current Limit, 8 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 200 V, 500 µs / div.

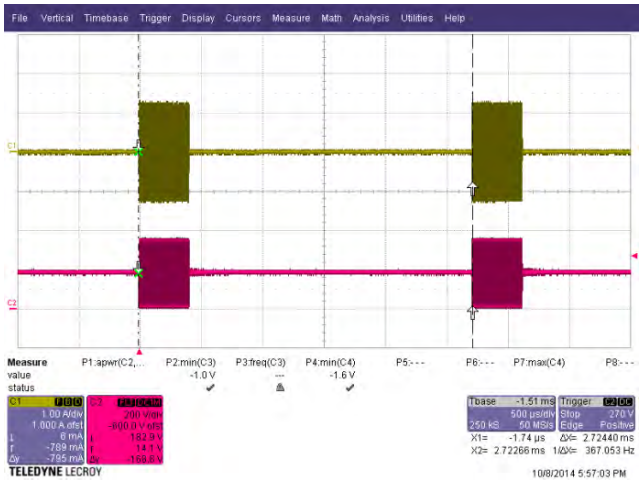

Figure 40 – LLC Stage Primary Voltage and Current, 132 VAC Input, CV Load, 0.5 A Current Limit, 4 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 200 V, 500 µs / div.

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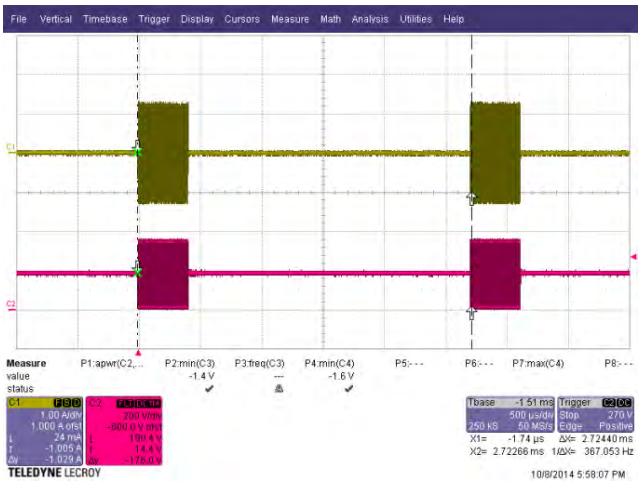

Figure 41 – LLC Stage Primary Voltage and Current, 132 VAC Input, CV Load, 0.5 A Current Limit, 2 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 200 V, 500 µs / div.

Figure 42 – LLC Stage Primary Voltage and Current, 132 VAC Input, CV Load, 0.5 A Current Limit, 0.5 V Load Setting.
Upper: Current, 1 A / div.
Lower: Voltage, 200 V, 500 µs / div.

12.3 Output Rectifier Peak Reverse Voltage

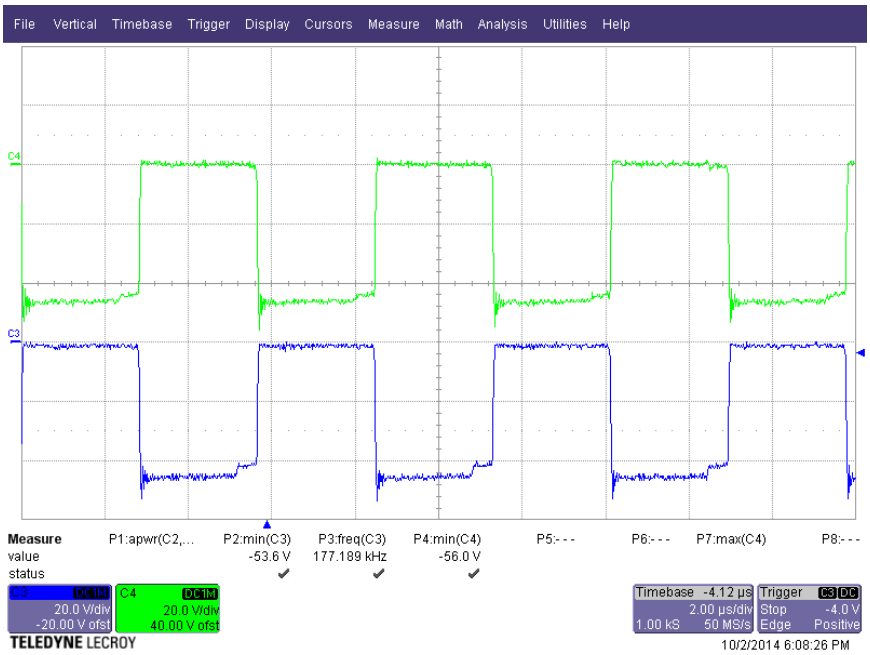

Figure 43 – Output Rectifier (D4 & D5) Reverse Voltage, 132 VAC, 22.5 V, 8 A Load.
Upper: D4 PIV, 20 V / div.
Lower: D5 PIV, 20 V, 2 µs / div.
Rectifier PIV at 132 VAC is 93% of maximum rating for 60 V Schottky diode. If this is not acceptable, use 80 V or 100 V device.

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12.4 LLC Start-up Output Voltage and Transformer Primary Current Using Constant Voltage Output Load

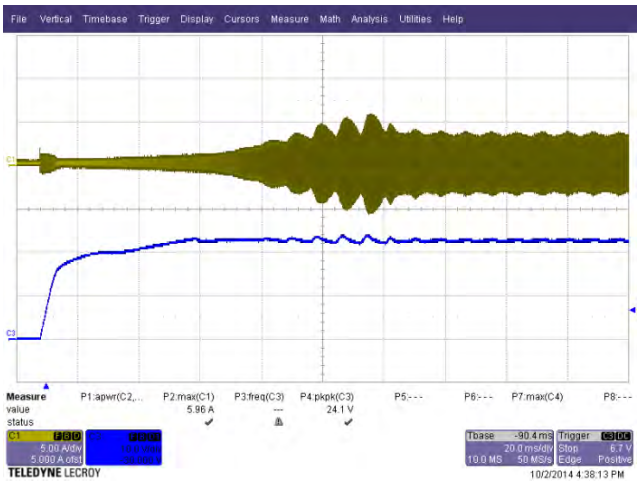

Figure 44 – LLC Start-up. 90 VAC, 22.5 V / 8 A CV Load.
Upper: LLC Primary Current, 5 A / div.
Lower: LLC V_{OUT}, 10 V, 20 ms / div.

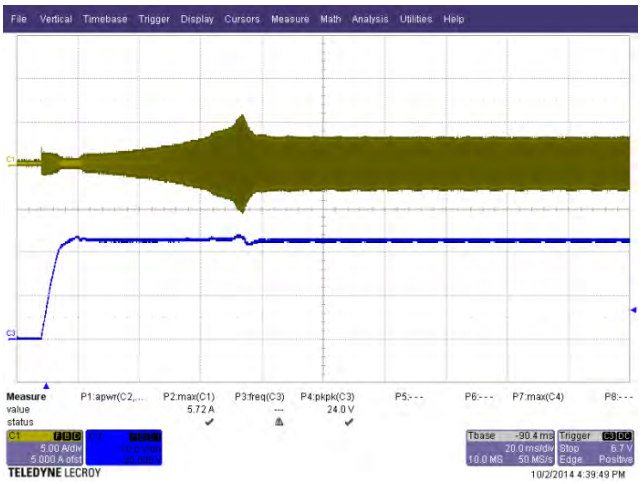

Figure 45 – LLC Start-up. 115 VAC, 22.5 V / 8 A CV Load.
Upper: LLC Primary Current, 5 A / div.
Lower: LLC V_{OUT}, 10 V, 20 ms / div.

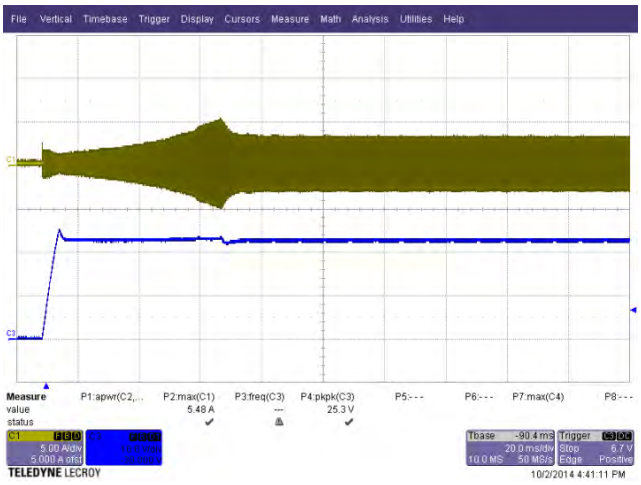

Figure 46 – LLC Start-up. 132 VAC, 22.5 V / 8 A CV Load.
Upper: LLC Primary Current, 5 A / div.
Lower: LLC V_{OUT}, 10 V, 20 ms / div.

12.5 LLC Output Short-Circuit

The figures below show the effect of an output short circuit on the LLC primary current and on the output current. Figure 47 shows the output voltage and primary current response to an output short circuit. Figure 48 shows the output current and output voltage during a short circuit. A mercury displacement relay was used to short the output in order to achieve a fast, bounce-free connection. Even so, there is some relay bounce in the short circuit test shown in Figure 48. The supply shuts down without damage and recovers when the short is removed.

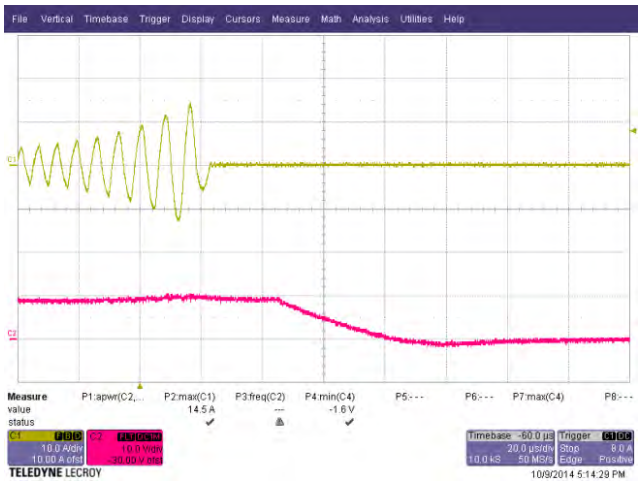

Figure 47 – Output Short-Circuit Test.
Upper: LLC Primary Current, 10 A / div.
Lower: LLC V_{OUT}, 10 V, 20 µs / div**.**

Figure 48 – Output Short-Circuit Test.
Upper: LLC I_{OUT}, 20 A / div.
Lower: LLC V_{OUT}, 20 V, 100 µs / div.

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12.6 Output Ripple Measurements

12.6.1 *Ripple Measurement Technique*

For DC output ripple measurements a modified oscilloscope test probe is used to reduce spurious signals. Details of the probe modification are provided in the figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 μF / 50 V ceramic capacitor and 1.0 μF / 100 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

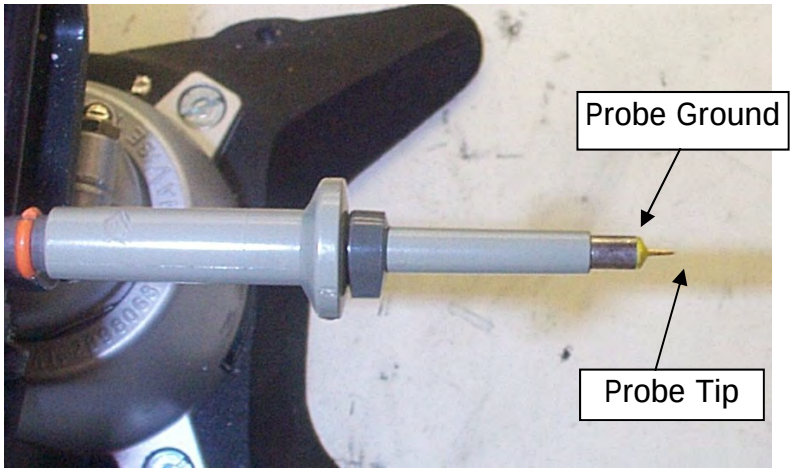

Figure 49 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

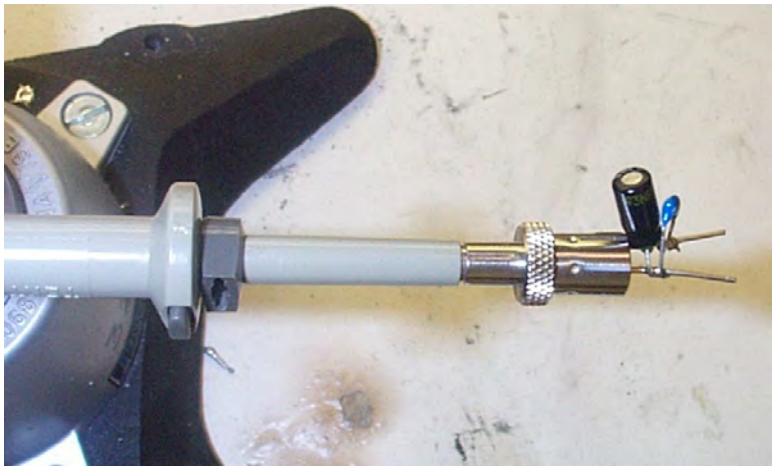

Figure 50 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

12.6.2 ***Ripple Measurements***

12.6.2.1 8 A Output Current Limit Setting

These measurements were taken using the 8 A default current limit setting. Output ripple voltage measurements were made using an AC coupled probe.

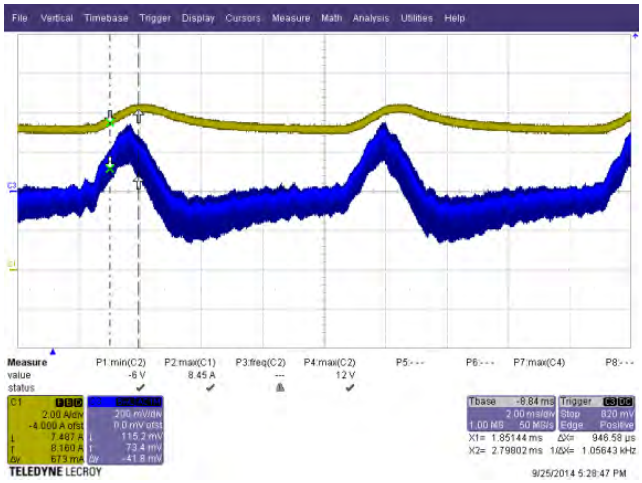

Figure 51 – Output Ripple, 90 VAC, 22.5 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

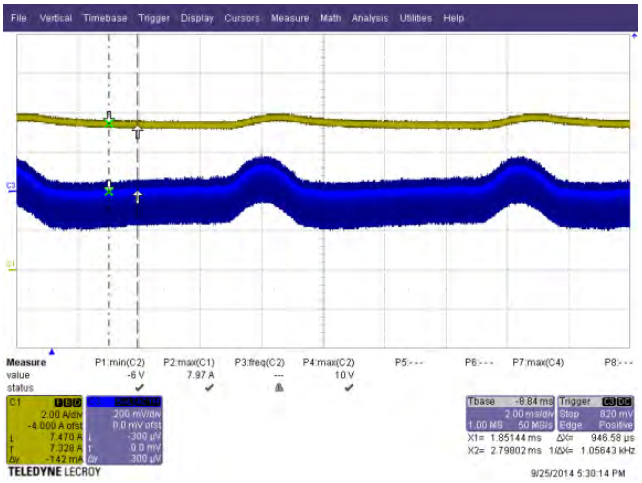

Figure 52 – Output Ripple, 90 VAC, 16 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

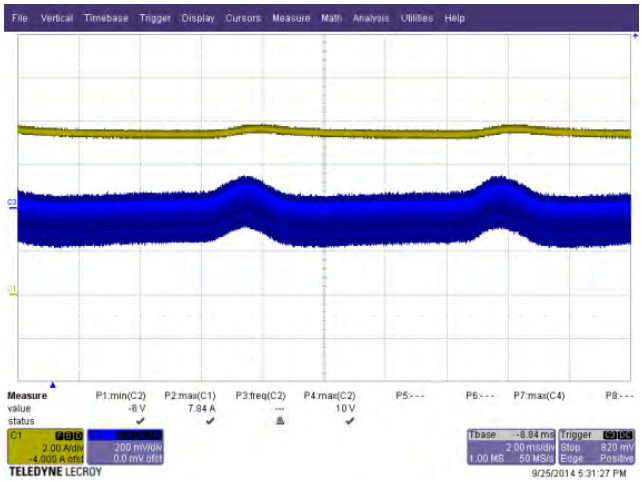

Figure 53 – Output Ripple, 90 VAC, 12 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

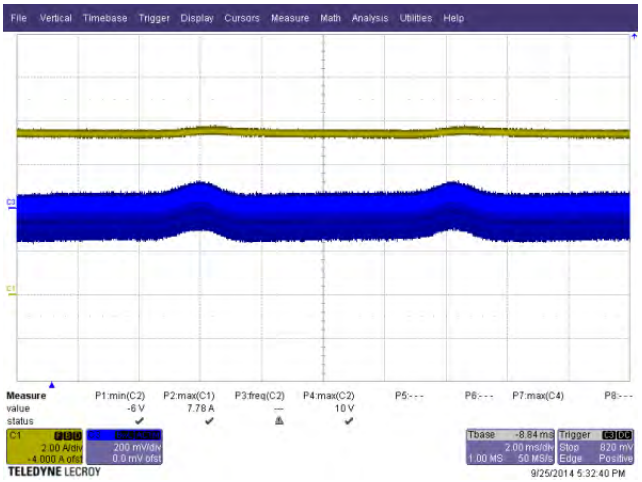

Figure 54 – Output Ripple, 90 VAC, 8 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

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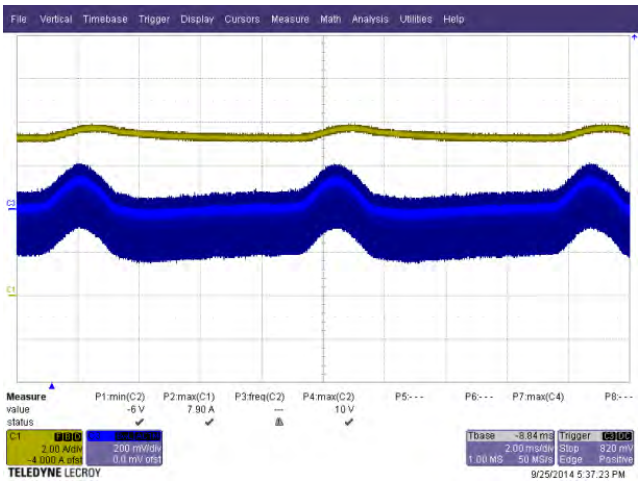

Figure 55 – Output Ripple, 115 VAC, 22.5 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

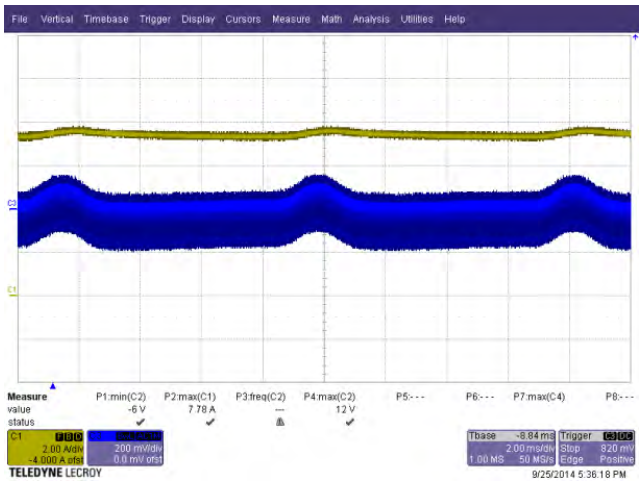

Figure 56 – Output Ripple, 115 VAC, 16 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

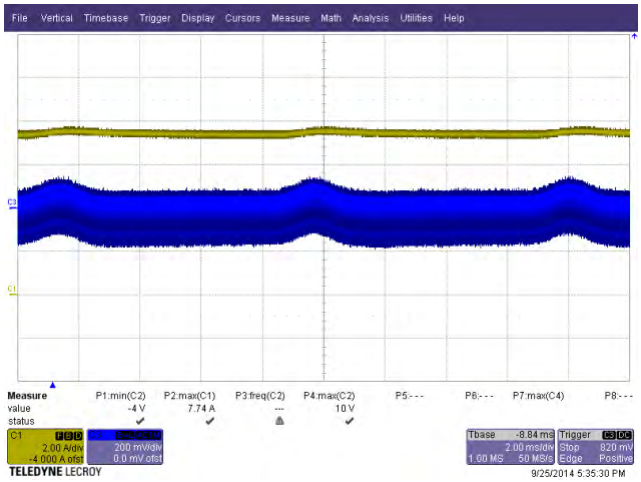

Figure 57 – Output Ripple, 115 VAC, 12 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

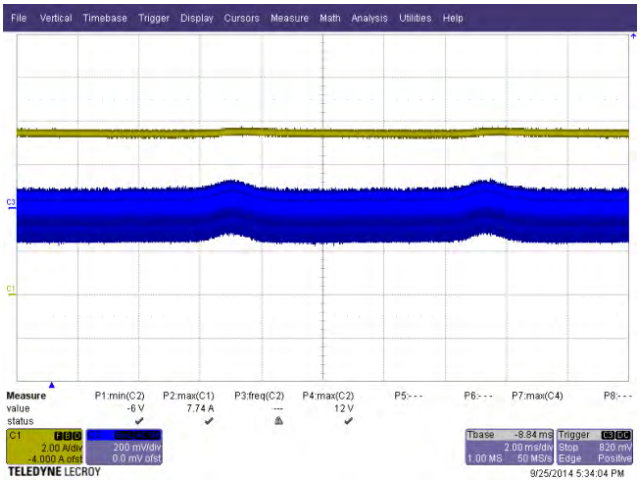

Figure 58 – Output Ripple, 115 VAC, 8 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

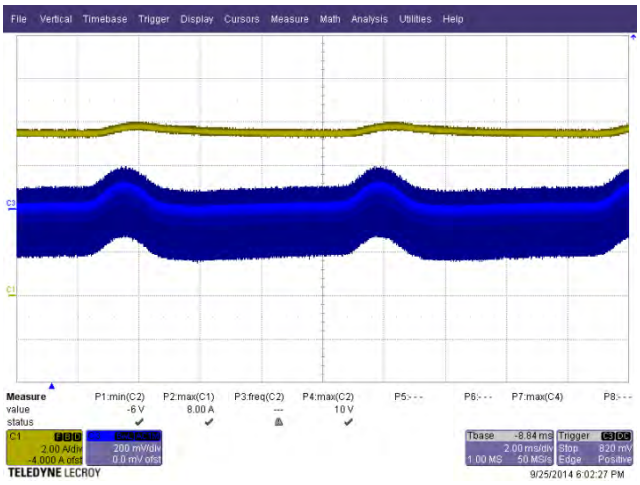

Figure 59 – Output Ripple, 132 VAC, 22.5 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

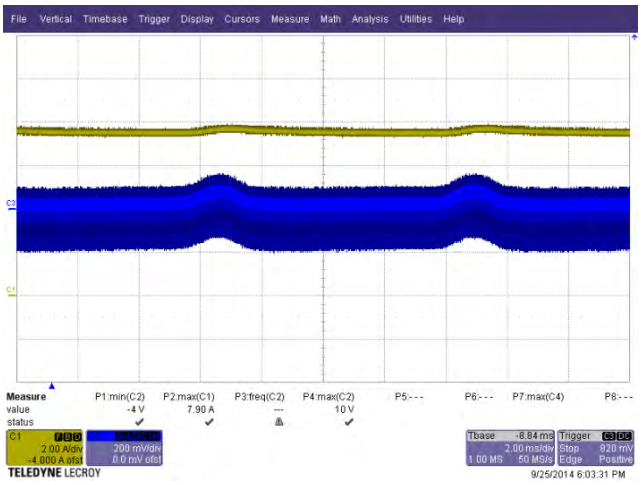

Figure 60 – Output Ripple, 132 VAC, 16 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

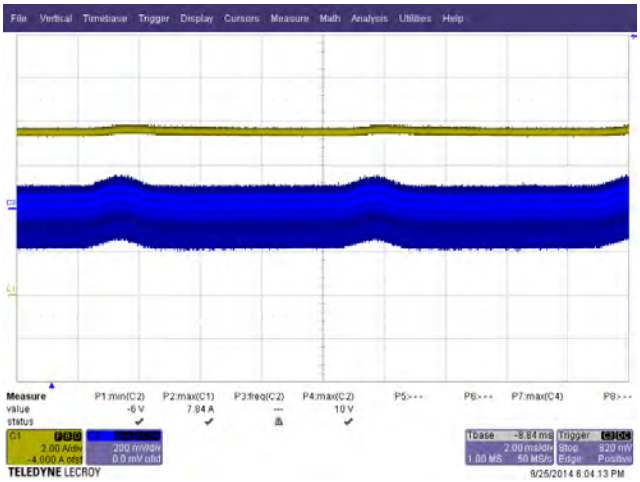

Figure 61 – Output Ripple, 132 VAC, 12 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

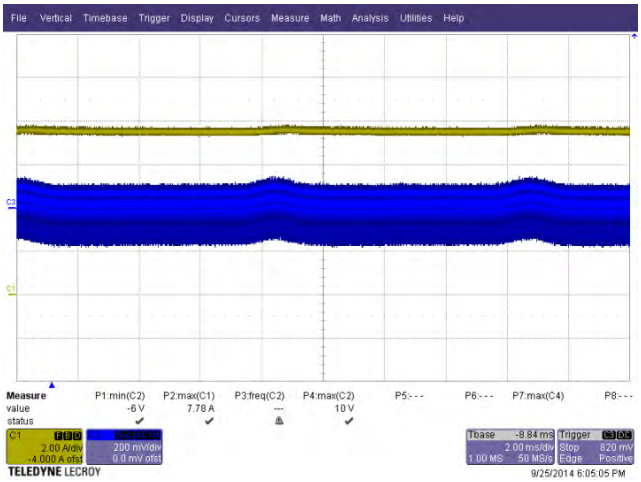

Figure 62 – Output Ripple, 132 VAC, 8 V CV Load, 8 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 200 mV, 2 ms / div.

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12.6.2.2 0.5 A Output Current Limit Setting

For this output current setting, the power supply operates in burst mode. Since the CV electronic load cannot source current (as compared to an actual battery being charged), the output voltage collapses between bursts. A DC coupled probe is used for measurements in this instance due to the high amplitude of the ripple voltage compared to the DC output voltage.

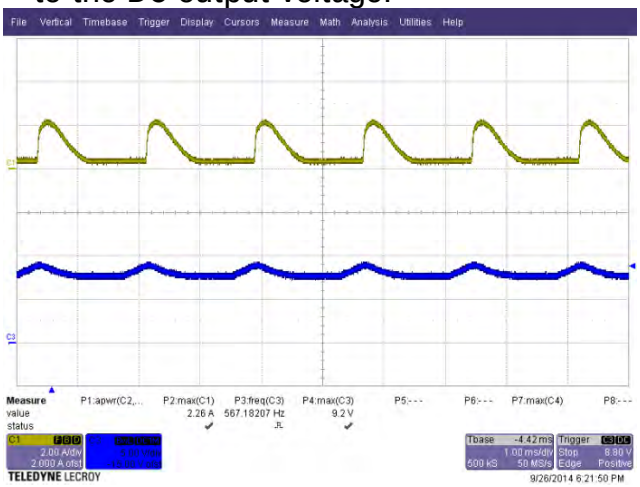

Figure 63 – Output Ripple, 90 VAC, 8 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 5 V, 1 ms / div.

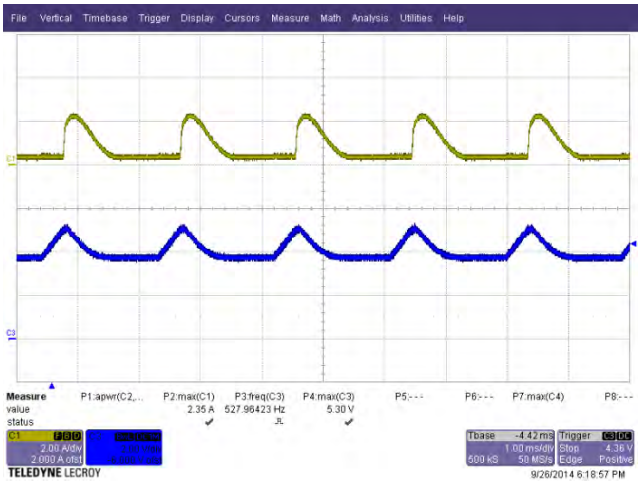

Figure 64 – Output Ripple, 90 VAC, 4 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 2 V, 1 ms / div.

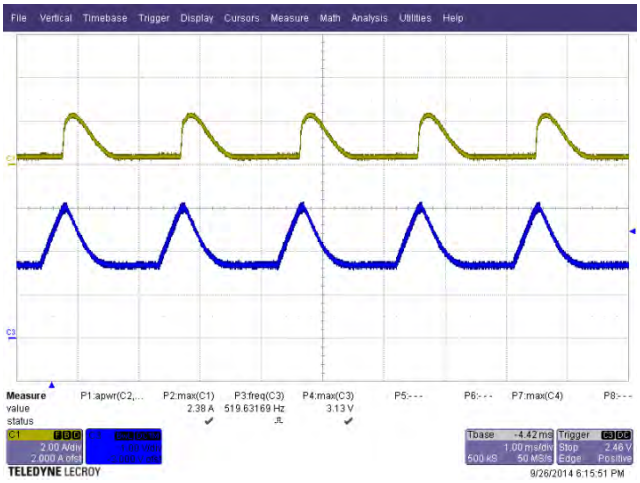

Figure 65 – Output Ripple, 90 VAC, 2 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 1 V, 1 ms / div.

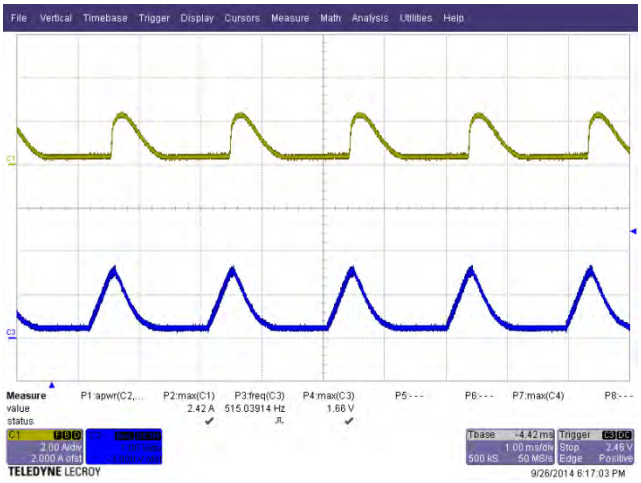

Figure 66 – Output Ripple, 90 VAC, 0.5 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 1 V, 1 ms / div.

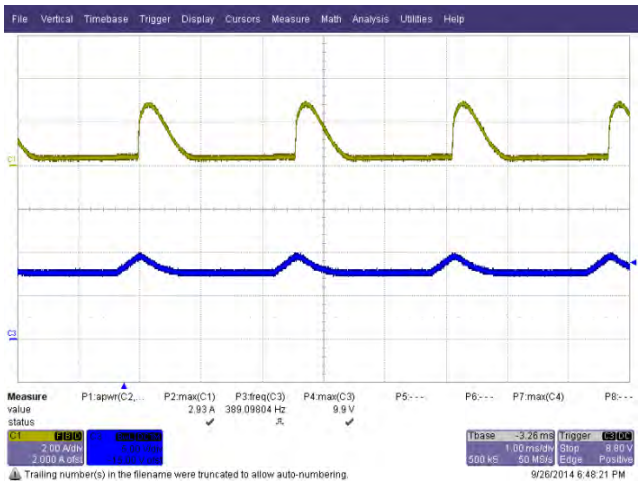

Figure 67 – Output Ripple, 115 VAC, 8 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 5 V, 1 ms / div.

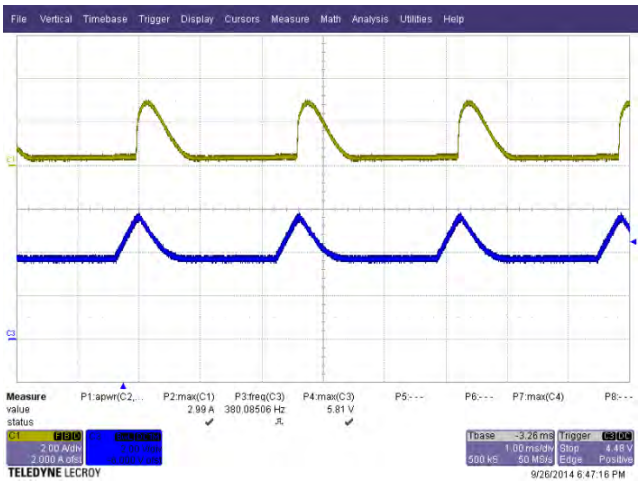

Figure 68 – Output Ripple, 115 VAC, 4 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 2 V, 1 ms / div.

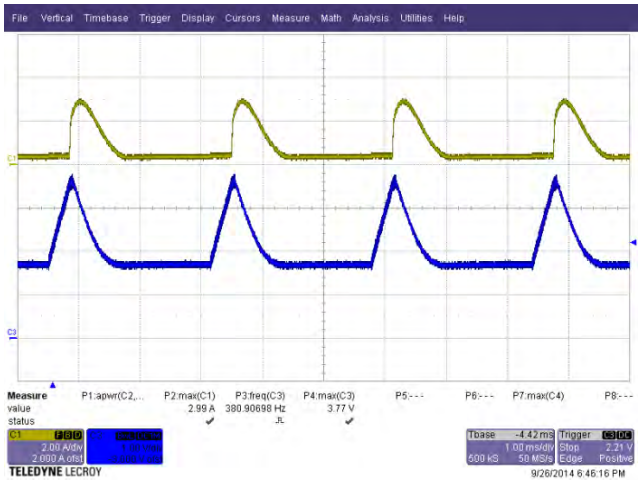

Figure 69 – Output Ripple, 115 VAC, 2 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 1 V, 1 ms / div.

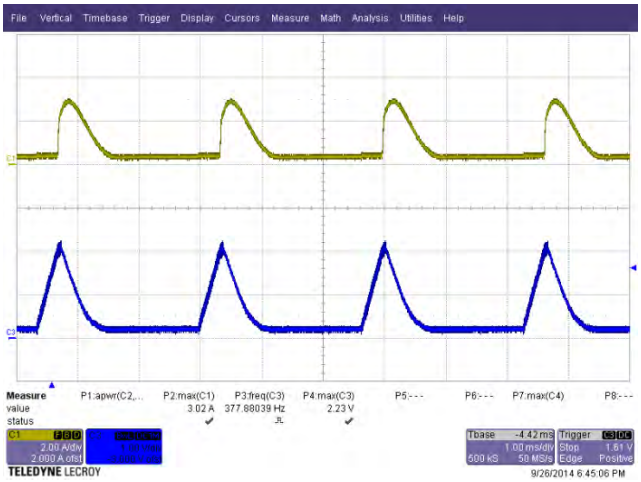

Figure 70 – Output Ripple, 115 VAC, 0.5 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 1 V, 1 ms / div.

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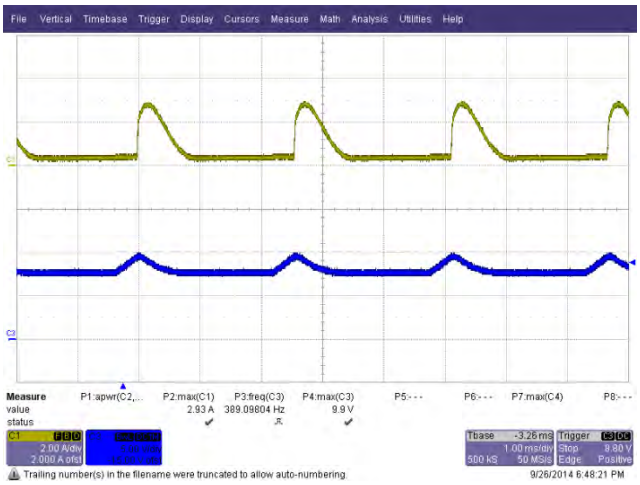

Figure 71 – Output Ripple, 132 VAC, 8 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 5 V, 1 ms / div.

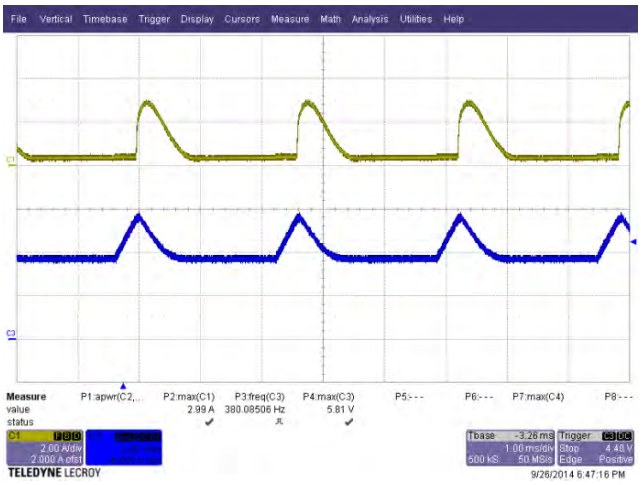

Figure 72 – Output Ripple, 132 VAC, 4 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 2 V, 1 ms / div.

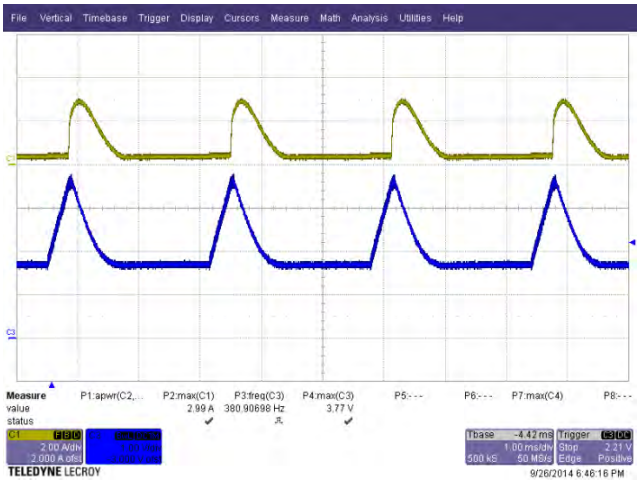

Figure 73 – Output Ripple, 132 VAC, 2 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 1 V, 1 ms / div.

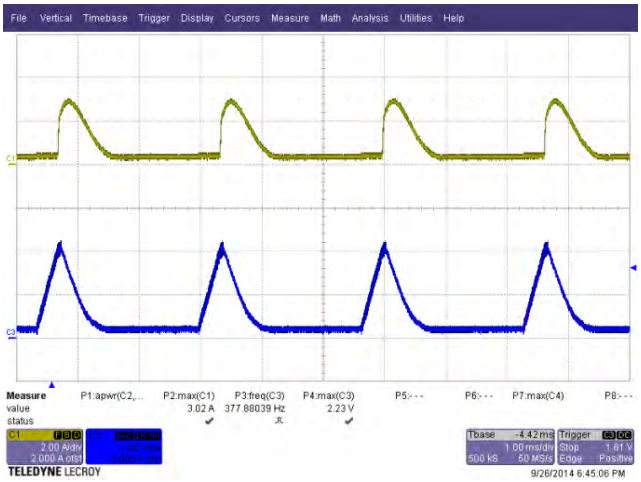

Figure 74 – Output Ripple, 132 VAC, 0.5 V CV Load, 0.5 A Current Limit.
Upper: I_{OUT}, 2 A / div.
Lower: V_{OUT} Ripple, 1 V, 1 ms / div.

13 Temperature Profiles

The board was operated at room temperature, with output set at maximum using a constant voltage load. For each test condition the unit was allowed to thermally stabilize (~1 hr) before measurements were made.

13.1 Spot Temperature Measurements

Position	Temperature (°C)		
	90 VAC	**115 VAC**	**132 VAC**
T1	66.9 (pri) / 68 (sec)	73.6 (pri) / 74.6 (sec)	78.7 (pri) / 80.4 (sec)
BR1	58	54	50.5
L1	69.5	57	52
L2	59	53	49
U1	60	58	59
C3/C4	47	45	41.4
D4/D5	62/64	64.5/64.9	67/67
R34/R35	59	59	59
AMB	24	24	24

13.2 90 VAC, 60 Hz, 100 % Load Temperature Profile

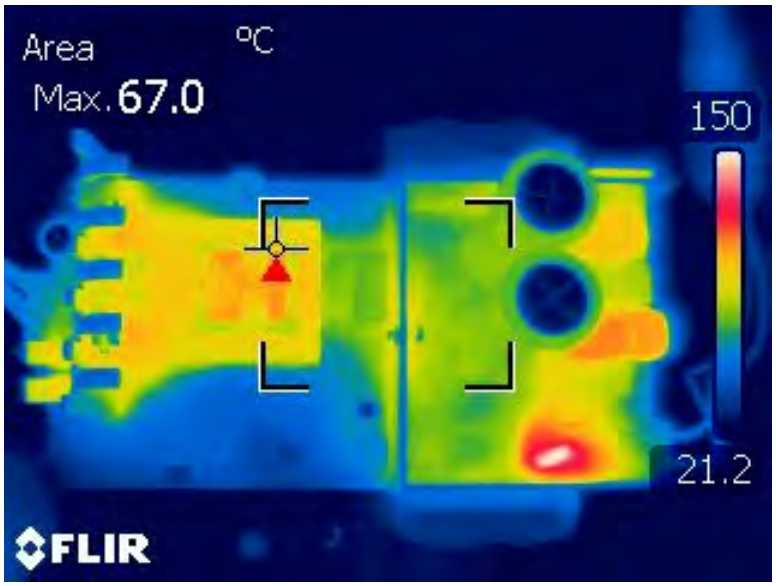

Figure 75 – Top View Thermal Picture, 90 VAC.

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13.3 115 VAC, 60 Hz, 100 % Load Temperature Profile

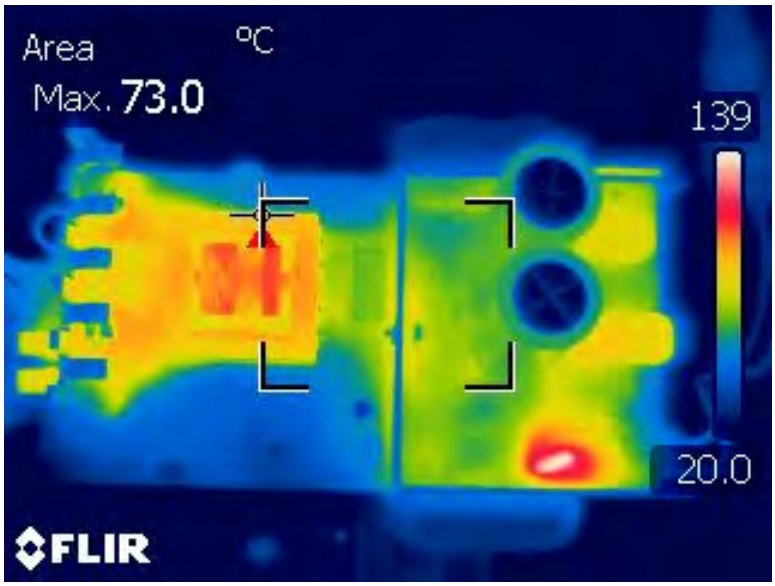

Figure 76 – Top View Thermal Picture, 100% Load, 115 VAC.

13.4 132 VAC, 60 Hz, 100 % Load Temperature Profile

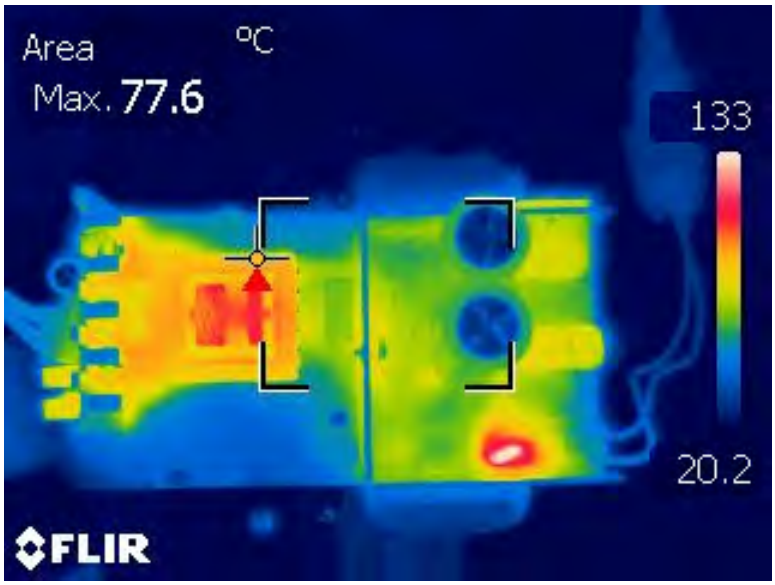

Figure 77 – Top View Thermal Picture, 100% Load, 132 VAC.

14 Constant Current Output Gain-Phase

Gain-phase was tested using an electronic load set to constant voltage mode at 22.5 V with the output current limit of the UUT set for 8 A. This is a worst-case setting that places the output in constant current mode near the knee of the CV/CC V-I characteristic so that the output power is maximized and operating frequency is minimized, placing the operating point of the LLC converter near resonance. Using a CV load maximizes the CC loop gain (worst case for control loop) and simulates operating while charging a battery. Using the constant resistance setting for the electronic load will yield overly optimistic results for gain-phase measurements and for determining component values for frequency compensation.

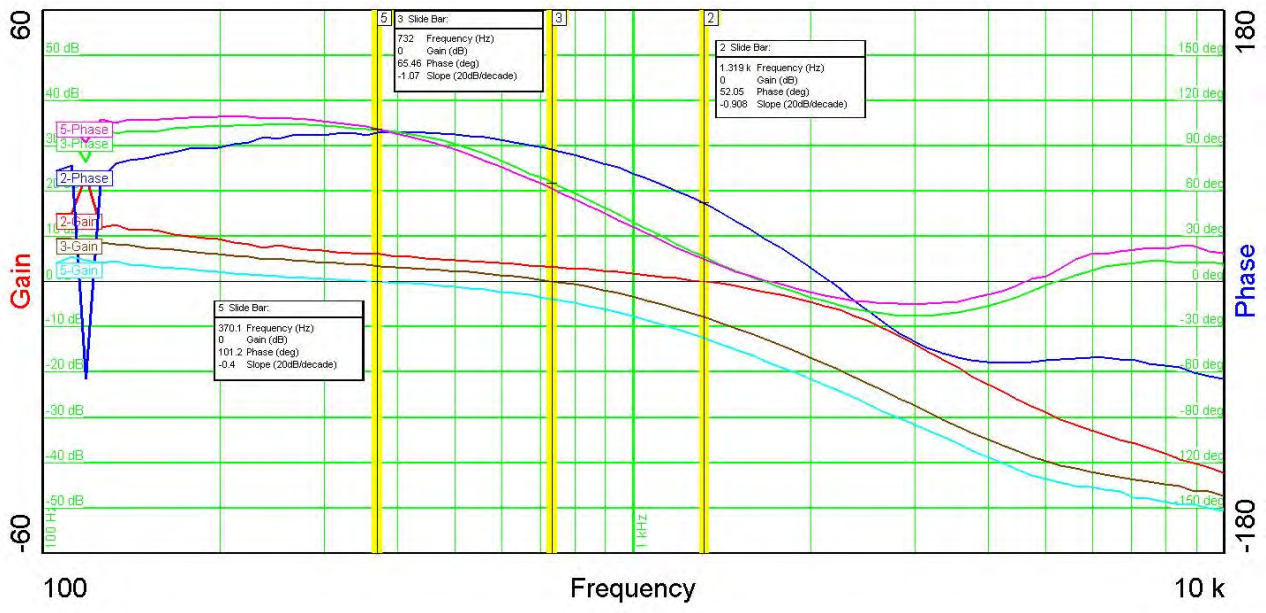

Figure 78 – LLC Converter Gain-Phase, 100% Load, Constant Current Output, Constant Voltage Load. Red/Blue – 90 VAC Gain and Phase Crossover Frequency – 1.3 kHz, Phase Margin – 52°. Brown/Green – 115 VAC Gain and Phase Crossover Frequency – 730 Hz, Phase Margin – 65°. Aqua/Pink – 132 VAC Gain and Phase Crossover Frequency – 370 Hz, Phase Margin – 101°.

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15 Conducted EMI

Conducted EMI tests were performed using a floating resistive load (3 Ω).

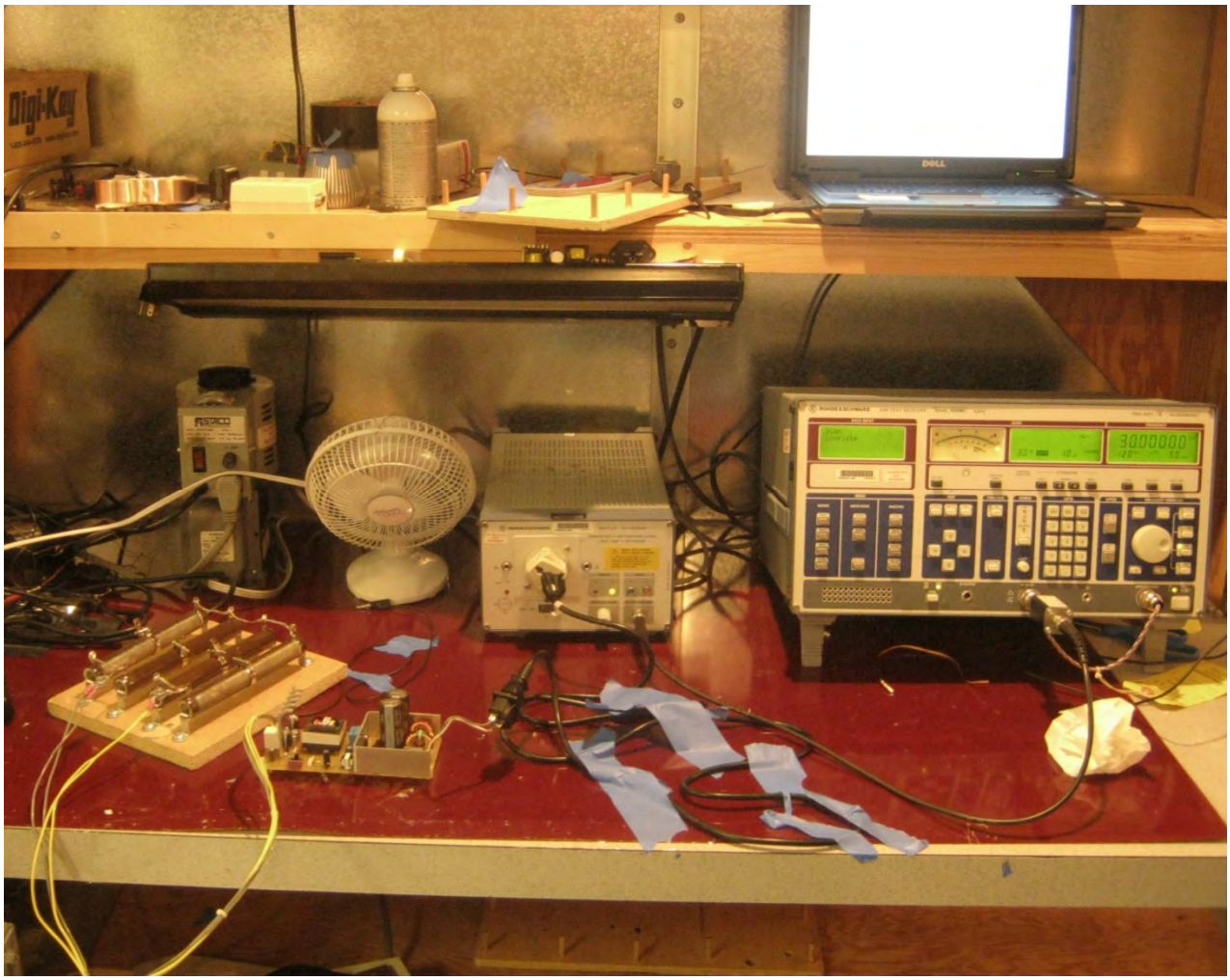

Figure 79 – EMI Set-up with Floating Resistive Load.

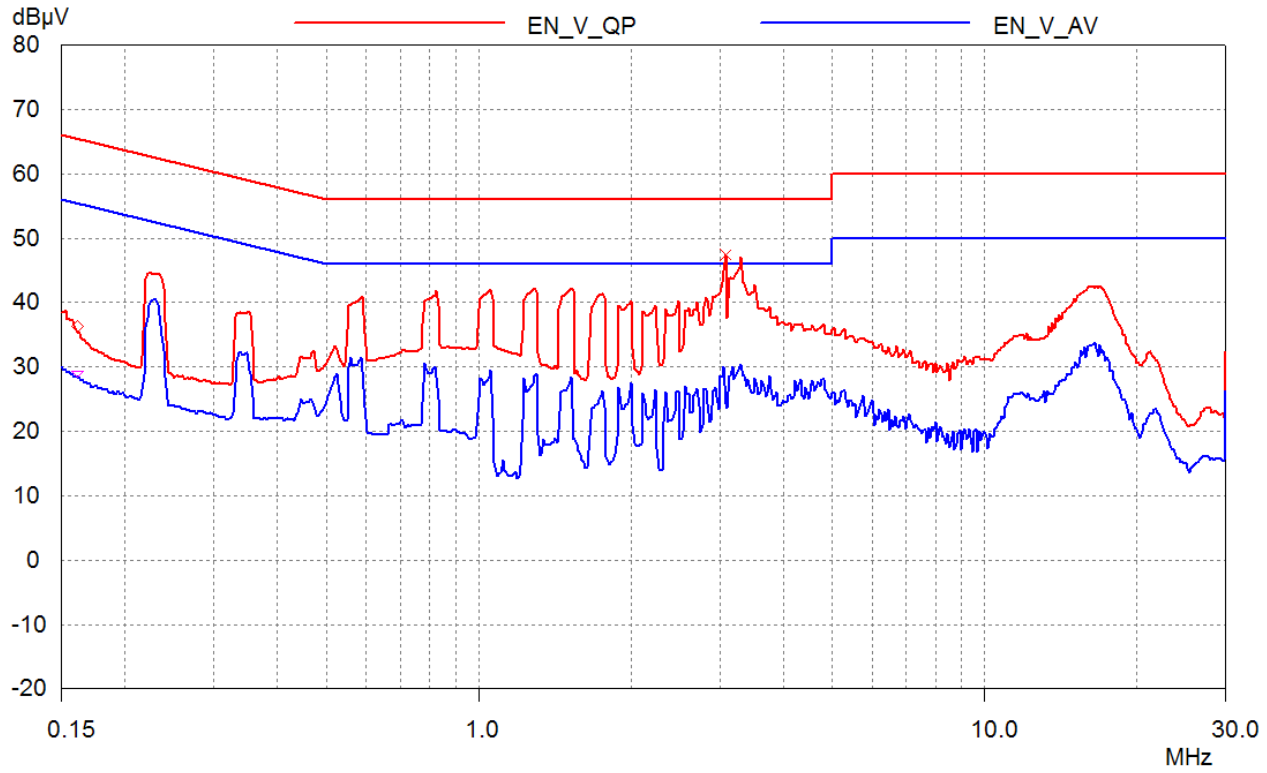

Figure 80 – Conducted EMI, 115 VAC, 3 Ω Floating Load.

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16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
07-Oct-15	4.1	RH	Initial Release.	Apps & Mktg
21-Jan-16	4.2	KM	Updated Schematic.	
15-May-17	4.3	RH	Transformer Drawing Updated.	
31-May-17	4.4	RH	Updated Schematic in Figure 3a.	

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