Jaypee University of Engineering & Technology, Guna (M.P)
Department of Computer Science & Engineering

Course: Computer Organization & Architecture
(B. Tech. IV/VI Sem, Code: CS107/18B11CI414)

Tutorial-5
Topic: Register Transfer & Microoperations

1. Design a common bus system using multiplexers and tri-states buffers for sharing data with CPU coming from five, 4-bit source registers.

2. Design 2-bit logic circuit which performs following four logical micro operations:

Selection lines S_1S_0	Micro operations
00	A ∧ B
01	A ∨ B
10	A⊕B
11	$\overline{B}$

3. Design 4-bit shift logic circuit which performs following micro operations:

Selection lines S_1S_0	Micro operations
00	shl B
01	ashr A
10	Cir A
11	Cil B

4. Design a 2-bit, 8-operation Arithmetic Logic Unit (ALU) which performs following operations as given in the table. Consider C_{in} as initial carry of full adder.

Control Lines $S_1S_0C_{in}$	Micro operations
000	Increment : $F = A + 3$
001	Subtract: $F = A - B$
010	Addition: $F = A + B$
011	Decrement: $F = A - 2$
100	AND: $F = A \wedge B$
101	XOR: $F = A \oplus B$
110	logical left shift of B: F = shl B
111	logical right shift of A: $F = shr\ A$