Computer Architecture - Pipeline and Performance Problems

2. Pipeline Segment Timing Problem

Given: Segment times: $t1 = 50$ ns, $t2 = 30$ ns, $t3 = 95$ ns, $t4 = 45$ ns; Register delay $tr = 5$ ns

Clock cycle time = 95 + 5 = 100 ns

(i) Time to add 100 pairs = (4 + 100 - 1) × 100 ns = 10,300 ns = 10.3 µs

(ii) Split t3 (95 ns) into two ~=47.5 ns parts. New max segment = 50 ns

New clock = 50 + 5 = 55 ns, Stages = 5

Time = (5 + 100 - 1) × 55 ns = 5,720 ns = 5.72 µs

3. Morris Mano Pipeline Problem

Delays: Memory read = 40 ns, Multiply = 45 ns, Transfer to R3 = 5 ns, Add = 15 ns

(iii) Min clock cycle = max(40, 45, 5, 15) + register delay = 45 + 5 = 50 ns

(iv) Non-pipeline time = 40 + 45 + 15 = 100 ns

(v) Speedup for 10 tasks = 1000 / 650 ~= 1.54

Speedup for 100 tasks = 10000 / 5150 ~= 1.94

(vi) Max theoretical speedup = non-pipelined time / pipeline cycle = 100 / 50 = 2

4. Floating Point Computation

250 billion operations, Speed = 100 MFLOPS = 10^8 ops/sec

Time = $2.5 \times 10^{11} / 10^8$ = 2500 seconds

5. Matrix Multiplication using Vector Processor

40×40 matrices

(i) Inner products = 40 × 40 = 1600

(ii) Multiply-add operations = 1600 × 40 = 64,000

6. Floating Point Pipeline Processors

4 processors with 40 ns cycle: 400 operations / 4 = 100 each -> 100 × 40 ns = 4000 ns

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Single processor with 10 ns cycle: 400 × 10 ns = 4000 ns

-> Time is the same in both cases: 4000 ns