Jaypee University of Engineering & Technology, Guna (M.P.)
Department of Computer Science & Engineering

Course: Computer Organization & Architecture
(B. Tech. IV/VI Sem, Code: CS107/18B11CI414)

Tutorial-10
Topic: Memory address map and cache access time

1. a. How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes? **[Ans: 16]**
   b. How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? **[Ans: 11, 7]**
   c. How many lines must be in decoder for chip select? Specify the size of the decoders. **[Ans: 4, 4:16]**

2. A computer employs RAM chips of 2048 x 8 and ROM chips of 512 x 8. The computer system needs total of 4KB of RAM and 1KB of ROM.
   a. How many RAM and ROM chips are needed? **[Ans: 2, 2]**
   b. Draw a block diagram of required architecture of memory system.
   c. Give the all possible address maps (ranges) in hexadecimal for RAM and ROM chips.
   [Ans: Address Maps for RAM1=0000-07FF; RAM2=0800-0FFF;
   ROM1=1000-11FF or 1200-13FF or 1400-15FF or 1600-17FF;
   ROM2=1800-19FF or 1A00-1BFF or 1C00-1DFF or 1E00-1FFF]

3. Assume that a read request takes 50 nsec on cache miss and 5 nsec on cache hit. If 80% of the processor read requests results in a cache hit. Find average read access time of cache memory.
   [Ans: 14 nsec]

4. Suppose in 1000 memory references, there are 40 misses in L1 cache and 10 misses in L2 cache. If the miss penalty of L2 is 200 clock cycles, hit time of L1 is 1 clock cycle, and hit time of L2 is 15 clock cycles. What will be the average memory access time if the system uses 1 GHz operating frequency?
   [Ans: 1.634 nsec]

5. The memory access time is 2 nsec for a read operation with a hit in cache, 6 nsec for a read operation with a miss in cache, 4 nsec for a write operation with a hit in cache, and 10 nsec for a write operation with a miss in cache. The execution of a sequence of instructions involves 1000 instruction fetch operations, 600 memory operand read operations, and 400 memory operand write operations. The cache hit ratio is 0.8. Find the average memory access time (in nanoseconds) in executing the sequence of instructions. **[Ans: 3.28 nsec]**