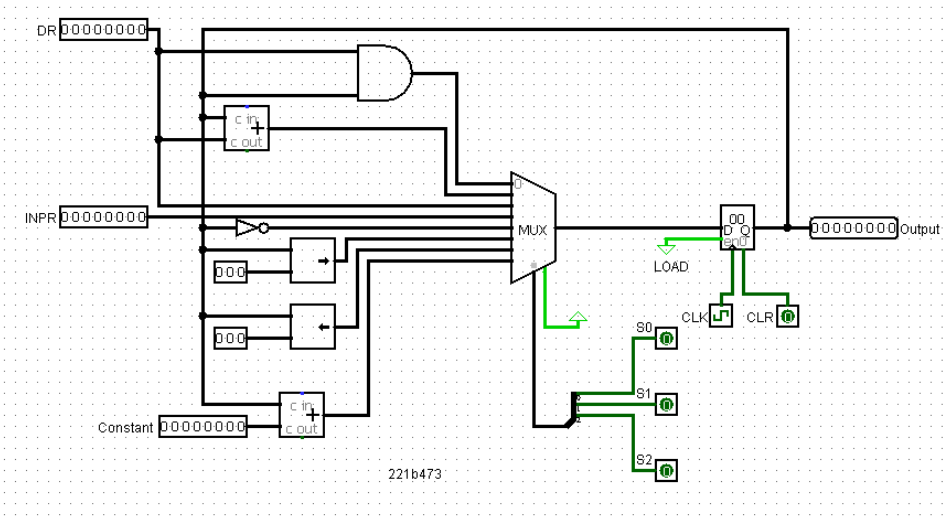
EXPERIMENT-8

Aim: Design of accumulator and basic CPU.

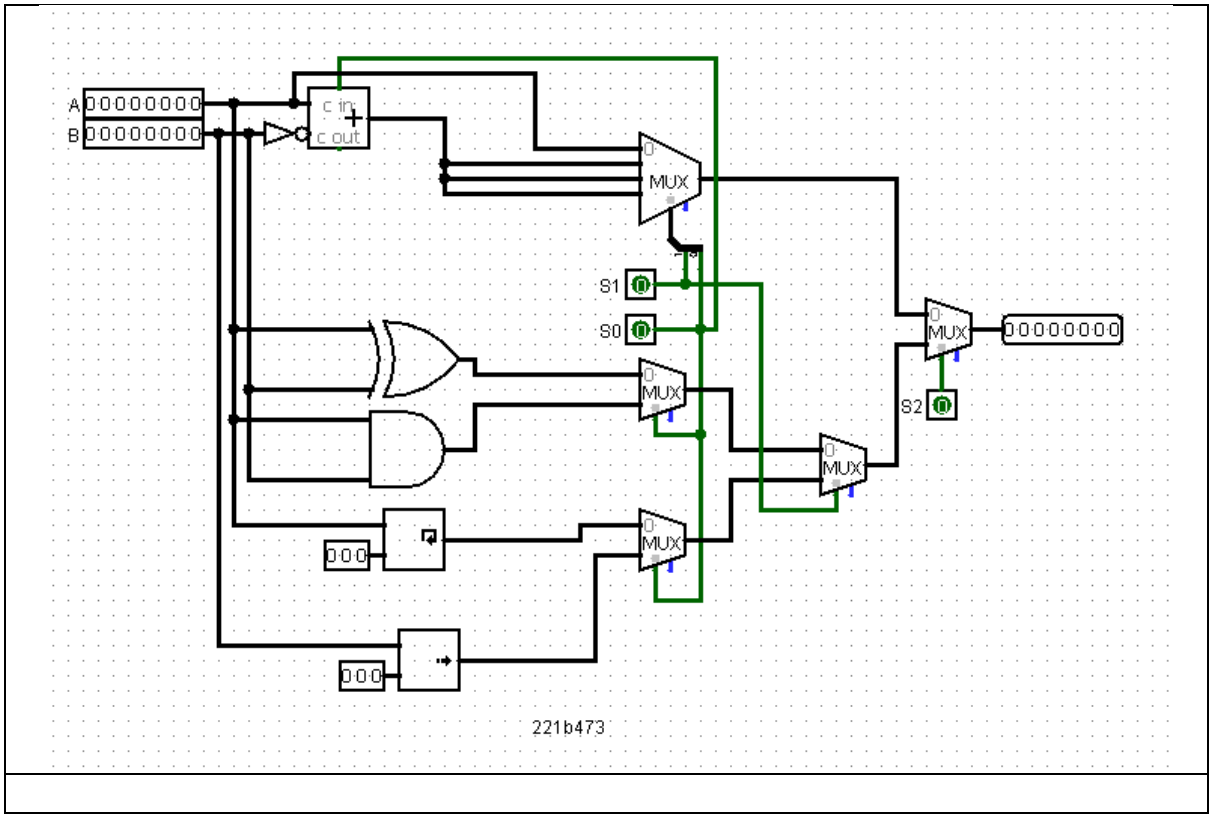
Exercise-1: Design and verify 8-bit logic diagram of accumulator shown Fig. 1 in that performs following operations. Use in built blocks of register as accumulator, 8:1 multiplexer as control (gates) unit, and two 8-bit input pins one for data register (DR) and other as input register (INPR).

Logic Diagram



Exercise-2: Design and verify 8-bit CPU shown Fig. 3 that performs operations given in Table-2. Use in built blocks of registers, multiplexers and decoder and sub circuit of ALU (designed in experiment no. 6).

Logic Diagram


A 00000000
B 00000000
c in
c out
MUX
S1
S0
MUX
MUX
MUX
MUX
S2
00000000
000
000
221b473