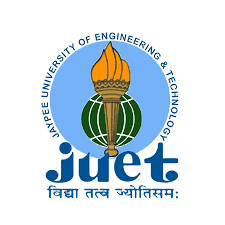
**JAYPEE UNIVERSITY OF ENGINEERING & TECHNOLOGY, GUNA**

**DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING**



**COMPUTER ORGANIZATION & ARCHITECTURE LAB**

**(COURSE CODE: CS208)**

**SUBMITTED TO: Dr. Ranu Gupta**

**NAME OF STUDENT: Priyanshi Mishra**

**ENROLLMENT NO: 221B473**

**BATCH: B14**

**BRANCH: CSE**

**SESSION: 2024-25**

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| **S.No.** | **Aim of the experiment** | **Date of submission** | **signature** | **remarks** |
| 1. | Designing of basic digital circuits using logic gates. |  |  |  |
| 2. | Design of binary adders and subtractors. |  |  |  |
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**EXPERIMENT-1**

**Aim: Designing of basic digital circuits using logic gates.**

**Exercise-1:** Design two inputs and five outputs All-in-One logic gate circuitusing Logisim simulator with (i) data width 1 (ii) data width 4.

**(i) data width 1**

**i) data width 1**

|  |  |
| --- | --- |
| **Boolean Expressions** | **Logic Diagram** |
| C = ~A  D = A.B  E = A+B  F = ~(A.B)  G = AB | 221b473 |
| **Truth Table** or **Karnaugh (K) Map** |
|  |

**(ii) data width 4.**

|  |  |
| --- | --- |
| **Boolean Expressions** | **Logic Diagram** |
| C = ~A  D = A.B  E = A+B  F = ~(A.B)  G = AB | 221B473 |
| **Truth Table** or **Karnaugh (K) Map** |
|  |

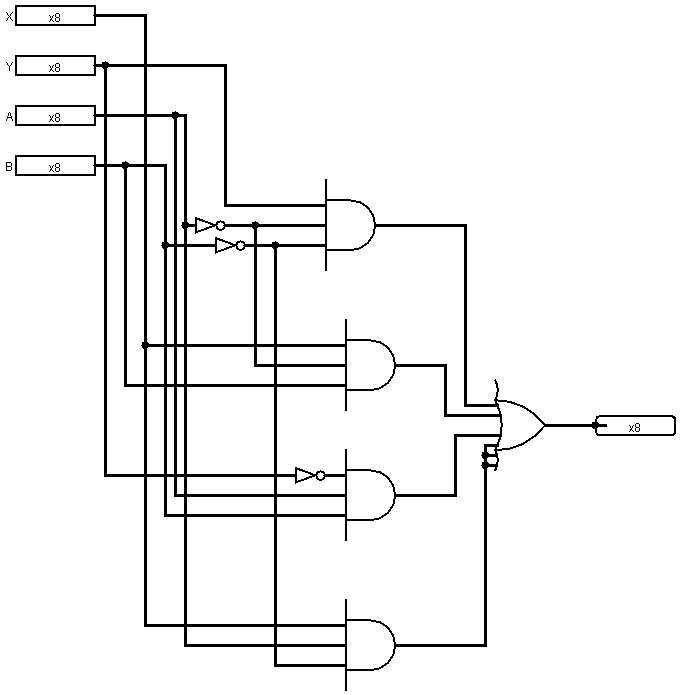
**Exercise-2**: Design two inputs and one output All-in-One logic gate diagram using Logisim

simulator with (i) data width 1 (ii) data width 8.

**(i) data width 1**

|  |  |
| --- | --- |
| **Boolean Expressions** | **Logic Diagram& Karnaugh (K) Map** |
| C = ~A~BY+ ~ABX+A~BX+AB~Y | \\192.168.4.11\221b473\sem6\COA Lab\Lab 1\exercise-2.png |
| **Truth Table** |
|  |

**(ii) data width 8.**



**Exercise-3:** Design a three-input majority detector combinational digital circuit using Logisim simulator which shows output equal to 1 if the input variables have more 1's than 0's, the output is 0 otherwise.

|  |  |
| --- | --- |
| **Boolean Expressions** | **Logic Diagram& Karnaugh (K) Map** |
| Y = B.C + A.C + A.B | \\192.168.4.11\221b473\sem6\COA Lab\Lab 1\exercise-3.png |
| **Truth Table** |
|  |

**Exercise-4:** Design a combinational circuit with three inputs and three outputs. When the input is 0, 1, 2, or 3, the output is one greater than the input and when the input is 4, 5, 6, or 7, the output is one less than the input. Display the input and output digits using Hex digit display with splitter.

|  |  |
| --- | --- |
| **Boolean Expressions** | **Logic Diagram** |
| X = B.C + A.C + A.B  Y = A.~B.~C + ~A.~B.C + A.B.C + ~A.B.~C  Z = ~C |  |
| **Truth Table** |
|  |

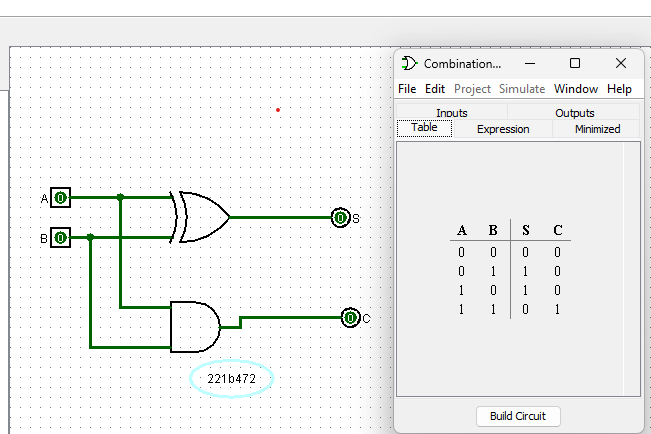
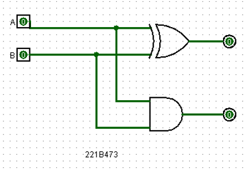
**EXPERIMENT-2**

**Aim: Design of binary adders and subtractors.**

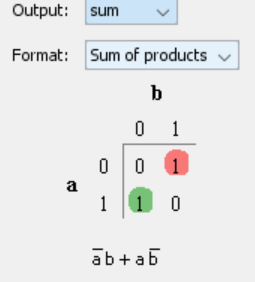
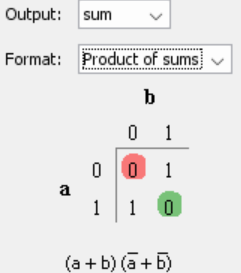
**Exercise#1:** Design and verify half adder and half subtractor shown in Fig. 1 and Fig. 2 using logisim simulator.

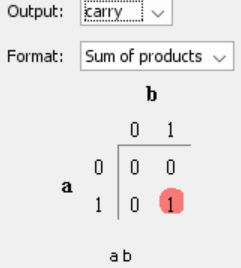
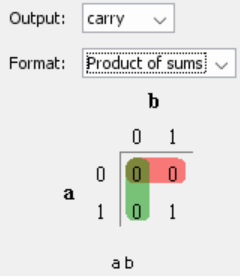
**Half Adder**

**Logic Diagram and Truth Table**

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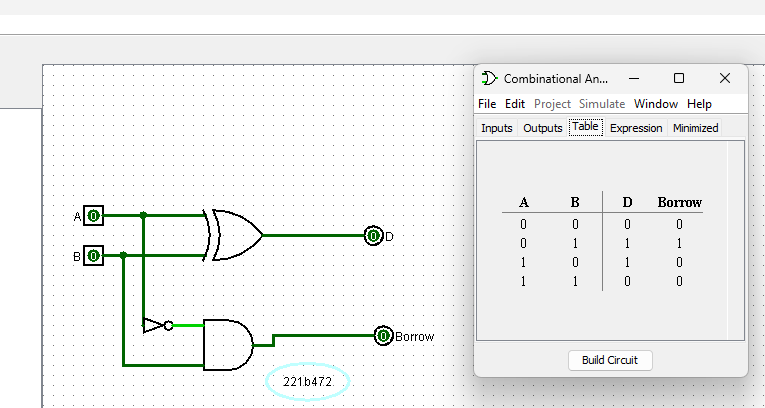
**Karnaugh (K) Map**

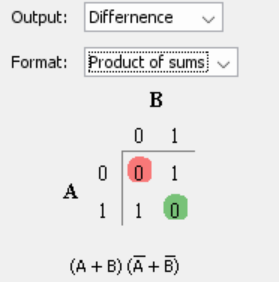
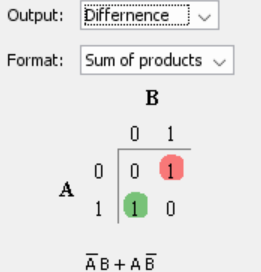
 

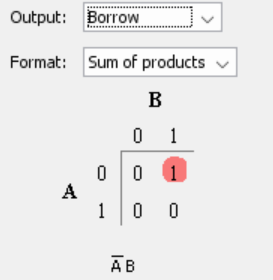
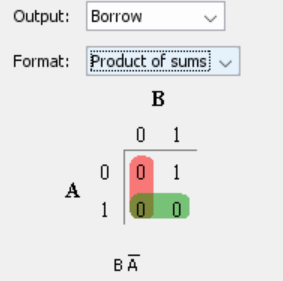
**Half Subtractor**

**Logic Diagram and Truth Table**



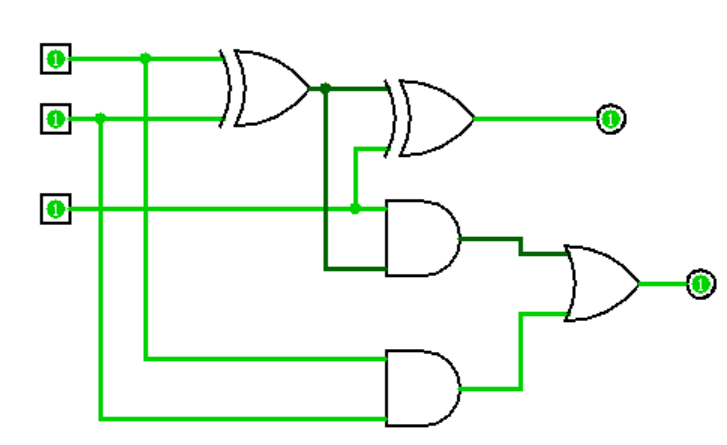
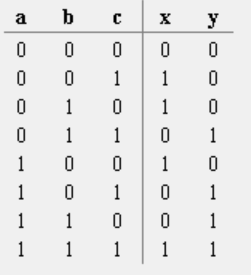
**Karnaugh (K) Map**

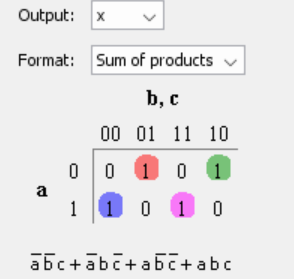
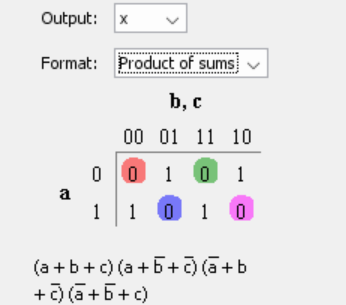
 

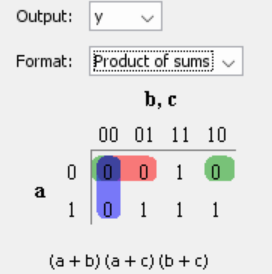
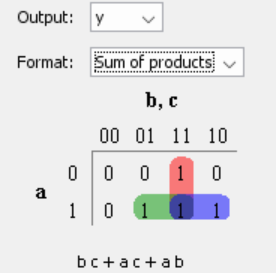
 

**Exercise#2** Design and verify full adder using logisim simulator (i) basic gates only shown in Fig. 3 (ii) by adding half adder (without in-built blocks) as sub circuit similar as shown in Fig. 4.

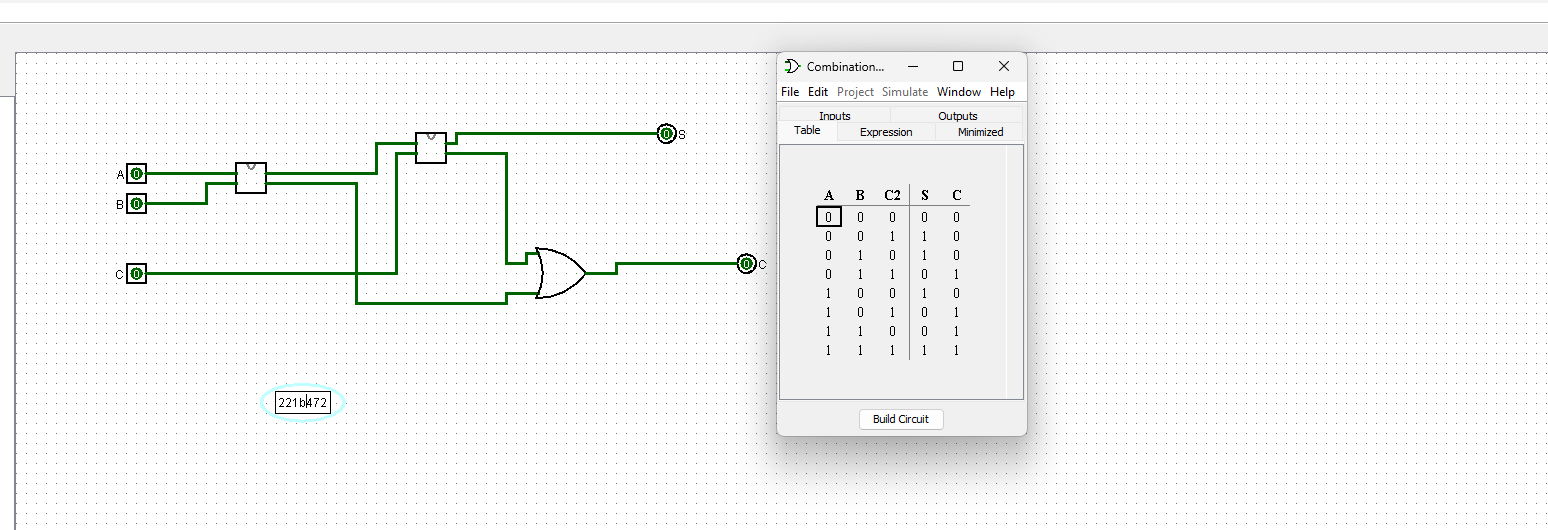
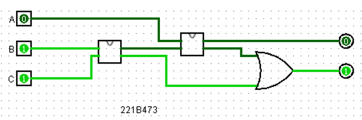
**Logic Diagram and Truth Table**

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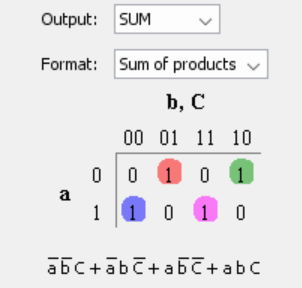
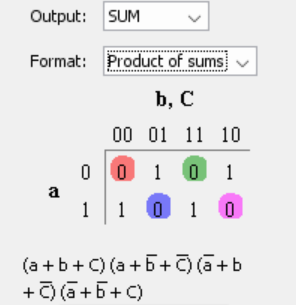
 

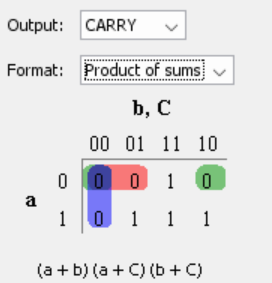
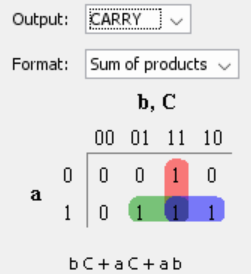
 

**Logic Diagram and Truth Table**

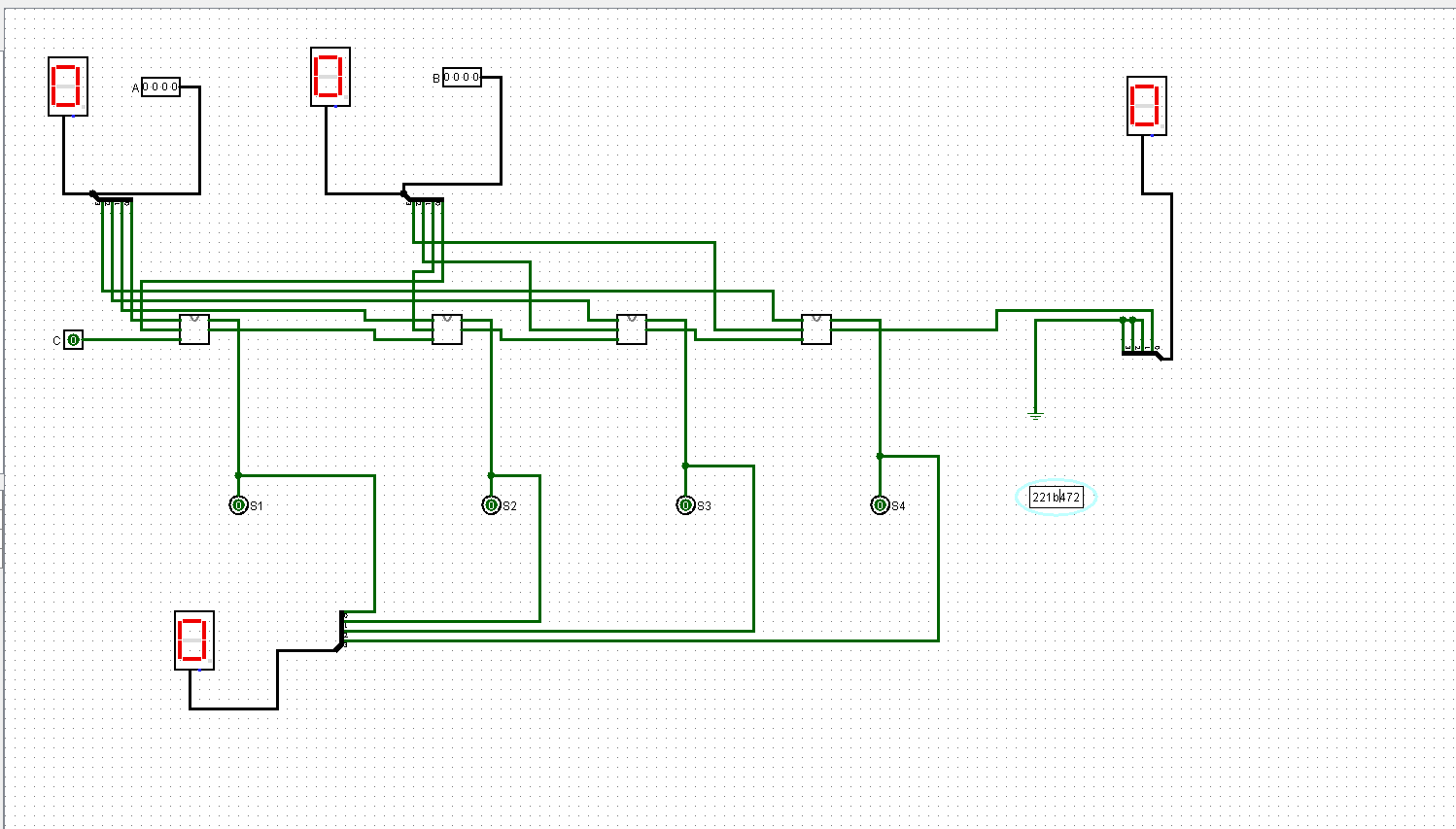


**Karnaugh (K) Map**

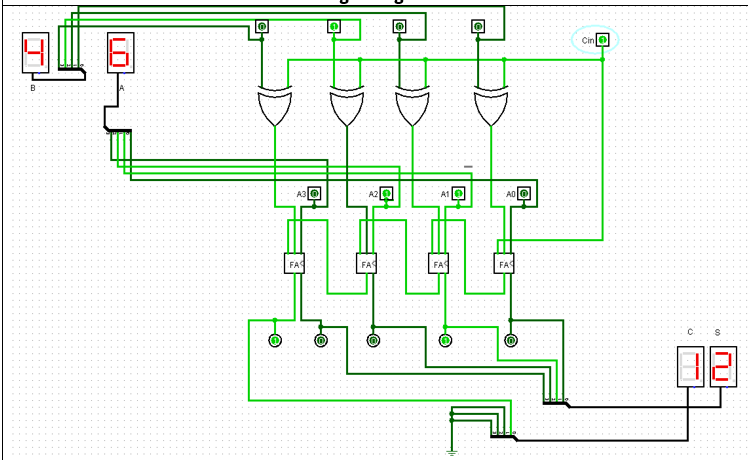
 

**Exercise#3:** Design 4-bit binary adder using one half adder and 3-full adders as shown in Fig. 5. Use half adder and full adders as sub circuits in the design. Display both the input digits; output digit and end carry digit using Hex digit display with splitter available in logisim simulator.



**Exercise#4:** Design 4-bit binary adder-subtractor using full adders as shown in Fig. 6. Use full adders as sub circuits in the design. Display both the input digits, initial carry digit; output digit, and end carry digit using Hex digit display with splitter available in logisim simulator.

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