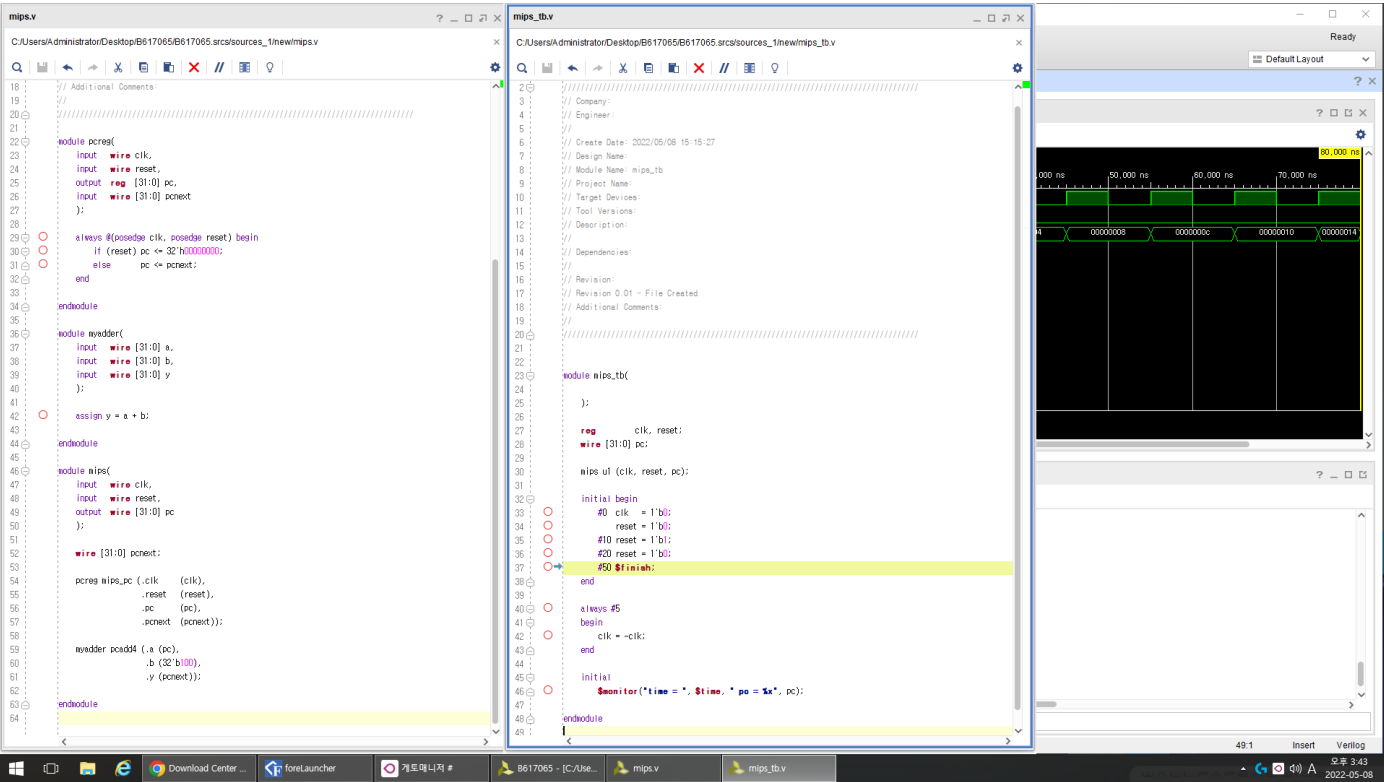


Stimulus



Verilog Design

