

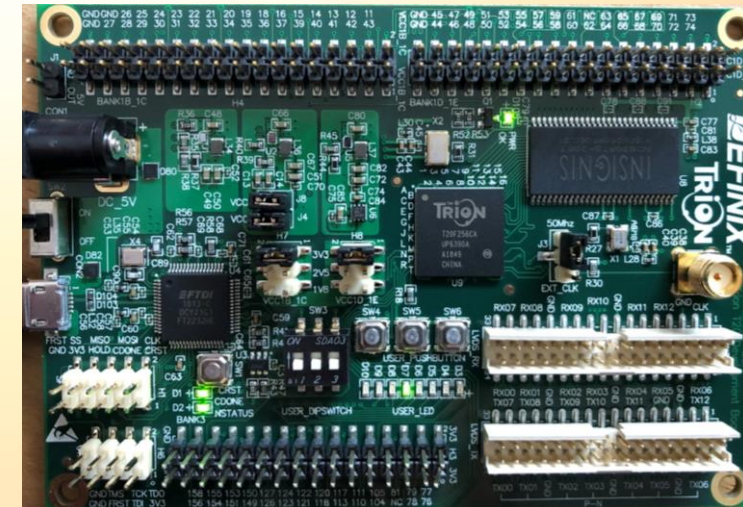


Accelerating Your Innovation

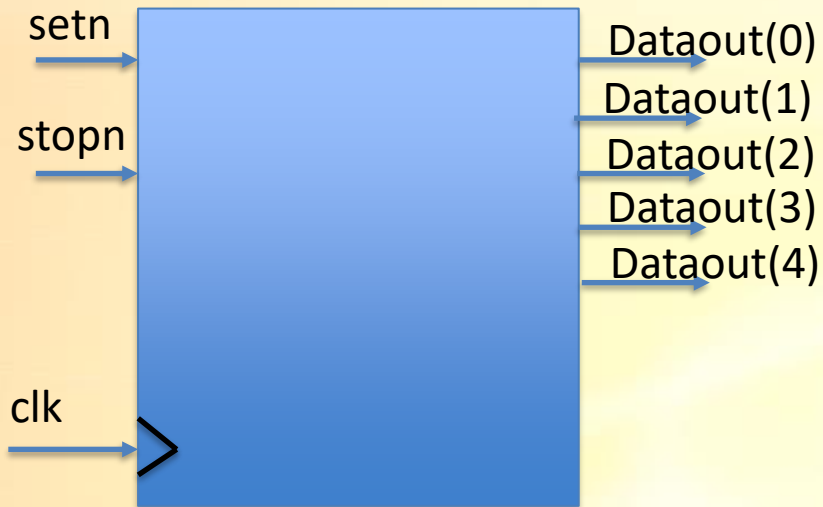
Trion T20 BGA256 LAB

By Harald Werner

Version: 1.0.4



Design (simple up counter with set and stop)



```
counter.vhd X
1  -- smal example design for the Trion 20 B6A256 Efinix Eval Board
2  -- By Harald Werner
3  -- 18.03.2020
4  --
5  library ieee;
6  use ieee.std_logic_1164.all;
7  use ieee.std_logic_unsigned.all;
8
9  entity counter is
10     port ( clk      : in std_logic;           -- clock input. external 74.25MHz clock use GPIOL_75_PLLIN
11           setn      : in std_logic;           -- Set signal, low active; sett all outputs to '1' (LED are low active, means all LEDs msut be OFF) GPIOL_02 SW4
12           stopn     : in std_logic;           -- Stop signal, low active Stop counting GPIOL_04 SW5
13           Dataout   : out std_logic_vector ( 4 downto 0)); -- Output data connected to the LEDs (low active); GPIOR_153,GPIOR_118,GPIOR_117,GPIOR_105,GPIOR_104
14   end counter;
15
16   architecture vers1 of counter is
17
18     signal cnt: std_logic_vector ( 30 downto 0) := (others => '0');
19
20   begin
21
22     cnt_proc : process(clk, setn)
23     begin
24       if setn = '0' then
25         cnt  <= (others => '1');
26         dataout <= (others => '1');
27       elsif clk'event and clk = '1' then
28         if stopn = '0' then
29           cnt <= cnt;
30         else
31           cnt <= cnt +1;
32         end if;
33         Dataout <= cnt(30 downto 26); --For the 75MHz external clock use 30 downto 26
34       end if;
35     end process;
36   end vers1;
37
```

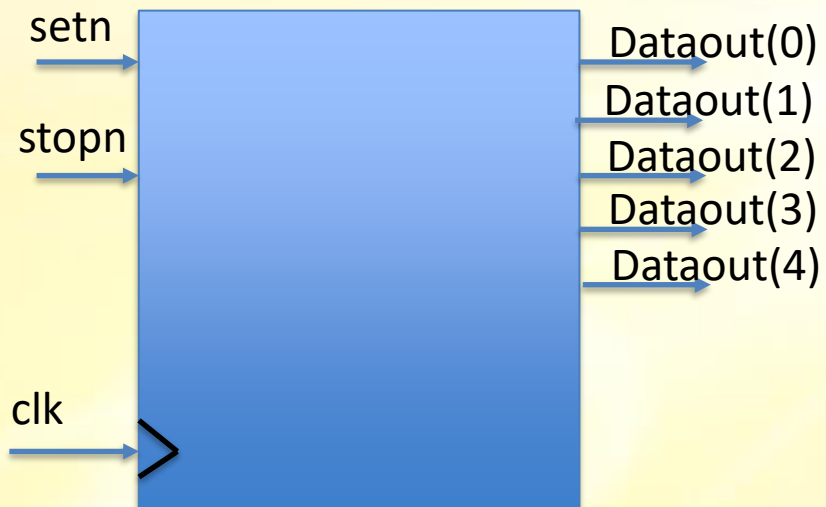
Design / Board connection



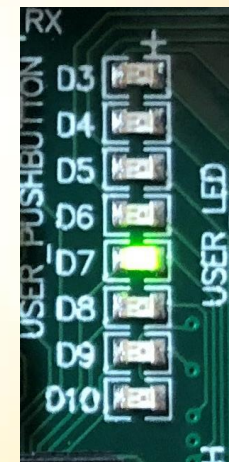
SW4 GPIO_L02

SW5 GPIO_L04

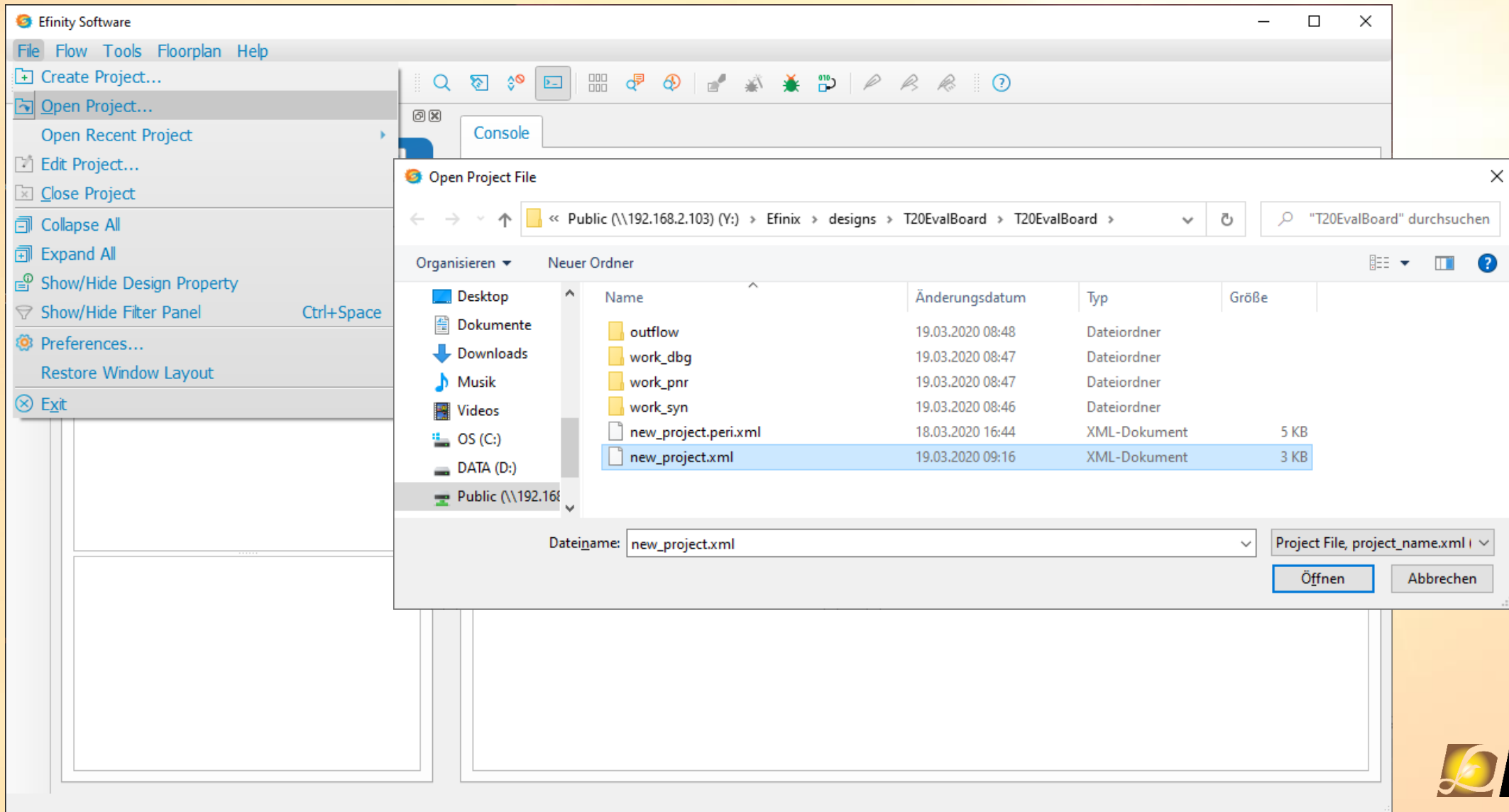
75MHz , GPIO_L75_PLLIN



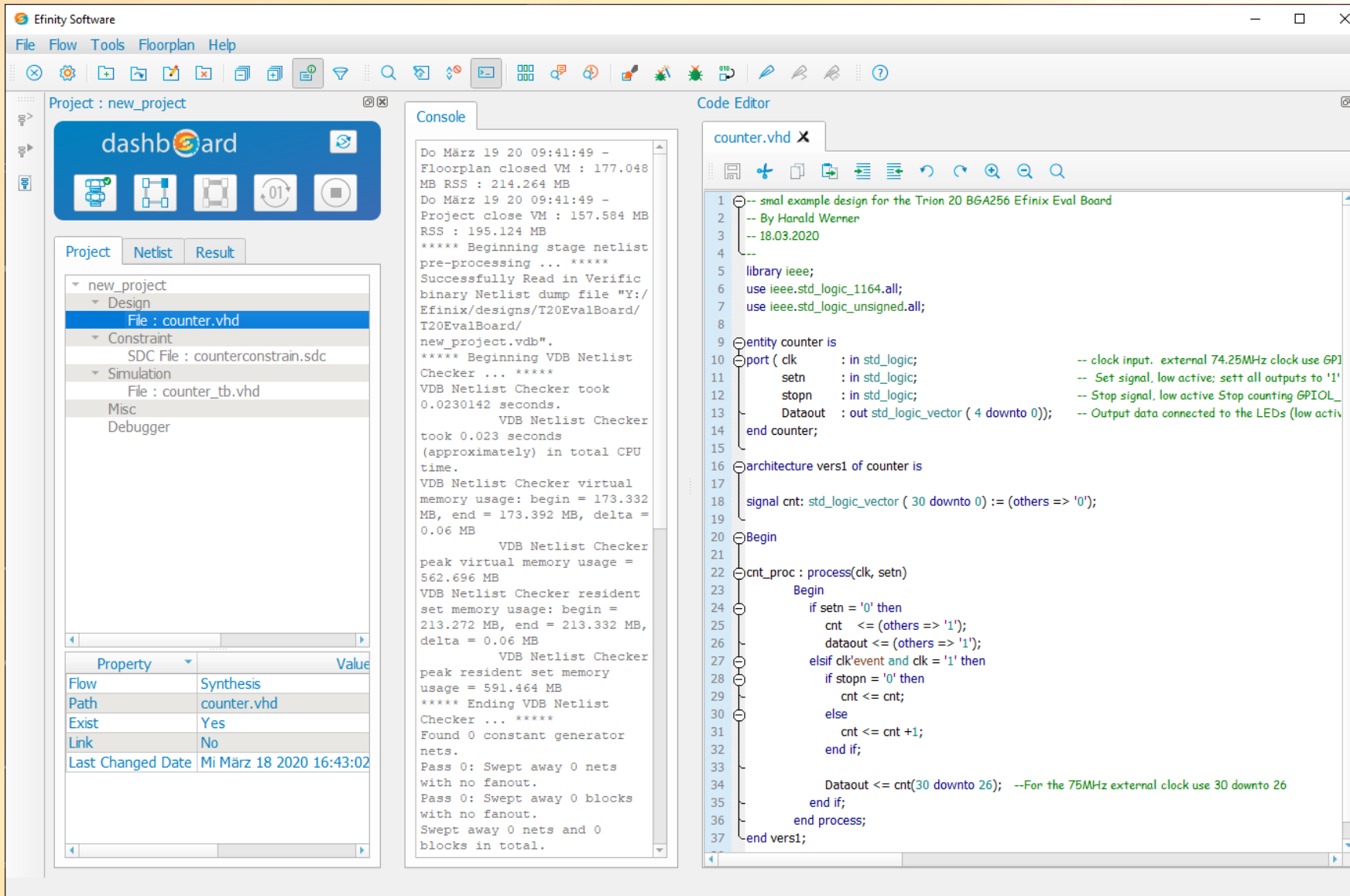
- LED D3 GPIOR_104
- LED D4 GPIOR_105
- LED D6 GPIOR_117
- LED D7 GPIOR_118
- LED D8 GPIOR_153



1. Open Efinity new_project.xml



Double click on counter.vhd



The screenshot displays the Efinity Software IDE interface. On the left, the 'Project' pane shows a tree view of the project files, including 'counter.vhd'. The 'Console' pane in the center shows the output of the compilation process, including messages about the Verilog netlist and VDB Netlist Checker. The 'Code Editor' on the right shows the contents of 'counter.vhd', which is a VHDL file for a counter entity. The code includes a library declaration, port declarations, and a process block for counting.

Project: new_project

dashb

Project | **Netlist** | **Result**

- new_project
 - Design
 - File : counter.vhd
 - Constraint
 - SDC File : counterconstrain.sdc
 - Simulation
 - File : counter_tb.vhd
 - Misc
 - Debugger

Console

```
Do März 19 20 09:41:49 -
Floorplan closed VM : 177.048
MB RSS : 214.264 MB
Do März 19 20 09:41:49 -
Project close VM : 157.584 MB
RSS : 195.124 MB
***** Beginning stage netlist
pre-processing ... *****
Successfully Read in Verific
binary Netlist dump file "Y:/
Efinix/designs/T20EvalBoard/
T20EvalBoard/
new_project.vdb".
***** Beginning VDB Netlist
Checker ... *****
VDB Netlist Checker took
0.0230142 seconds.
VDB Netlist Checker
took 0.023 seconds
(approximately) in total CPU
time.
VDB Netlist Checker virtual
memory usage: begin = 173.332
MB, end = 173.392 MB, delta =
0.06 MB
VDB Netlist Checker
peak virtual memory usage =
562.696 MB
VDB Netlist Checker resident
set memory usage: begin =
213.272 MB, end = 213.332 MB,
delta = 0.06 MB
VDB Netlist Checker
peak resident set memory
usage = 591.464 MB
***** Ending VDB Netlist
Checker ... *****
Found 0 constant generator
nets.
Pass 0: Swept away 0 nets
with no fanout.
Pass 0: Swept away 0 blocks
with no fanout.
Swept away 0 nets and 0
blocks in total.
```

Code Editor

counter.vhd

```
1 -- smal example design for the Trion 20 BGA256 Efinix Eval Board
2 -- By Harald Werner
3 -- 18.03.2020
4
5 library ieee;
6 use ieee.std_logic_1164.all;
7 use ieee.std_logic_unsigned.all;
8
9 entity counter is
10 port ( clk      : in std_logic;          -- clock input. external 74.25MHz clock use GPI
11       setn      : in std_logic;          -- Set signal, low active; sett all outputs to '1'
12       stopn     : in std_logic;          -- Stop signal, low active Stop counting GPIOL_
13       Dataout   : out std_logic_vector ( 4 downto 0)); -- Output data connected to the LEDs (low activ
14 end counter;
15
16 architecture vers1 of counter is
17 signal cnt: std_logic_vector ( 30 downto 0) := (others => '0');
18
19
20 Begin
21 cnt_proc : process(clk, setn)
22 Begin
23 if setn = '0' then
24 cnt <= (others => '1');
25 dataout <= (others => '1');
26
27 elsif clk'event and clk = '1' then
28 if stopn = '0' then
29 cnt <= cnt;
30 else
31 cnt <= cnt +1;
32 end if;
33
34 Dataout <= cnt(30 downto 26); --For the 75MHz external clock use 30 downto 26
35 end if;
36 end process;
37 end vers1;
```

- The counter.vhd will show up in the Code Editor

Double click on the timing constrain counterconstrain.sdc

The counterconstrain.sdc will show up and you can see the 13ns period constrain for the 75MHz clock

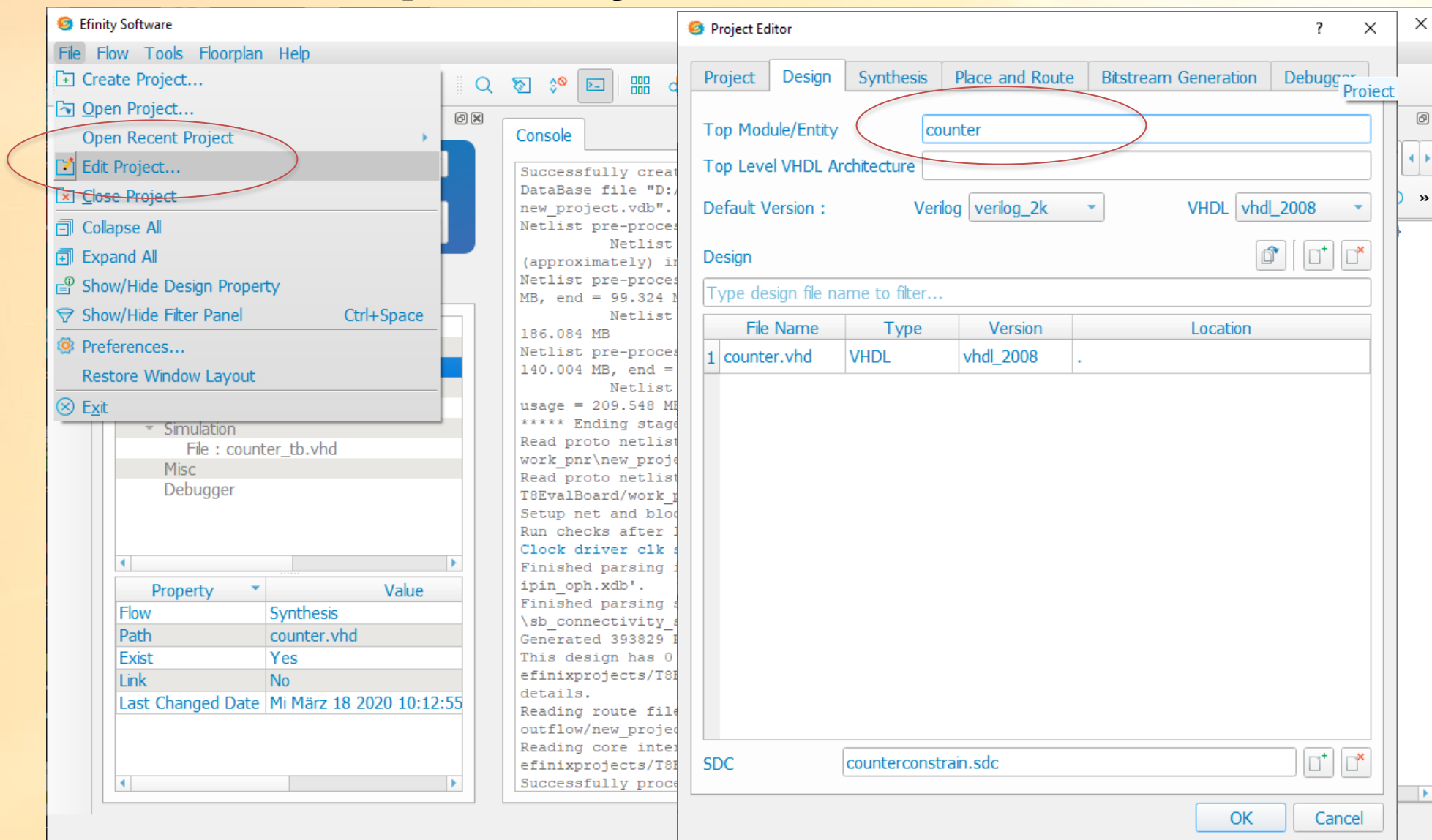
The screenshot displays the Efinity Software interface with three main panels:

- Project Panel (Left):** Shows a tree view for 'new_project'. Under 'Constraint', the file 'counterconstrain.sdc' is highlighted. Below it, a table lists project properties.
- Console (Middle):** Displays the output of the VDB Netlist Checker, including memory usage and timing analysis results.
- Code Editor (Right):** Shows the content of 'counterconstrain.sdc' with the line '1 create_clock -period 13 -name {clk}' circled in red.

Property	Value
Flow	Timing Analysis
Path	counterconstrain.sdc
Exist	Yes
Link	No
Last Changed Date	Mi März 18 2020 16:36:28

```
1 create_clock -period 13 -name {clk}
```


Set the top entity name



Enter counter
to top
Module/Entity
and click OK

Run the whole flow

The screenshot displays the Efinity Software interface. The top menu bar includes File, Flow, Tools, Floorplan, and Help. The main workspace is divided into three panes. The left pane, titled 'Project : new_project', shows a tree view with folders for Design, Constraint, Simulation, Misc, and Debugger. The middle pane, titled 'Console', displays the output of the automated flow process. The right pane shows a 'dashboard' with icons for various tools. At the bottom, a status bar indicates 'Running automated flow starting from synthesis...routing is in progress...'

Project : new_project

dashb

Project Netlist Result

new_project

- Design
 - File : counter.vhd
- Constraint
 - SDC File : counterconstrain.sdc
- Simulation
 - File : counter_tb.vhd
- Misc
- Debugger

Property	Value
Flow	Timing Analysis
Path	counterconstrain.sdc
Exist	Yes
Link	No
Last Changed Date	Mi März 18 2020 16:36:28

Console

```
Completed placement consistency check successfully.

Placement estimated critical path delay: 4.18204 ns

Successfully created FPGA place file 'Y:/Efinix/designs/T20EvalBoard/
T20EvalBoard/outflow/new_project.place'
Placement took 3.6546 seconds.
Placement took 3.653 seconds (approximately) in total CPU time.
Placement virtual memory usage: begin = 15.996 MB, end = 21.392 MB, delta =
5.396 MB
Placement peak virtual memory usage = 124.464 MB
Placement resident set memory usage: begin = 23.552 MB, end = 31.788 MB, delta =
8.236 MB
Placement peak resident set memory usage = 131.96 MB
***** Ending stage placement *****

Efinix FPGA Placement and Routing.
Version: 2019.3.272.5.3
Compiled: Feb 24 2020.

Copyright (C) 2013 - 2019 Efinix Inc. All rights reserved.

The Tool Is Based on VPR of University of Toronto,
a free open source code under MIT license.

Running Placement and Routing for Family "Trion", Device "T20F256" ...

***** Beginning stage routing graph generation ... *****
Finished parsing ipin pattern file 'C:/Efinity/2019.3/arch/./ipin_oph.xdb'.
Finished parsing switch_block file 'C:/Efinity/2019.3/arch/./
sb_connectivity_subset.xdb'.
```

Running automated flow starting from synthesis...routing is in progress...

- If the Automated flow button is grayed out click on the button to activate the automated flow.



- Click on the synthesis icon and the flow will run automatically



Assign the top level Signals to Pins.

1. Open Interface Designer

The screenshot displays the Efinity Software Interface Designer window. The top menu bar includes File, Flow, Tools, Floorplan, and Help. The toolbar contains various icons for file operations, design manipulation, and simulation. The main workspace is divided into three panes: Project, Netlist, and Result. The Project pane shows a tree view of the project structure, including Interface, Simulation, Synthesis, Placement, Routing, Bitstream, and Debugger. The Netlist pane displays a table of Core Resource usage.

Core Resource	
Inputs	3 / 470
Outputs	5 / 595
Clocks	1 / 16
Logic Elements	38 / 19728
Memory Blocks	0 / 204
Multipliers	0 / 36
Interface	

The Result pane shows the console output, which includes the following text:

```
Clock driver clk should use the dedicated clock pad.
Finished parsing ipin pattern file 'C:/Efinity/2019.3/arch/./ipin_oph.xdb'.
Finished parsing switch_block file 'C:/Efinity/2019.3/arch/./sb_connectivity_subset.xdb'.
Generated 1169277 RR nodes and 4443471 RR edges
This design has 0 global control net(s). See Y:/Efinity/designs/T20EvalBoard/
T20EvalBoard/outflow/new_project.pnr.rpt for details.
Reading route file, Y:/Efinity/designs/T20EvalBoard/T20EvalBoard/outflow/
new_project.route
Reading core interface constraints from 'Y:/Efinity/designs/T20EvalBoard/
T20EvalBoard/outflow/new_project.interface.csv'.
Successfully processed interface constraints file "Y:/Efinity/designs/
T20EvalBoard/T20EvalBoard/outflow/new_project.interface.csv".

SDC file 'Y:/Efinity/designs/T20EvalBoard/T20EvalBoard/counterconstrain.sdc'
parsed successfully.
1 clocks (including virtual clocks), 0 inputs and 0 outputs were constrained.

NOTE: The timing data is not final.

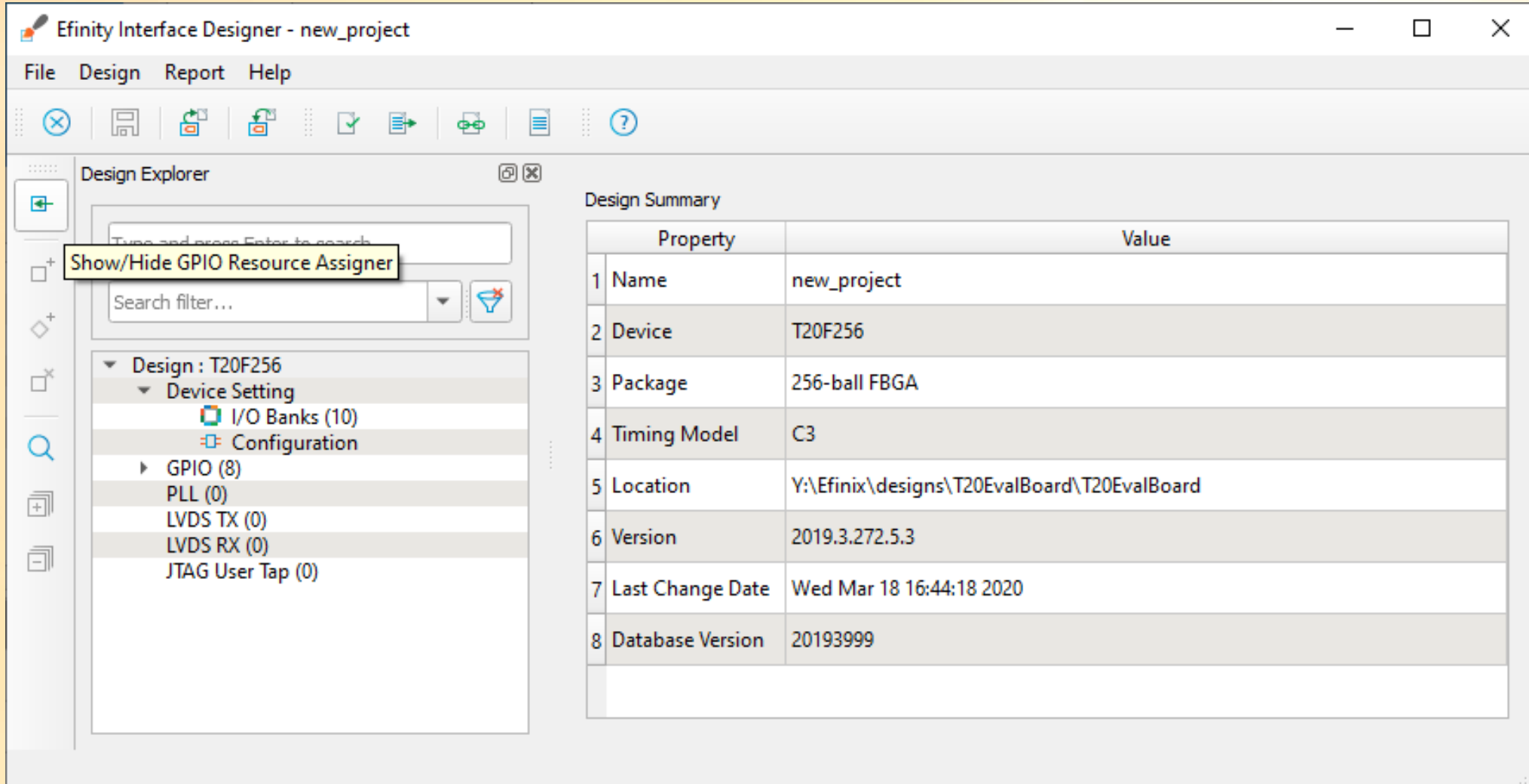
Maximum possible analyzed clocks frequency
Clock Name      Period (ns)   Frequency (MHz)   Edge
clk              4.415          226.484          (R-R)

Geomean max period: 4.415

Launch Clock     Capture Clock   Constraint (ns)   Slack (ns)       Edge
clk              clk              13.000           8.585            (R-R)

Do März 19 20 09:46:10 - Flow data refreshed. Elapsed time = 0m 6.468s VM :
485.324 MB RSS : 516.472 MB
Do März 19 20 09:46:10 - Running automated flow starting from synthesis done.
Total duration = 1m 29.916s
```

Show GPIO Resource Assigner



The screenshot shows the Efinix Interface Designer - new_project window. The Design Explorer on the left lists the design hierarchy: Design : T20F256, Device Setting, I/O Banks (10), Configuration, GPIO (8), PLL (0), LVDS TX (0), LVDS RX (0), and JTAG User Tap (0). A yellow callout box points to the 'Show/Hide GPIO Resource Assigner' button in the Design Explorer. The Design Summary table on the right provides details about the project.

Design Explorer

Type and press Enter to search

Search filter...

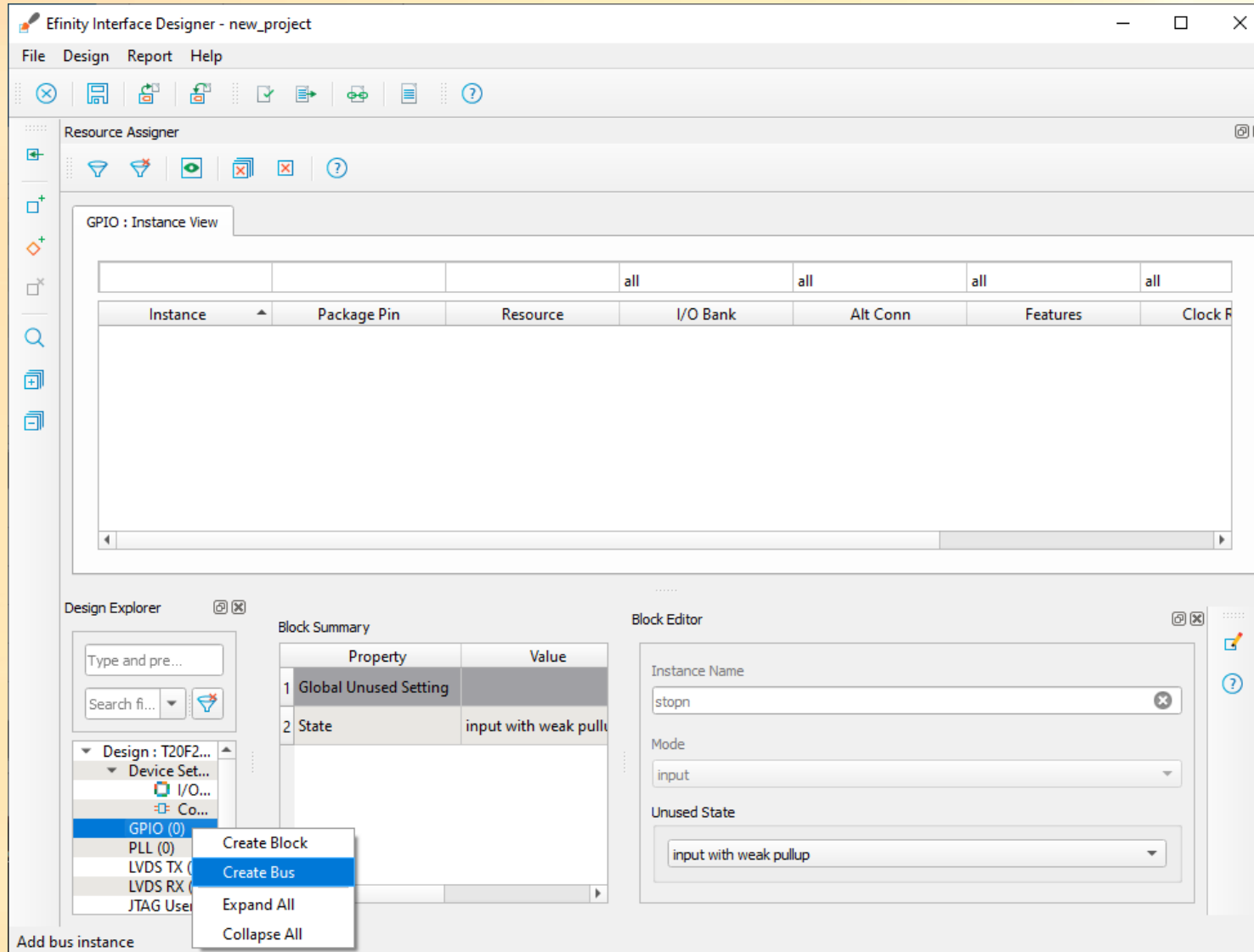
Design : T20F256

- Device Setting
 - I/O Banks (10)
 - Configuration
 - GPIO (8)
 - PLL (0)
 - LVDS TX (0)
 - LVDS RX (0)
 - JTAG User Tap (0)

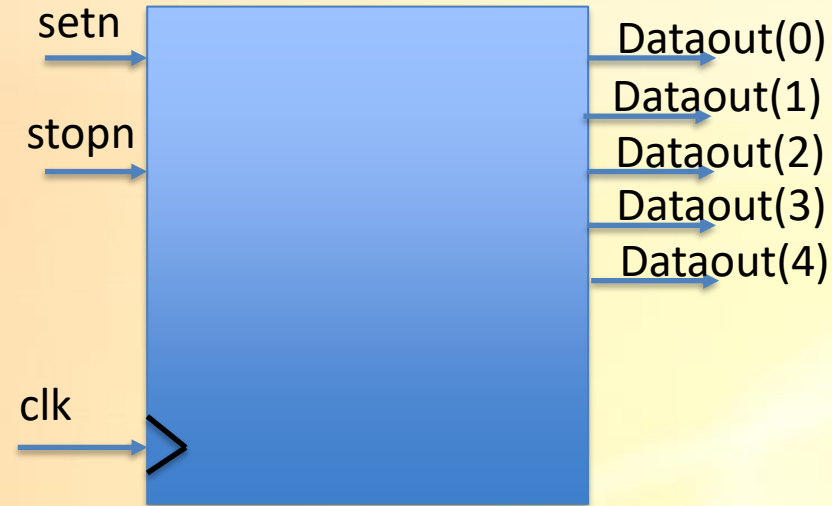
Design Summary

	Property	Value
1	Name	new_project
2	Device	T20F256
3	Package	256-ball FBGA
4	Timing Model	C3
5	Location	Y:\Efinix\designs\T20EvalBoard\T20EvalBoard
6	Version	2019.3.272.5.3
7	Last Change Date	Wed Mar 18 16:44:18 2020
8	Database Version	20193999

Select GPIO, RMB, Create Bus



Create a Output BUS Dataout(4 downto 0)



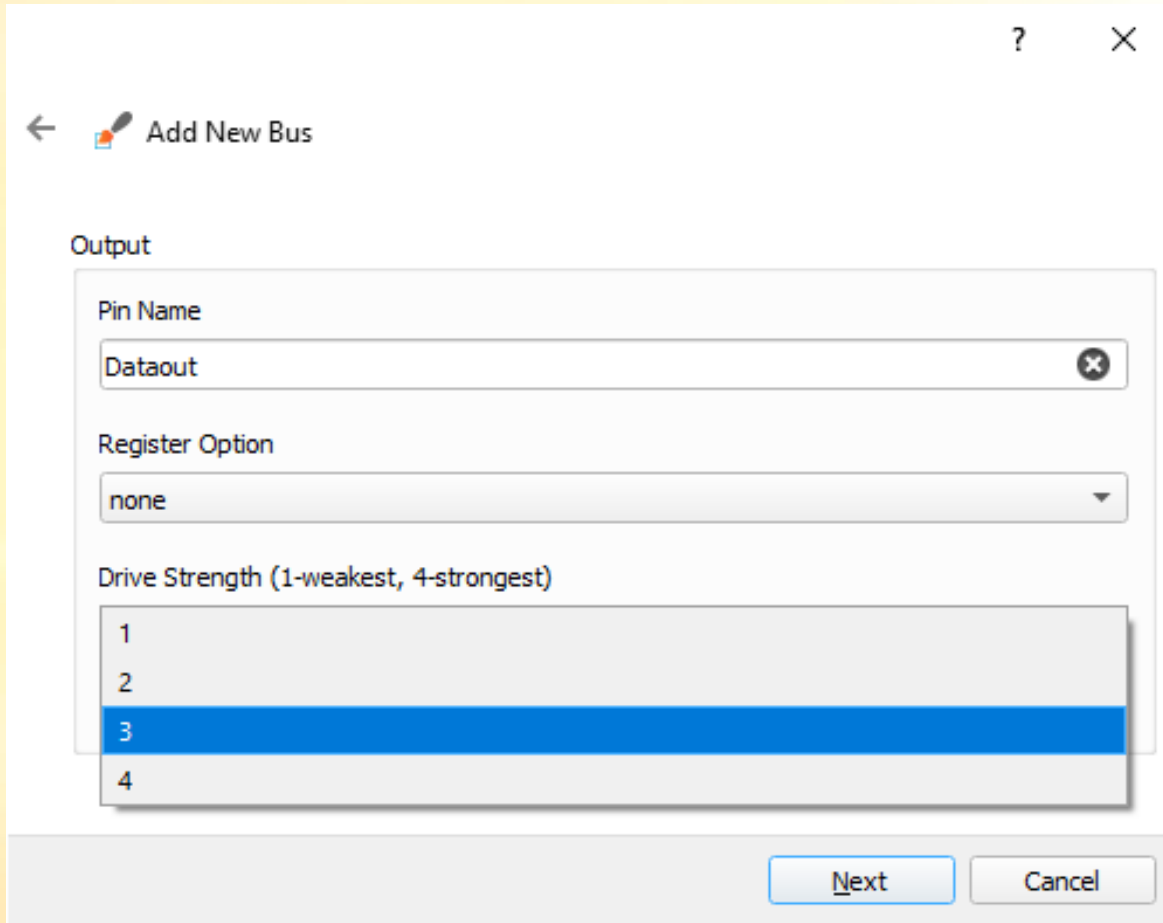
The screenshot shows a dialog box titled 'Add New Bus'. It contains the following fields and options:

- Name:** A text field containing 'Dataout'.
- MSB:** A numeric field containing '4'.
- LSB:** A numeric field containing '0'.
- Mode:** A dropdown menu with three options: 'input', 'output' (which is highlighted in blue), and 'inout'.

At the bottom right of the dialog box are two buttons: 'Next' and 'Cancel'.

Name: Dataout
MSB: 4
LSB: 0
Mode: output
Click Next

Set drive strength to 3; click Next



?

×

← Add New Bus

Output

Pin Name

Dataout

Register Option

none

Drive Strength (1-weakest, 4-strongest)

1

2

3


4

Next

Cancel

Click Finish

? ×

←  Add New Bus

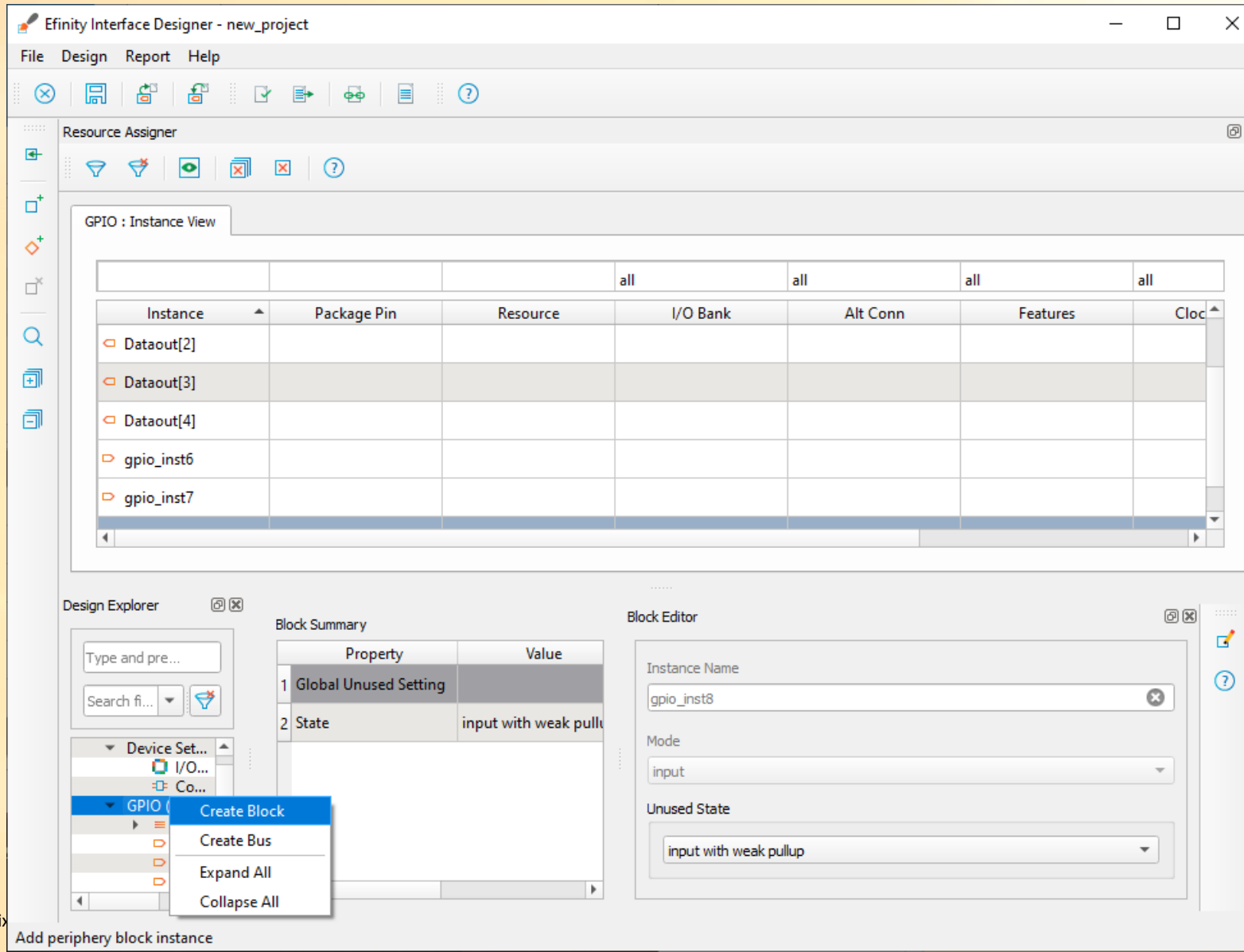
A new bus will be created with these properties

	Property	Value
1	Bus Name	Dataout
2	MSB	4
3	LSB	0
4	Mode	output
5	Output	
6	Pin Name	Dataout
7	Constant Output	none
8	Drive Strength	3
9	Enable Slew Rate	false
10	Register Option	none

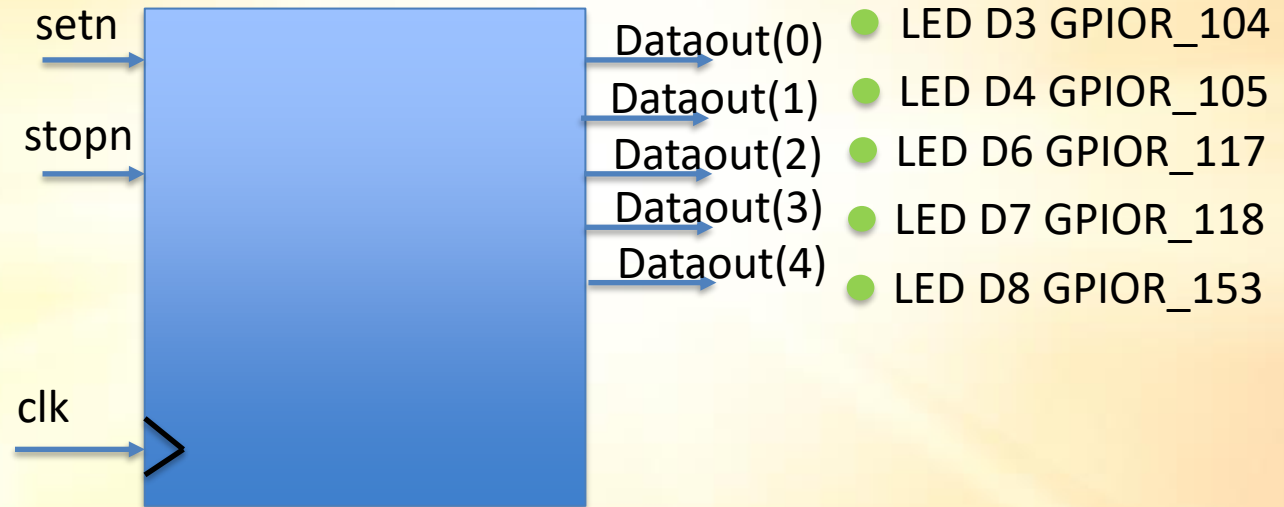
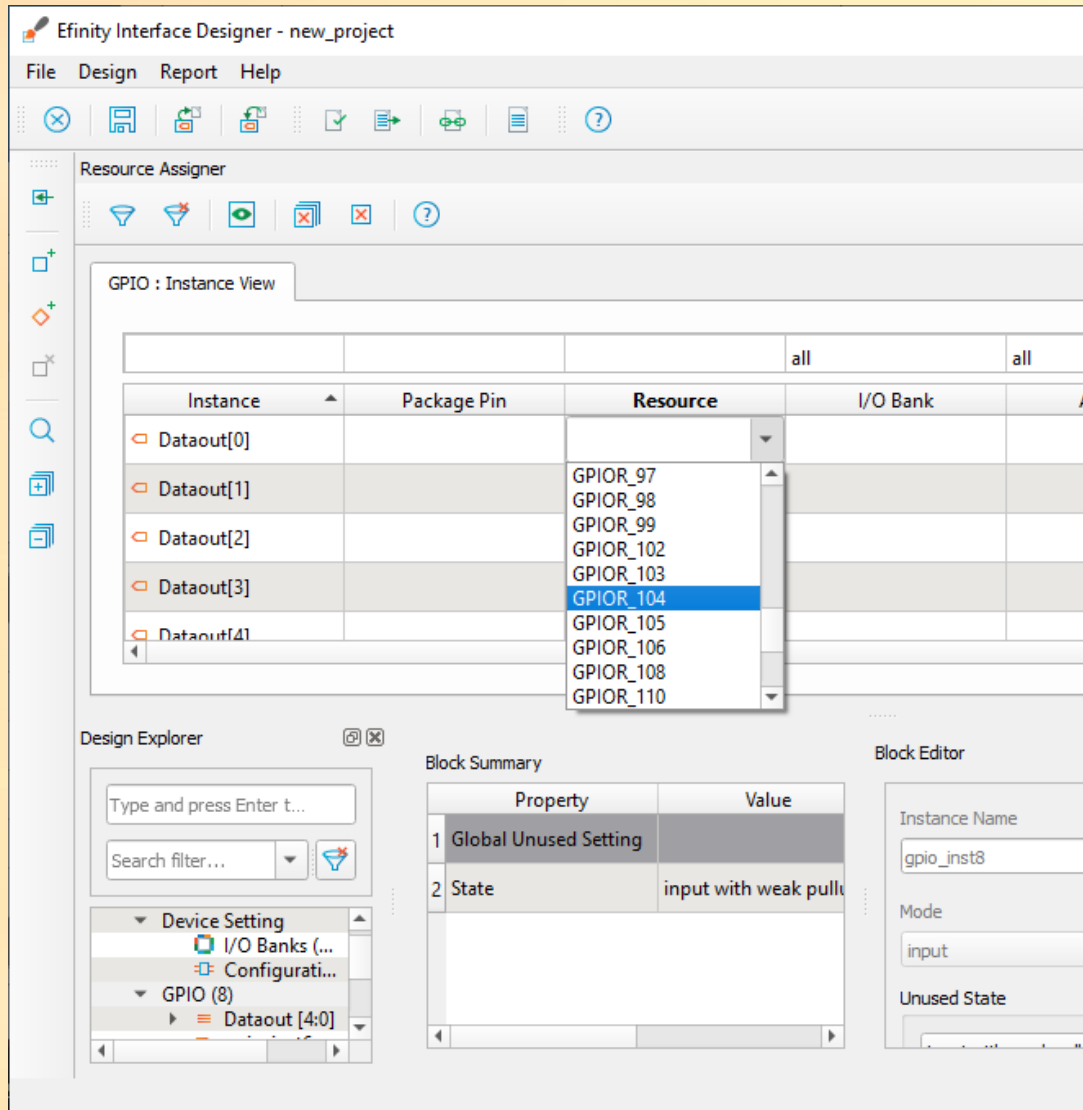
Finish Cancel

Adding the additional Pins clk, stopn, setn

Select GPIO
Create Block
Select GPIO
Create Block
Select GPIO
Create Block

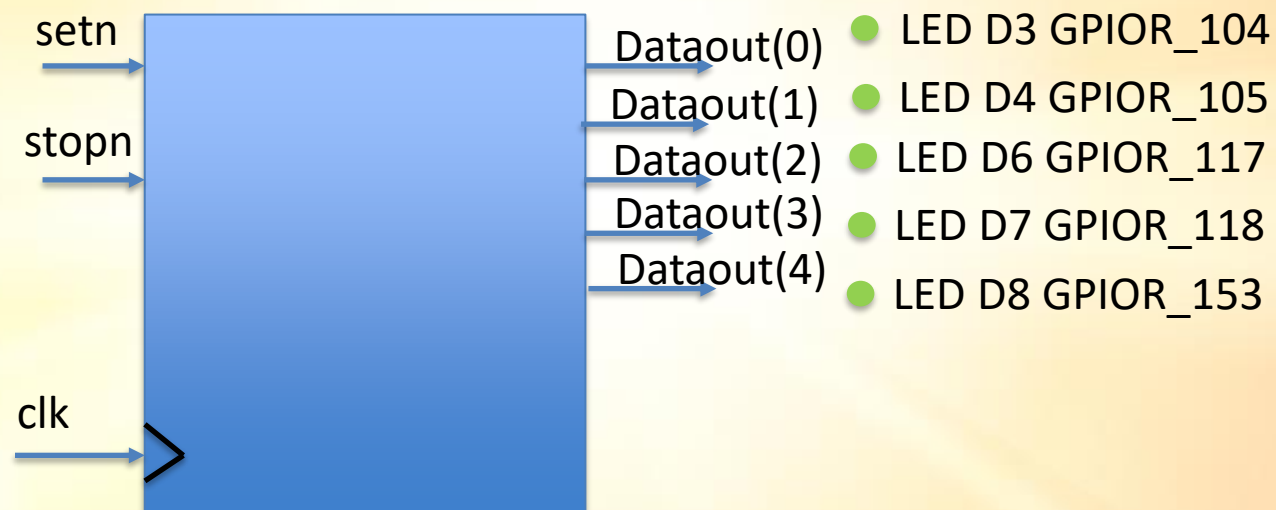
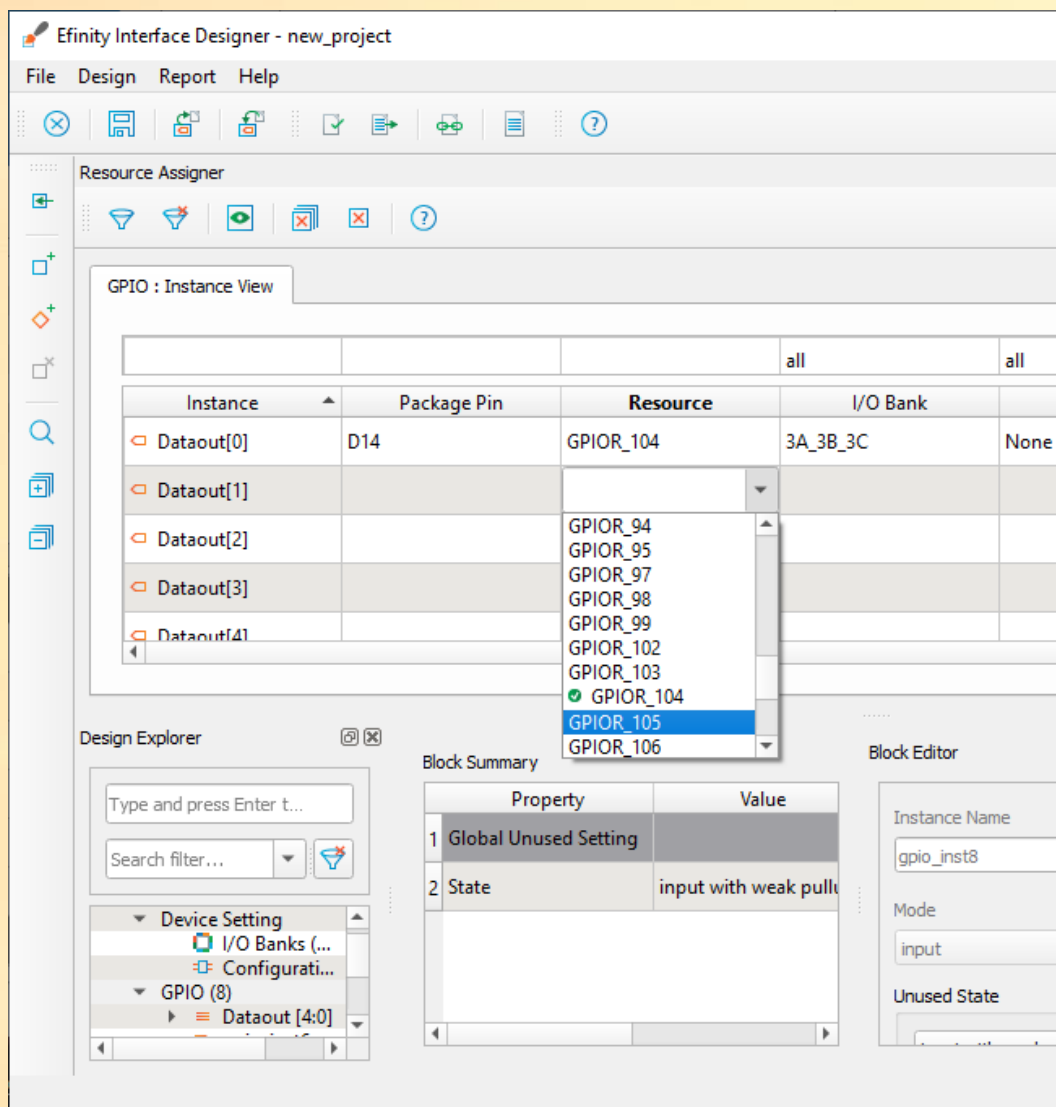


Select GPIO: Instance View Dataout[0]->Resource



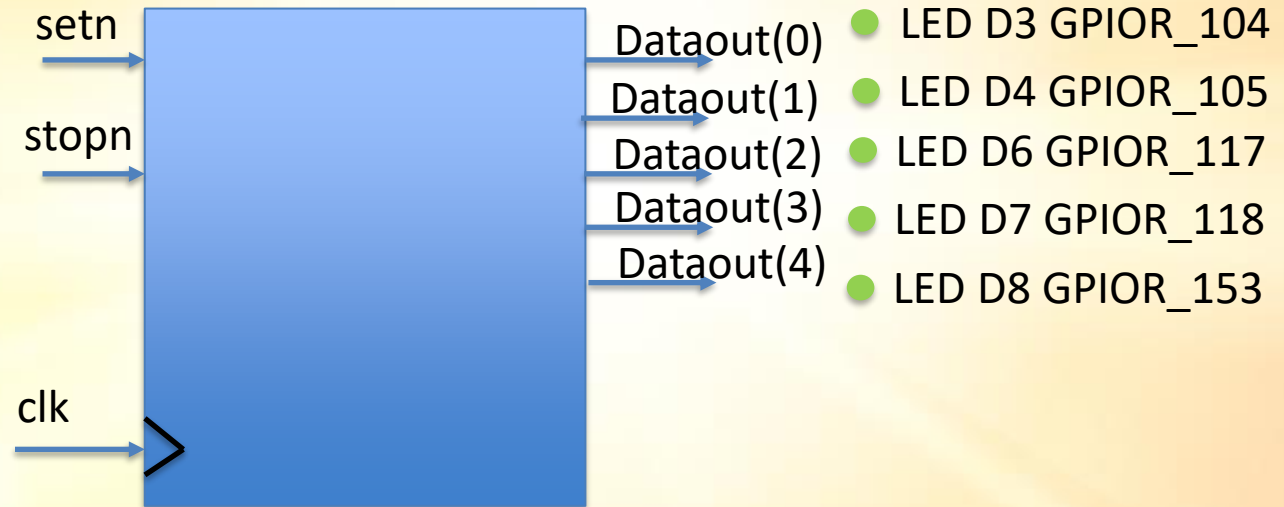
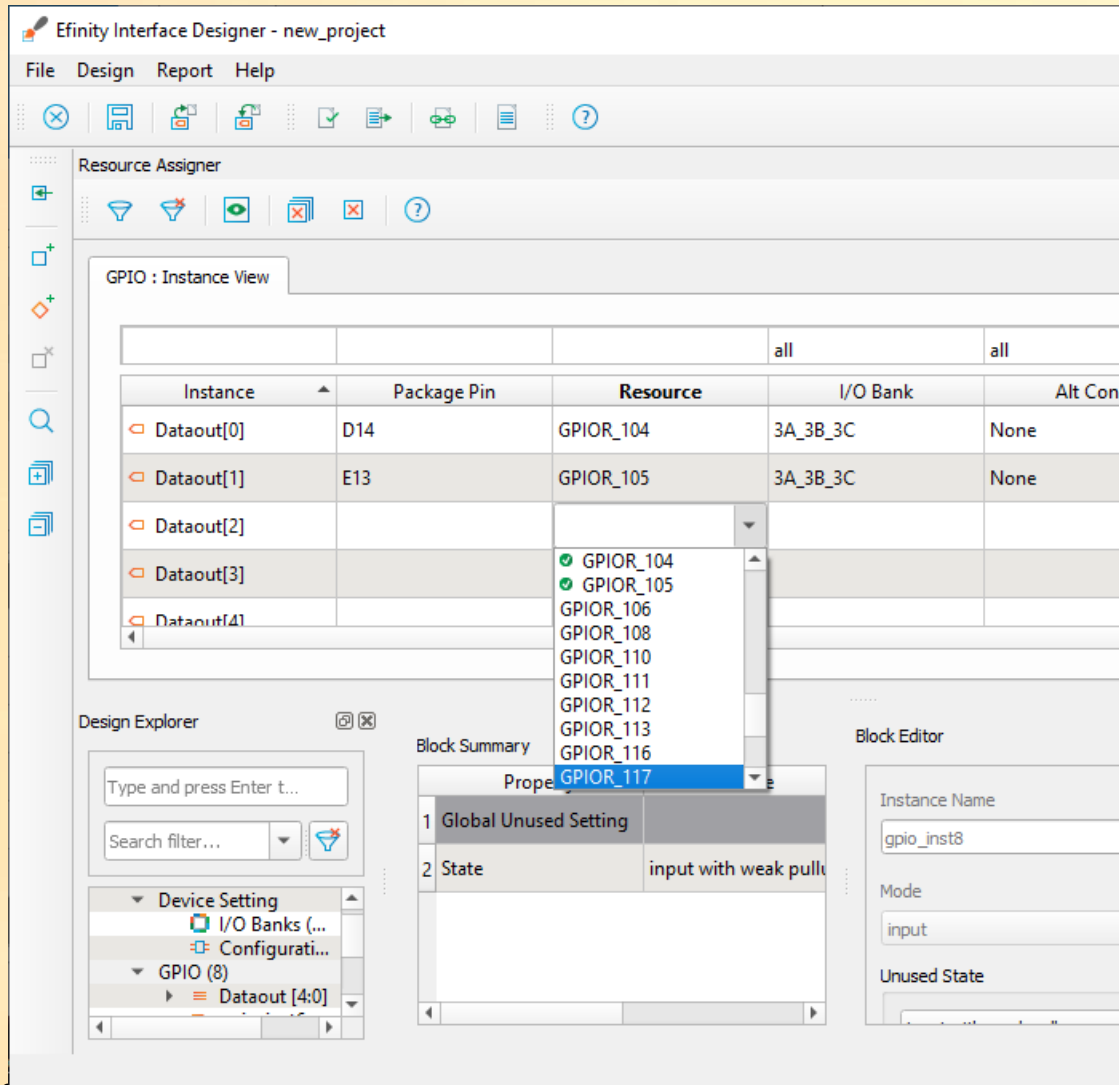
Dataout[0] -> GPIOR_104

Select GPIO: Instance View Dataout[1]->Resource



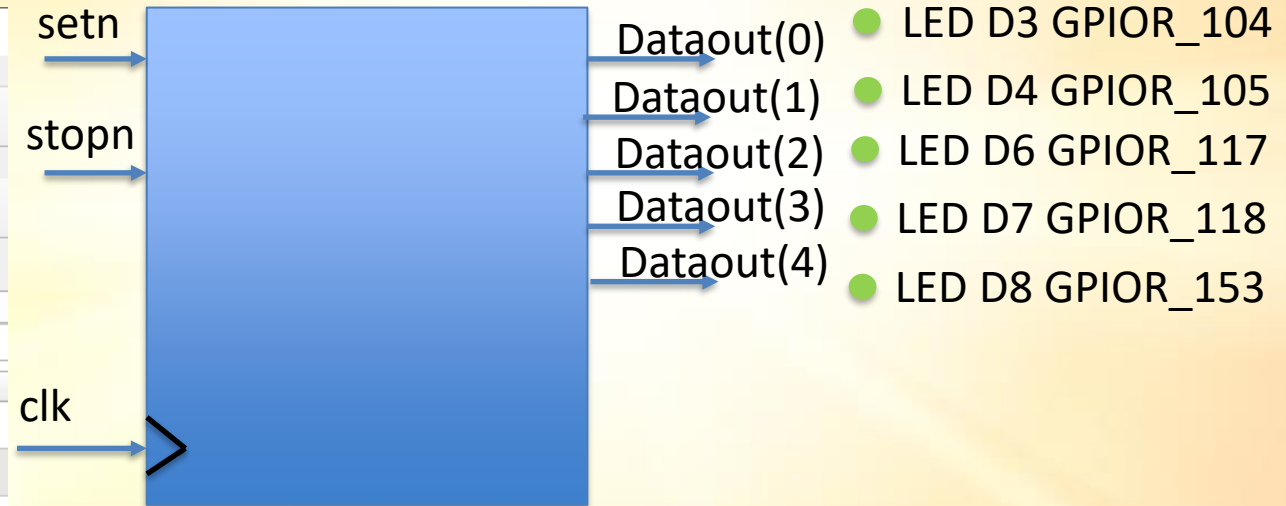
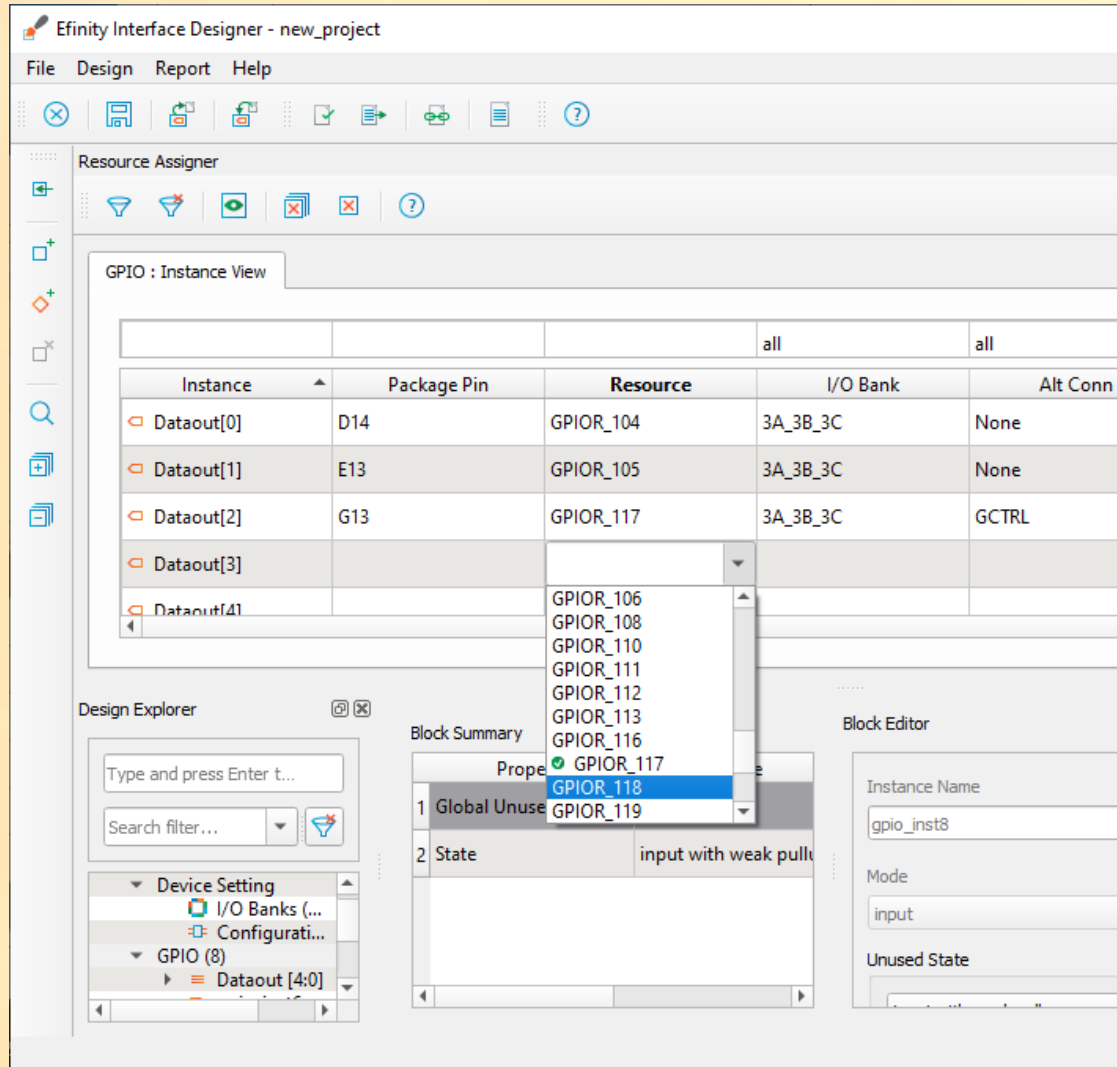
Dataout[1] -> GPIOR_105

Select GPIO: Instance View Dataout[2]->Resource



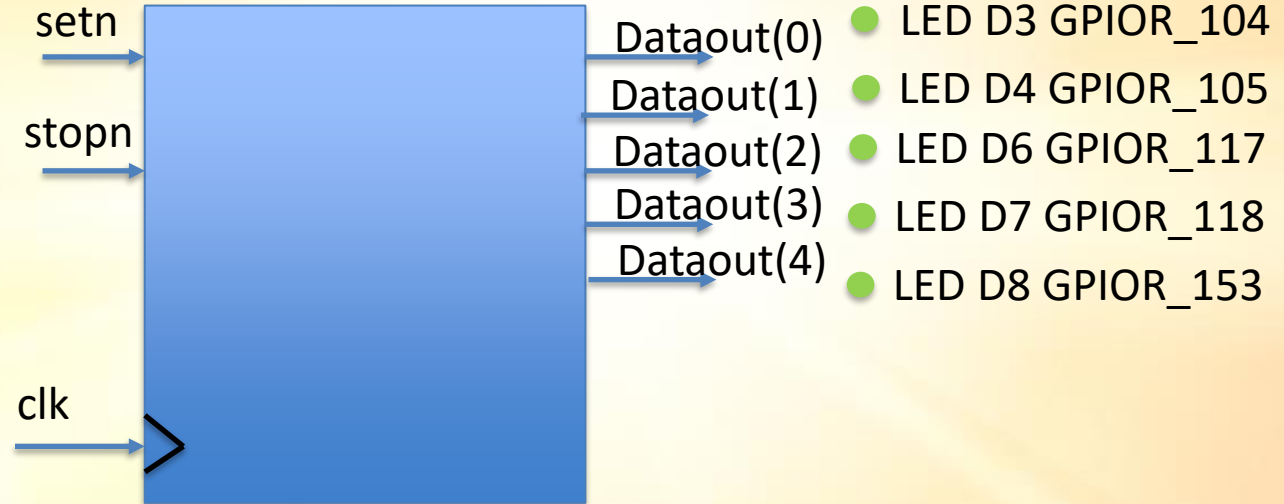
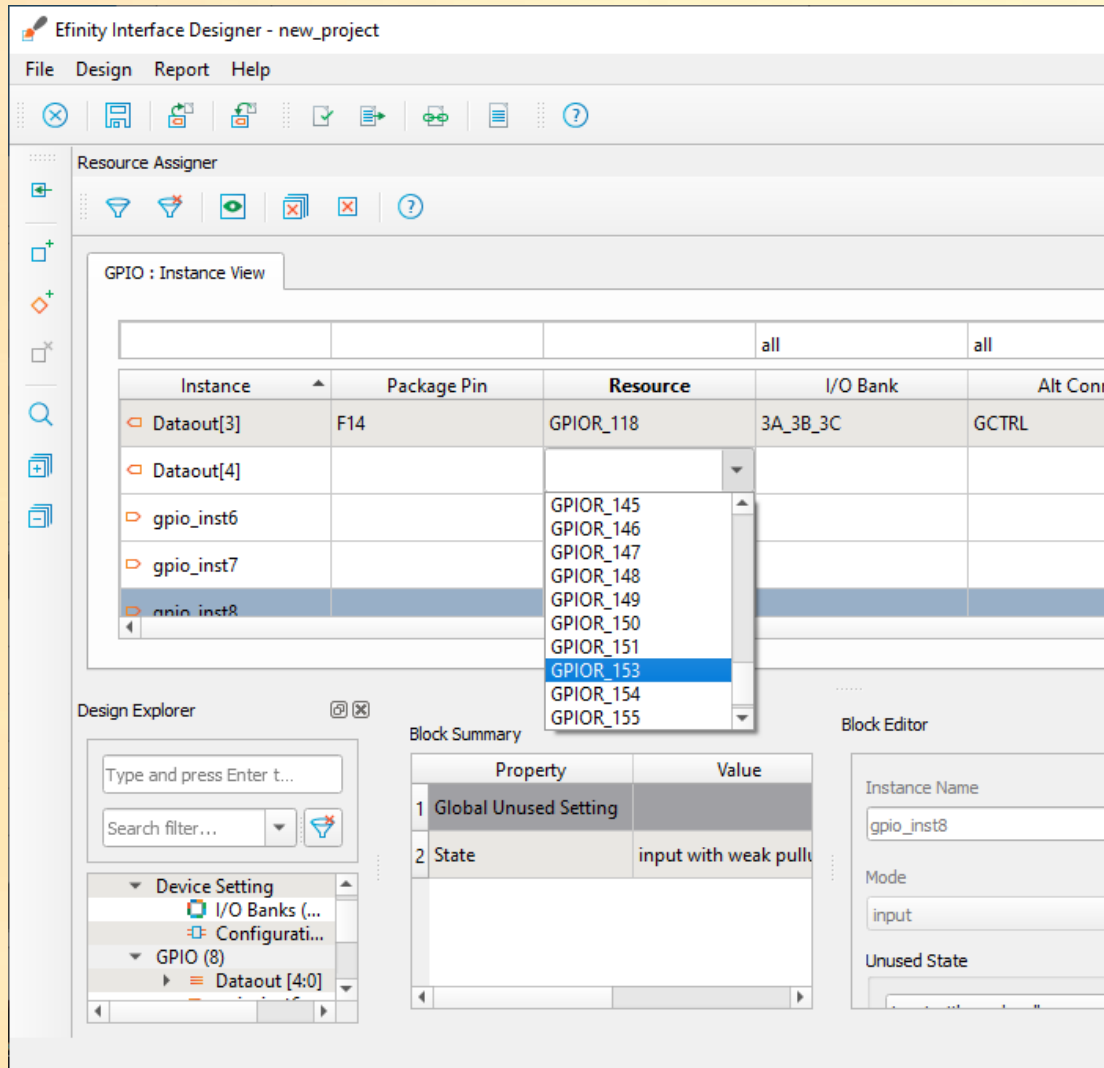
Dataout[2] -> GPIOR_117

Select GPIO: Instance View Dataout[3]->Resource



Dataout[3] -> GPIOR_118

Select GPIO: Instance View Dataout[4]->Resource



- LED D3 GPIOR_104
- LED D4 GPIOR_105
- LED D6 GPIOR_117
- LED D7 GPIOR_118
- LED D8 GPIOR_153

Dataout[4] -> GPIOR_153

Change the name from the remaining Inputs: clk

Select gpio_inst6
Enter name in the
Block Editor clk
and press enter !

The screenshot shows the Efinity Interface Designer interface. The top window is the Resource Assigner, displaying a table of GPIO instances. The bottom window is the Block Editor, showing the configuration for the selected instance, gpio_inst6.

Resource Assigner - GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region
Dataout[3]	F14	GPOR_118	3A_3B_3C	GCTRL	DDIO	R1
Dataout[4]	N14	GPOR_153	3D_3E	None	DDIO	R0
gpio_inst6						
gpio_inst7						
gpio_inst8						

Design Explorer

- Device Setting
 - I/O Banks (...)
 - Configurati...
 - GPIO (8)
 - Dataout [4:0]
 - gpio_inst6:
 - gpio_inst7:
 - gpio_inst8:
 - PLL (0)
 - LVDS TX (0)
 - LVDS RX (0)
 - JTAG User Tap (0)

Block Summary

Property	Value
1 Instance Name	gpio_inst6
2 GPIO Resource	
3 Mode	input
4 Unused State	NA
5 Input	
6 Pin Name	gpio_inst6
7 Connection Type	normal
8 Register Option	none

Block Editor

Instance Name: clk

Mode: gpio_inst6

Input

Pin Name: gpio_inst6

Connection Type: normal

setn

The screenshot shows the Efinity Interface Designer interface. The main window is titled "Efinity Interface Designer - new_project". The "Resource Assigner" tab is active, displaying a table of GPIO instances. The "GPIO : Instance View" table is as follows:

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region
Dataout[3]	F14	GPIOR_118	3A_3B_3C	GCTRL	DDIO	R1
Dataout[4]	N14	GPIOR_153	3D_3E	None	DDIO	R0
clk						
gpio_inst7						
gpio_inst8						

The "Design Explorer" on the left shows the project hierarchy. Under "GPIO (8)", "gpio_inst7" is selected and circled in red. The "Block Summary" table in the center shows the properties of the selected instance:

Property	Value
1 Instance Name	gpio_inst7
2 GPIO Resource	
3 Mode	input
4 Unused State	NA
5 Input	
6 Pin Name	gpio_inst7
7 Connection Type	normal

The "Block Editor" on the right shows the configuration for the selected instance. The "Instance Name" field is circled in red and contains the text "setn". The "Mode" is set to "input". The "Pin Name" field contains "gpio_inst7".

Select gpio_inst7
Enter name in the
Block Editor setn
and press enter !

stopn

Select gpio_inst8
Enter name in the
Block Editor stopn
and press enter !

The screenshot shows the Efinity Interface Designer software interface. The top window is titled "Efinity Interface Designer - new_project" and has a menu bar with "File", "Design", "Report", and "Help". Below the menu is a toolbar with various icons. The main workspace is divided into several panels:

- Resource Assigner:** This panel shows a table of GPIO instances. The "GPIO : Instance View" tab is active. The table has columns for Instance, Package Pin, Resource, I/O Bank, Alt Conn, Features, and Clock Region. The instance "gpio_inst8" is highlighted in blue.
- Design Explorer:** This panel shows a tree view of the project structure. Under "Device Setting", there is a "GPIO (8)" folder, which contains "Dataout [4:0]", "clk:", "setn:", and "gpio_inst8:". The "gpio_inst8:" folder is circled in red.
- Block Summary:** This panel shows a table of properties for the selected instance. The properties are: 1. Instance Name (gpio_inst8), 2. GPIO Resource, 3. Mode (input), 4. Unused State (NA), 5. Input, 6. Pin Name (gpio_inst8), and 7. Connection Type (normal).
- Block Editor:** This panel shows the configuration for the selected instance. The "Instance Name" field is circled in red and contains the text "stopn". The "Mode" dropdown is set to "input". The "Pin Name" field contains "gpio_inst8".

Assign the Resource CLK=>GPIOL_75

Efinity Interface Designer - new_project

File Design Report Help

Resource Assigner

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clk
Dataout[3]	F14	GPIOR_118	3A_3B_3C	GCTRL	DDIO	R1
Dataout[4]	N14	GPIOR_153	3D_3E	None	DDIO	R0
clk						
setn						
stopn						

Design Explorer

Type and press Enter to ...

Search filter...

Device Setting

- I/O Banks (10)
- Configuration
- GPIO (8)
 - Dataout [4:0]
 - clk :
 - setn :
 - stopn :
- PLL (0)

Block Summary

Property	Value
1 Instance Name	stopn
2 GPIO Resource	
3 Mode	input
4 Unused State	NA
5 Input	
6 Pin Name	stopn
7 Connection Type	normal

Block Editor

Instance Name

stopn

Mode

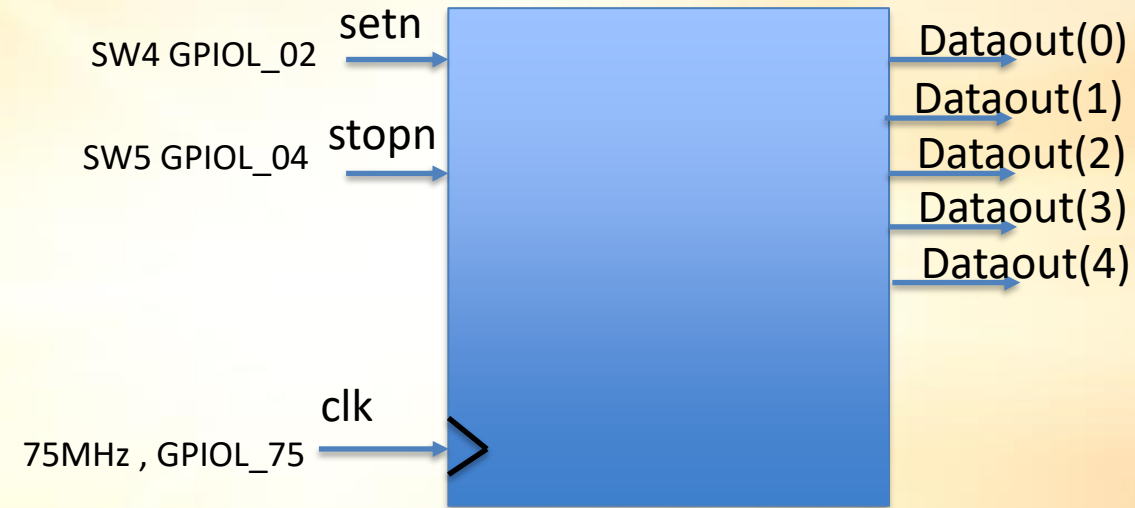
input

Input

Pin Name

stopn

Connection Type



Assign the Resource setn=>GPIOL_02

Efinity Interface Designer - new_project

File Design Report Help

Resource Assigner

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features
Dataout[3]	F14	GPIOB_118	3A_3B_3C	GCTRL	DDIO
Dataout[4]	N14	GPIOB_153	3D_3E	None	DDIO
clk	E8	GPIOL_75	1D_1E	PLL_CLKIN	None
setn					
stopn					

Design Explorer

Type and press Enter to ...

Search filter...

Device Setting

- I/O Banks (10)
- Configuration
- GPIO (8)
 - Dataout [4:0]
 - clk : GPIOL_75
 - setn :
 - stopn :
- PLL (0)

Block Summary

Pr	Instance Name	stopn
1	GPIO Resource	
2	Mode	input
3	Unused State	NA
4	Input	
5	Pin Name	stopn
6	Connection Type	normal

Block Editor

Instance Name

stopn

Mode

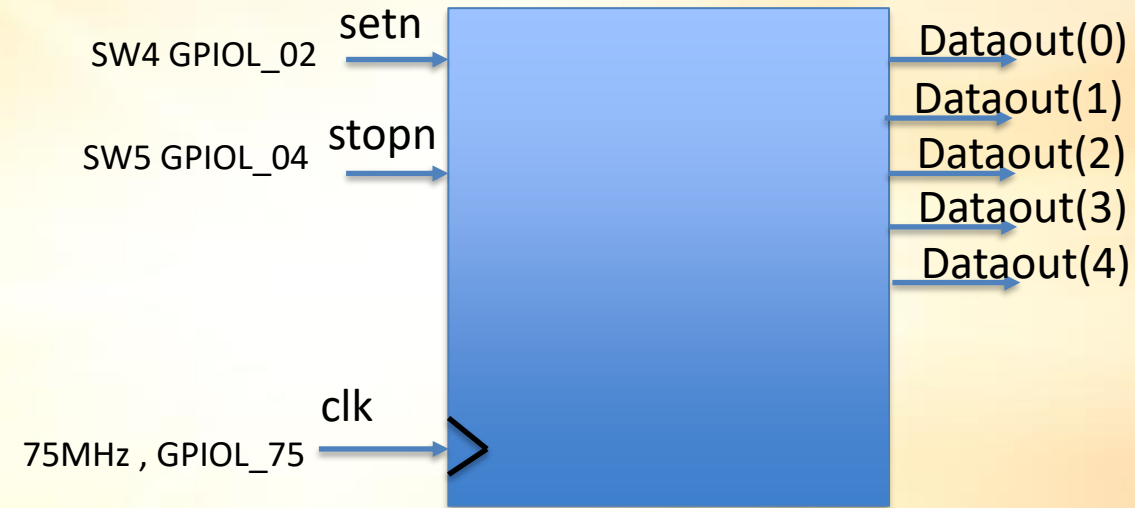
input

Input

Pin Name

stopn

Connection Type



Assign the Resource stopn=>GPIOL_04

Efinity Interface Designer - new_project

File Design Report Help

Resource Assigner

GPIO : Instance View

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features
Dataout[3]	F14	GPIOR_118	3A_3B_3C	GCTRL	DDIO
Dataout[4]	N14	GPIOR_153	3D_3E	None	DDIO
clk	E8	GPIOL_75	1D_1E	PLL_CLKIN	None
setn	P2	GPIOL_02	1A	None	None
stopn					

Design Explorer

Type and press Enter to ...

Search filter...

Device Setting

- I/O Banks (10)
- Configuration
- GPIO (8)
 - Dataout [4:0]
 - clk : GPIOL_75
 - setn : GPIOL_02
 - stopn :
- PLL (0)

Block Summary

Pr	Instance	GPIO Resource	Mode	Unused State	Input	Pin Name	Connection Type
1	Instance						
2	GPIO Resource						
3	Mode		input				
4	Unused State		NA				
5	Input						
6	Pin Name		stopn				
7	Connection Type		normal				

Block Editor

Instance Name

stopn

Mode

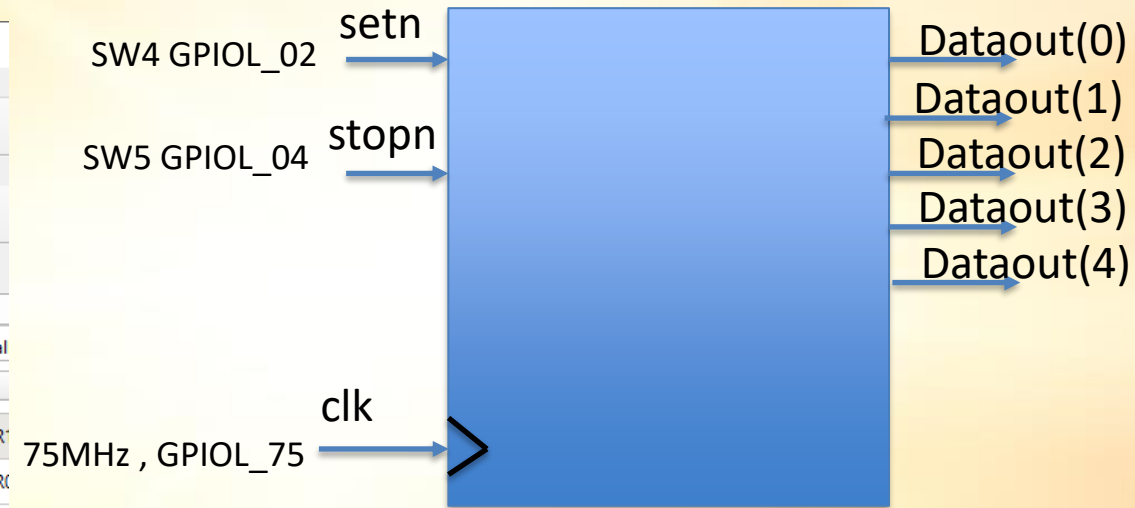
input

Input

Pin Name

stopn

Connection Type



Check the design and close the interface designer

The screenshot shows the Efinity Interface Designer window with the title 'Efinity Interface Designer - new_project'. The menu bar includes File, Design, Report, and Help. The toolbar contains various icons, with the 'Check Design' icon (a green checkmark) circled in red. Below the toolbar is the 'Resource Assigner' section, which includes a 'Check Design' button. The main area displays the 'GPIO : Instance View' table, which lists GPIO instances and their configurations. At the bottom, there are three panels: 'Design Explorer' showing a tree view of the design, 'Block Summary' showing a table of properties for the selected instance, and 'Block Editor' showing the configuration fields for the selected instance.

Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region
Dataout[3]	F14	GPIOR_118	3A_3B_3C	GCTRL	DDIO	R1
Dataout[4]	N14	GPIOR_153	3D_3E	None	DDIO	R0
clk	E8	GPIOL_75	1D_1E	PLL_CLKIN	None	T
setn	P2	GPIOL_02	1A	None	None	L0
stopn	N3	GPIOL_04	1A	None	None	L0

Property	Value
1 Instance Name	stopn
2 GPIO Resource	GPIOL_04
3 Mode	input
4 Unused State	NA
5 Alternate Connection	None
6 Features	None
7 Clock Region	L0

Instance Name: stopn
Mode: input
Input: stopn
Connection Type:

Check design...done. 0 issue.

Run the flow with clicking on placement



Efinity Software

File Flow Tools Floorplan Help

Project : new_project

dashb

Project Netlist Result

Interface
Simulation
Synthesis
Placement
Routing
Bitstream
Debugger

Core Resource	
Inputs	3 / 470
Outputs	5 / 595
Clocks	1 / 16
Logic Elements	38 / 19728
Memory Blocks	0 / 204
Multipliers	0 / 36
Interface	

Console

```
Generated 1169277 RR nodes and 4443471 RR edges
This design has 0 global control net(s). See Y:/Efinix/designs/T20EvalBoard/
T20EvalBoard/outflow/new_project.pnr.rpt for details.
Reading route file, Y:/Efinix/designs/T20EvalBoard/T20EvalBoard/outflow/
new_project.route
Reading core interface constraints from 'Y:/Efinix/designs/T20EvalBoard/
T20EvalBoard/outflow/new_project.interface.csv'.
Successfully processed interface constraints file "Y:/Efinix/designs/
T20EvalBoard/T20EvalBoard/outflow/new_project.interface.csv".

SDC file 'Y:/Efinix/designs/T20EvalBoard/T20EvalBoard/counterconstrain.sdc'
parsed successfully.
1 clocks (including virtual clocks), 0 inputs and 0 outputs were constrained.

NOTE: The timing data is not final.

Maximum possible analyzed clocks frequency
Clock Name      Period (ns)    Frequency (MHz)    Edge
clk              4.415          226.484           (R-R)

Geomean max period: 4.415

Launch Clock    Capture Clock    Constraint (ns)    Slack (ns)    Edge
clk             clk              13.000            8.585         (R-R)

Do März 19 20 09:46:10 - Flow data refreshed. Elapsed time = 0m 6.468s VM :
485.324 MB RSS : 516.472 MB
Do März 19 20 09:46:10 - Running automated flow starting from synthesis done.
Total duration = 1m 29.916s
Do März 19 20 09:46:46 - Interface design file exists, open design
Do März 19 20 09:46:46 - Running Efinity Interface Designer...
Do März 19 20 10:07:34 - Efinity Interface Designer finished. Exit code = 0 Exit
status : Normal
```

If you have an unassigned pin, check the Placement report, go back to interface designer and fix the name and rerun the flow

The screenshot displays the Efinity Software interface with the following components:

- Project : new_project** (top left)
- dashbord** (top left, below project name)
- Project | Netlist | Result** (tabs)
- Placement** (selected in the left sidebar)
- Outputs** table:

Outputs	5 / 113
Clocks	1 / 16
Logic Elements	37 / 7384
Memory Blocks	0 / 24
Multipliers	0 / 8
Interface	
Missing Interface Pins	1
Unassigned Core Pins	1
Timing	
Least Slack	23.349 ns
clk	103.613 MHz
Debugger	
- Console** (middle left):

```
efinixprojects/T8EvalBoard/outflow/  
new_project.interface.csv'.  
Successfully processed  
interface constraints file  
"D:/user/efinixprojects/  
T8EvalBoard/outflow/  
new_project.interface.csv".  
  
SDC file 'D:/user/  
efinixprojects/T8EvalBoard/  
counterconstrain.sdc' parsed  
successfully.  
1 clocks (including virtual  
clocks), 0 inputs and 0  
outputs were constrained.  
  
Maximum possible analyzed  
clocks frequency  
Clock Name      Period (ns)  
Frequency (MHz)  Edge  
clk              9.651  
103.613         (R-R)  
  
Geomean max period: 9.651  
  
Launch Clock    Capture Clock  
Constraint (ns) Slack (ns)  
Edge           clk  
clk            33.000    23.349    (R-  
R)  
  
Mi März 18 20 11:36:00 - Flow  
data refreshed. Elapsed time  
= 0m 3.156s VM : 220.104 MB  
RSS : 253.856 MB  
Mi März 18 20 11:36:00 -  
Running automated flow  
starting from synthesis done.  
Total duration = 0m 12.308s
```
- Code Editor** (right):
 - new_project.timing.rpt**:

```
11  
12 ----- Resource Summary (begin) -----  
13 Inputs: 3 / 96 (3.12%)  
14 Outputs: 5 / 113 (4.42%)  
15 Clocks: 1 / 16 (6.25%)  
16 Logic Elements: 37 / 7384 (0.50%)  
17    LE: LUTs/Adders: 31 / 7384 (0.42%)  
18    LE: Registers: 35 / 5280 (0.66%)  
19 Memory Blocks: 0 / 24 (0.00%)  
20 Multipliers: 0 / 8 (0.00%)  
21 ----- Resource Summary (end) -----  
22  
23 Elapsed time for packing: 0 hours 0 minutes 0 seconds  
24  
25 ----- IO Interface Summary (begin) -----  
26  
27 +-----+  
28 | Missing Interface Pins | Input/Output |  
29 +-----+  
30 | stop | Input |  
31 +-----+  
32  
33 ----- IO Interface Summary (end) -----  
34  
35 ----- IO Placement Summary (begin) -----  
36  
37 +-----+  
38 | Unassigned Core Pins | Input/Output |  
39 +-----+  
40 | stopn | Input |  
41 +-----+  
42  
43 ----- IO Placement Summary (end) -----  
44  
45 Elapsed time for placement: 0 hours 0 minutes 1 seconds  
46  
47
```
 - new_project.route.rpt**: (empty)
 - new_project.place.rpt**: (empty)

Typo in
Interface
designer:
stop instead
of **stopn**

Check static timing

The screenshot displays the Efinix Software interface with the following components:

- Project:** new_project
- dashb@rd:** A dashboard with icons for Project, Netlist, Result, and a timer.
- Project Tree:** A list of project files including Interface, Simulation, Synthesis, Placement, Routing (selected), Bitstream, and Debugger. Under Routing, files like new_project.route.rpt, new_project.timing.rpt, and new_project.route.out are listed.
- Core Resource:** A table showing resource usage:

Resource	Used	Total
Inputs	3	470
Outputs	5	595
Clocks	1	16
Logic Elements	38	19728
Memory Blocks	0	204
Multipilers	0	36
Interface		
Missing Interface Pins	0	
Unassigned Core Pins	0	
Timing		
Least Slack	8.585 ns	
clk	226.484 MHz	
Debugger		
Auto Instantiation	No	
System Resource		
- Console:** A log window showing the progress of the static timing analysis, including netlist pre-processing and resident set memory usage.
- Code Editor:** A window displaying the static timing analysis report (new_project.timing.rpt). The report includes a Table of Contents and a section titled "1. Clock Frequency Summary (begin)". A red circle highlights the "User target constrained clocks" table.

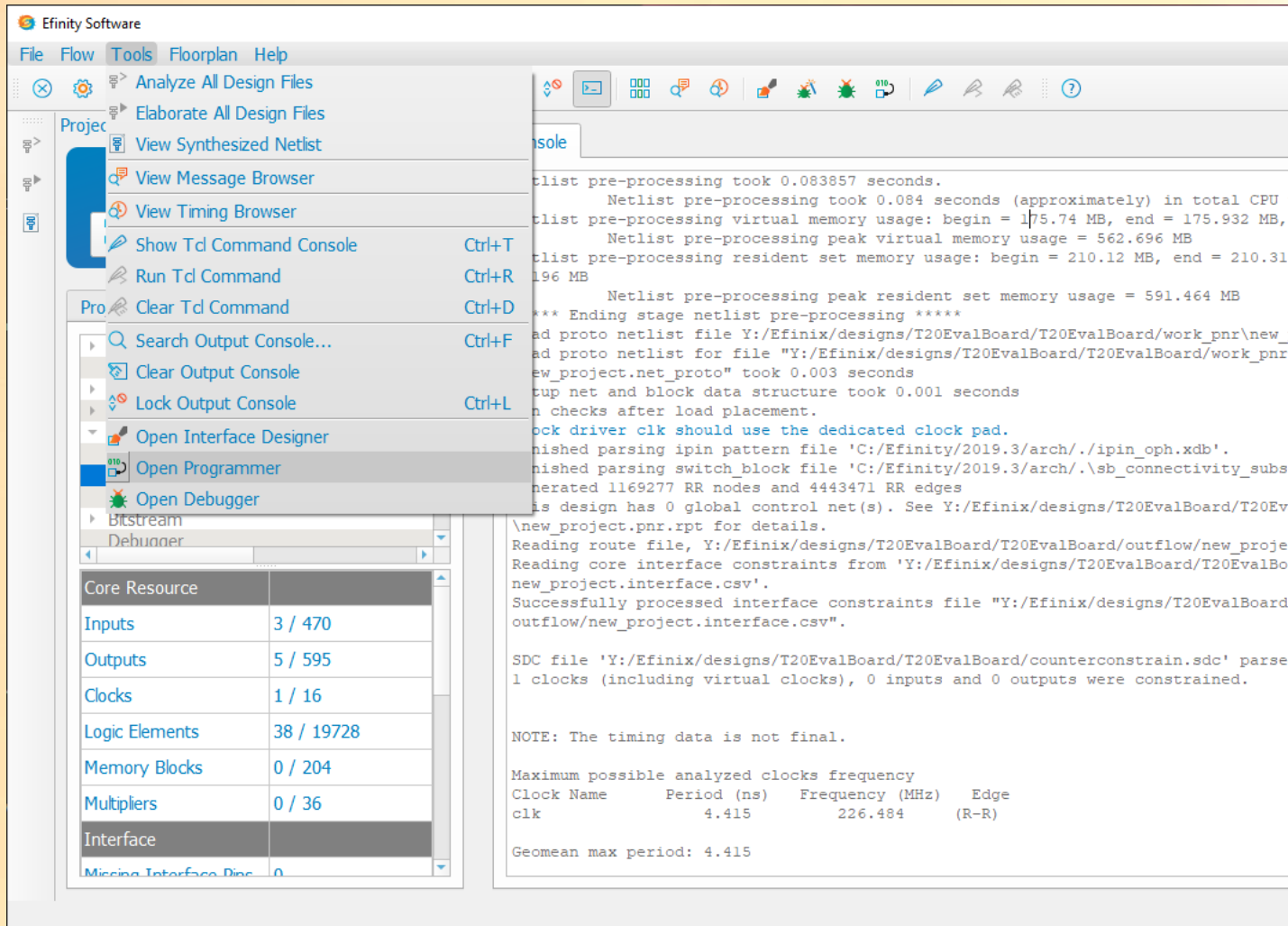
User target constrained clocks table:

Clock Name	Period (ns)	Frequency (MHz)	Waveform	Source Clock Name
clk	13.000	76.923	{0.000 6.500}	virtual

The report also includes a section for "Maximum possible analyzed clocks frequency" and a "Geomean max period" of 4.415 ns.

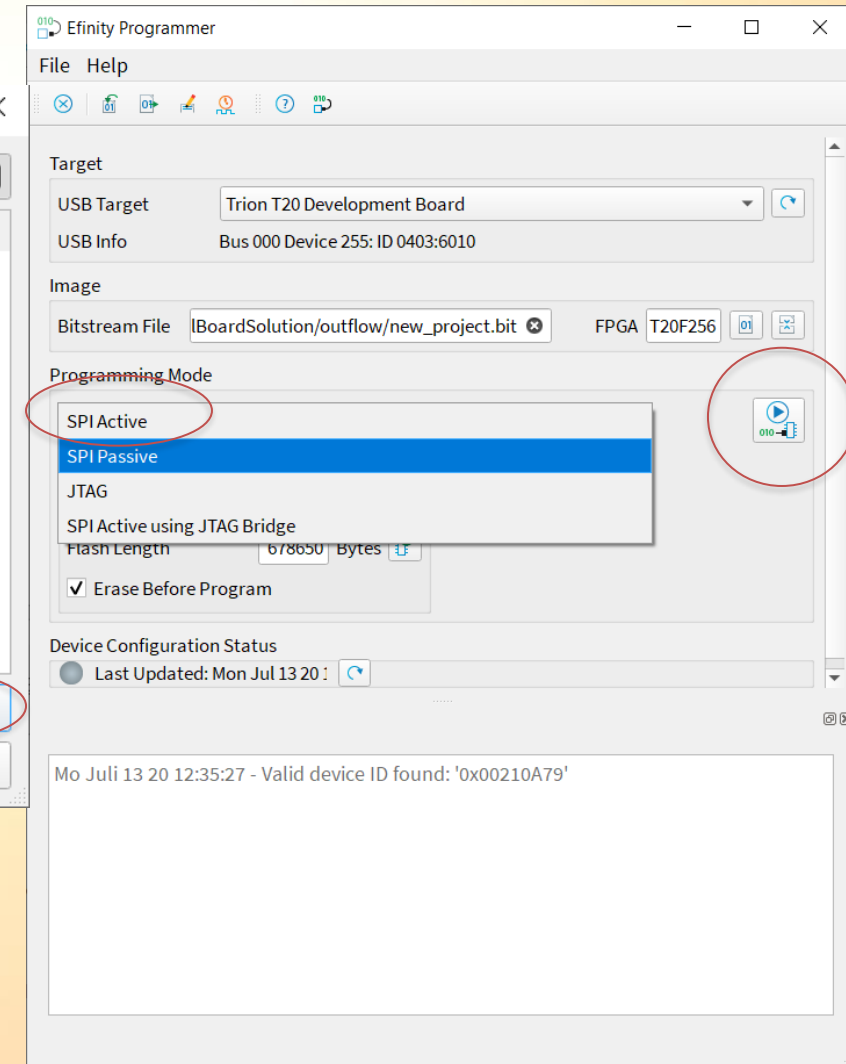
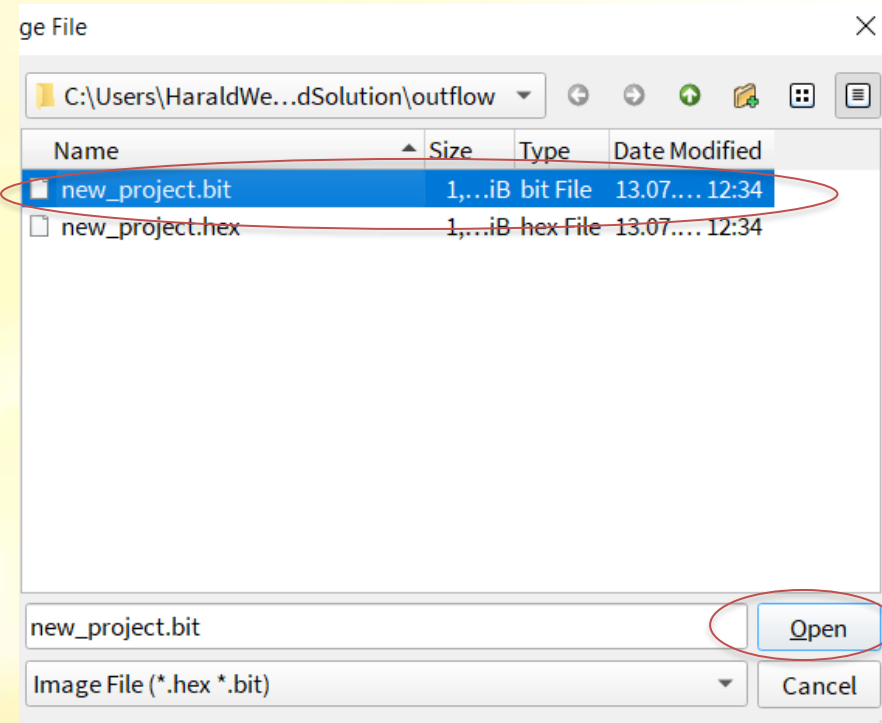
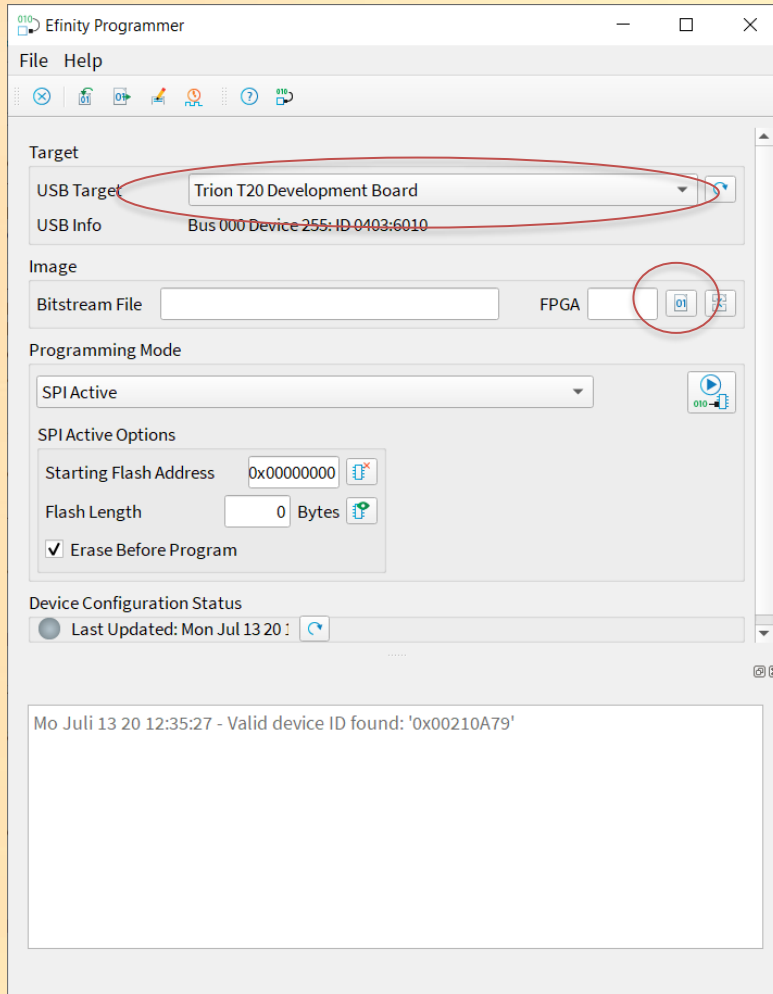
To check the static timing select routing_new_project.timing.rpt. Here you will find the constrains from the constrain file (clk :13ns) and the result

Program the Device



Open Programmer
Tools->OpenProgrammer

Select Image File, Start Program to the SPI Flash (Check USB Target Trion T20 Development Board)

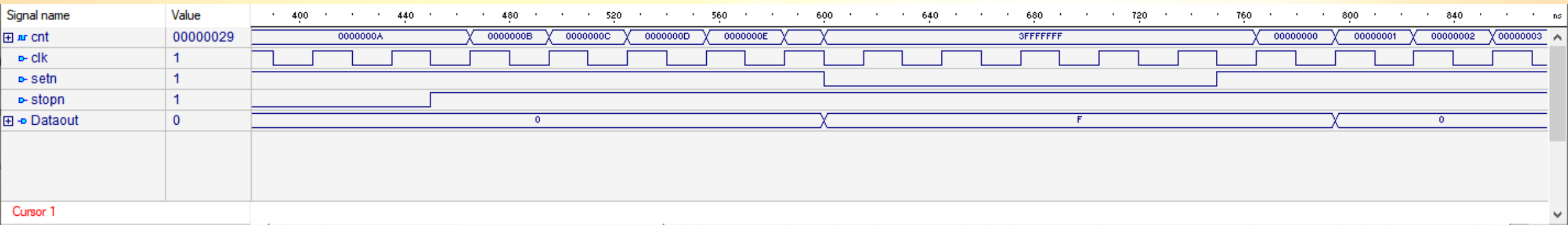


Problem solving

- If you can not see the Trion T20 Development Board, check if you installed the corect USB driver with zadig

Simulation

- For HDL simulation you can use any VHDL simulator. The testbench is included in the design.
- Here a wave form the design with testbench with an ALDEC HDL simulator.

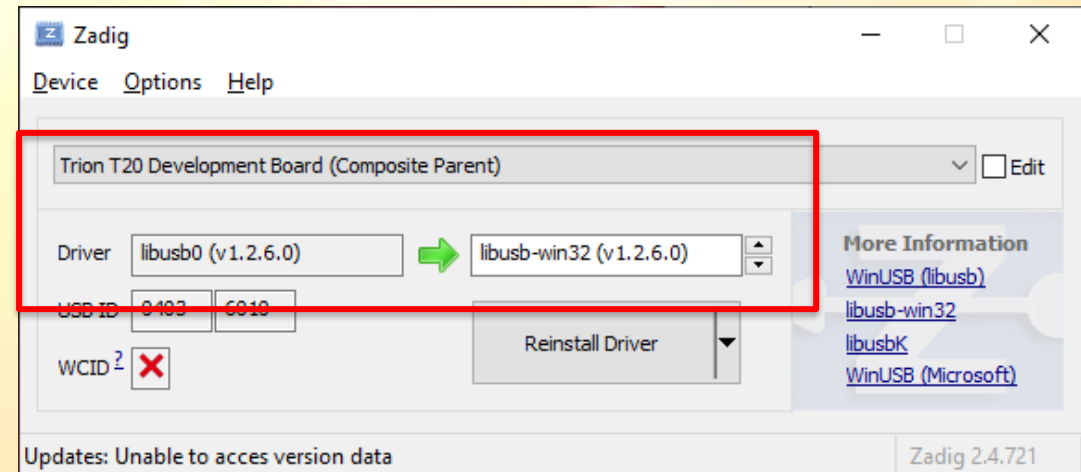
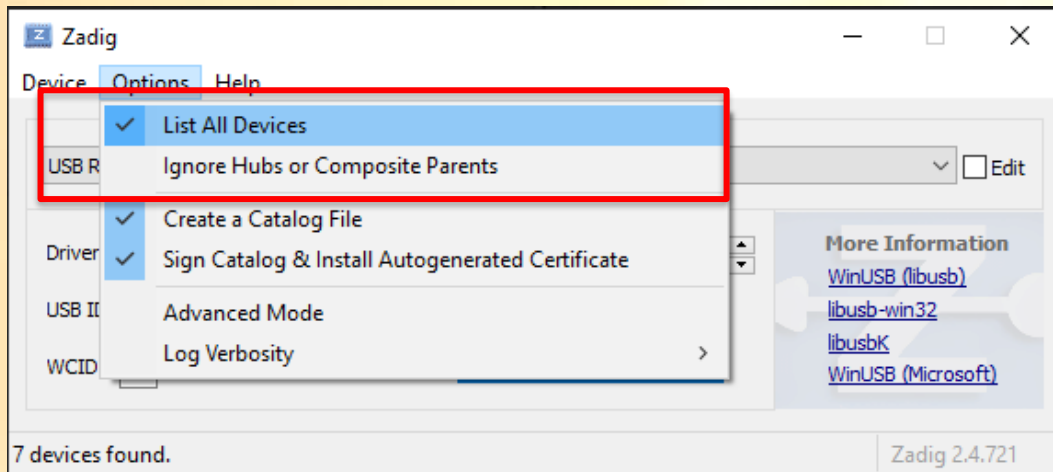


- If you would like to simulate the synthesized netlist, include the new_project.dbg.map.v below the outflow folder and include the simulation libraries <installation path>\Efinity\2020.1\sim_models\verilog folder instead of the RTL Design

Design Debugging

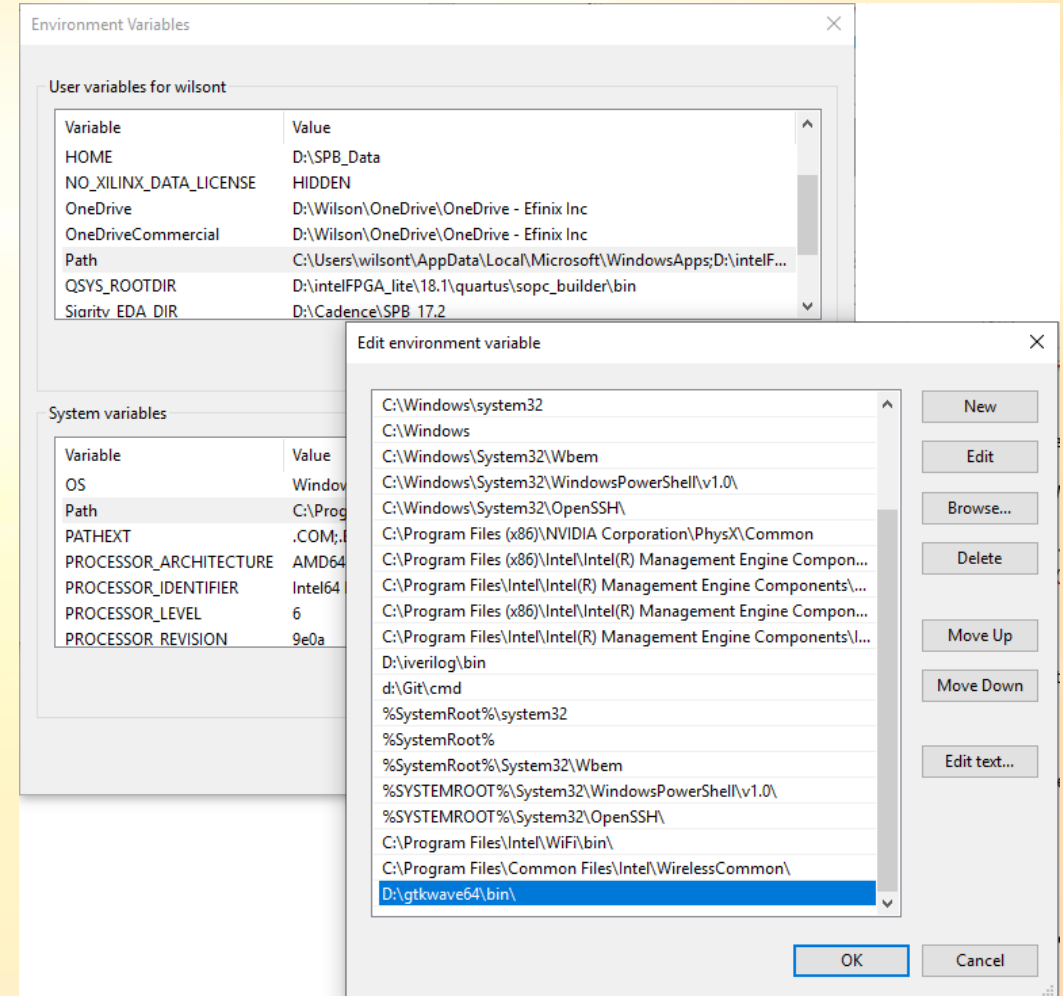
Driver Installation with zadig

- Check “List All Devices”
- Uncheck “Ignore Hubs or Composite Parents”
- Select “Trion T20 Development Board (Composite Parent)”
- Replace with **libusb-win32** driver



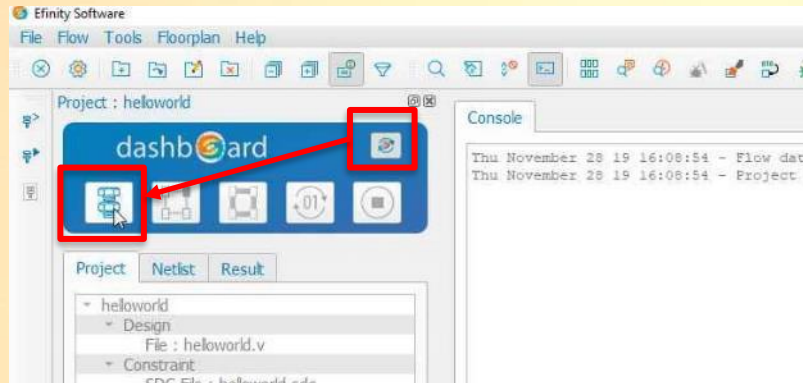
GTKWave

- Install GTKWave
- To launch GTKWave automatically after data capture from Logic Analyzer, please add “\$GTKWave_folder\$\\bin\\” into Path of System Variables

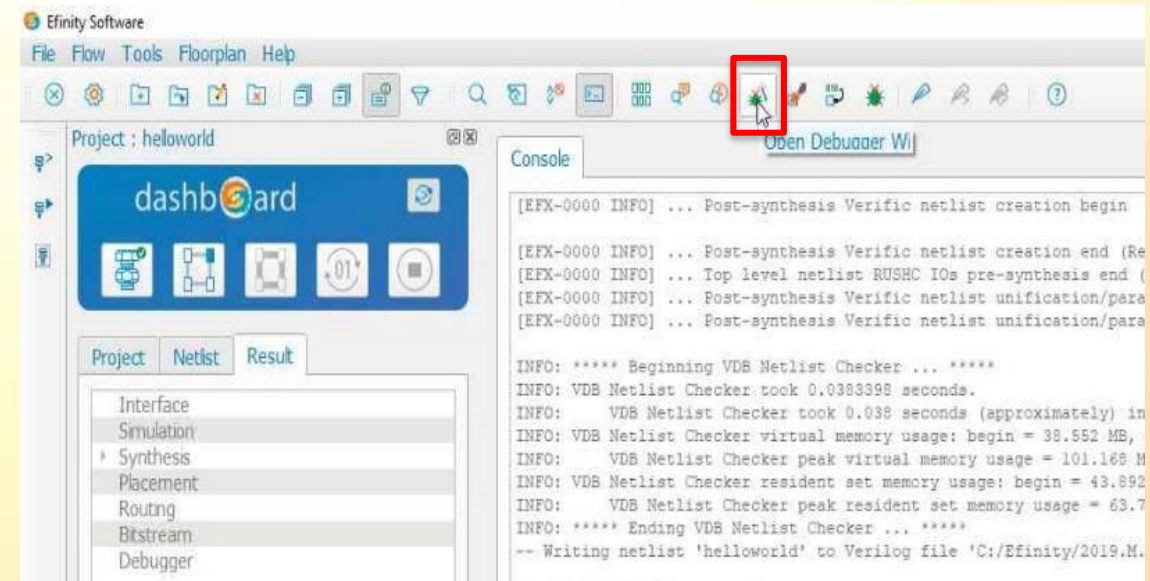


Auto Instantiation of the Debug core

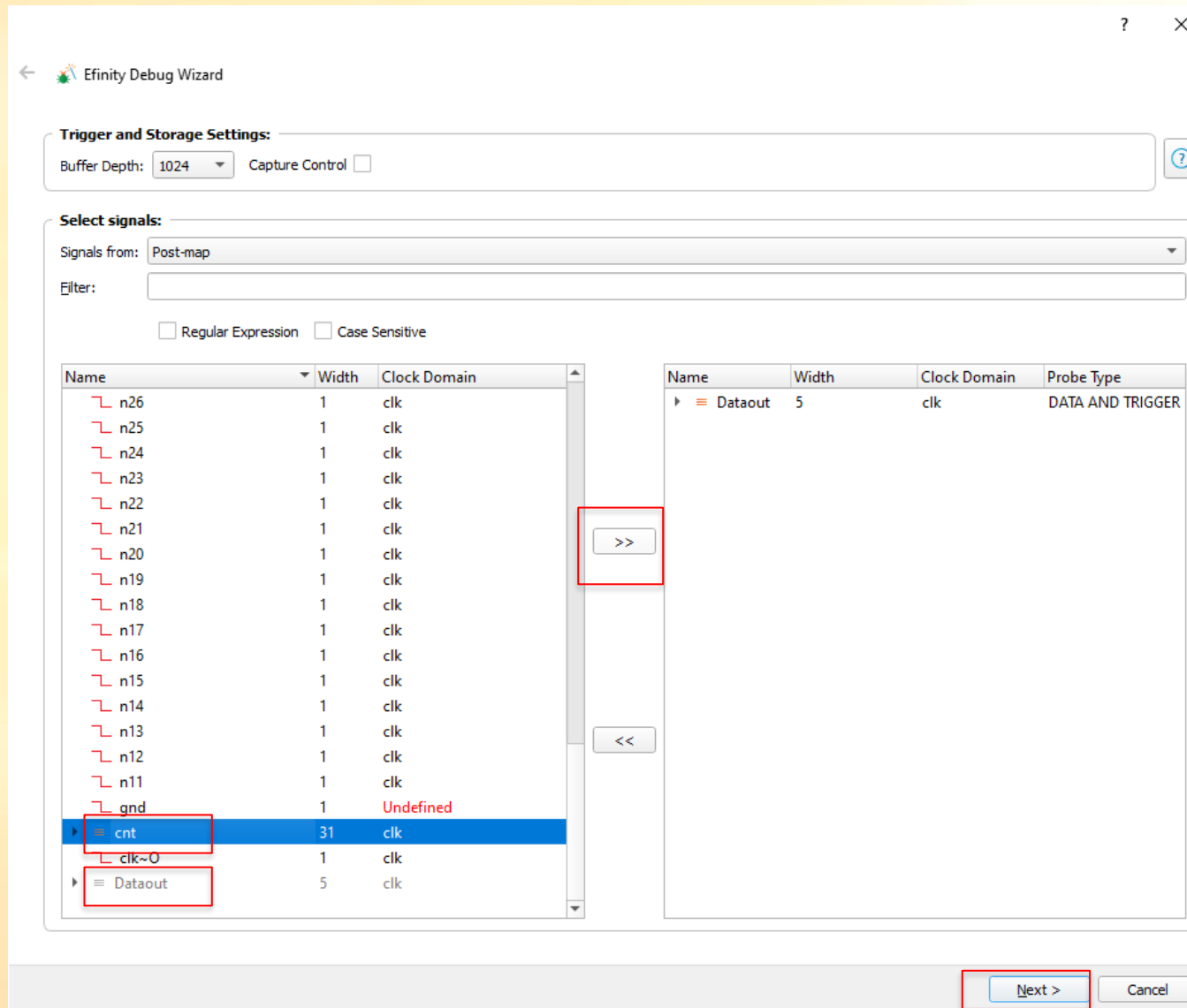
1. Allow step-by-step project flow, and run synthesis



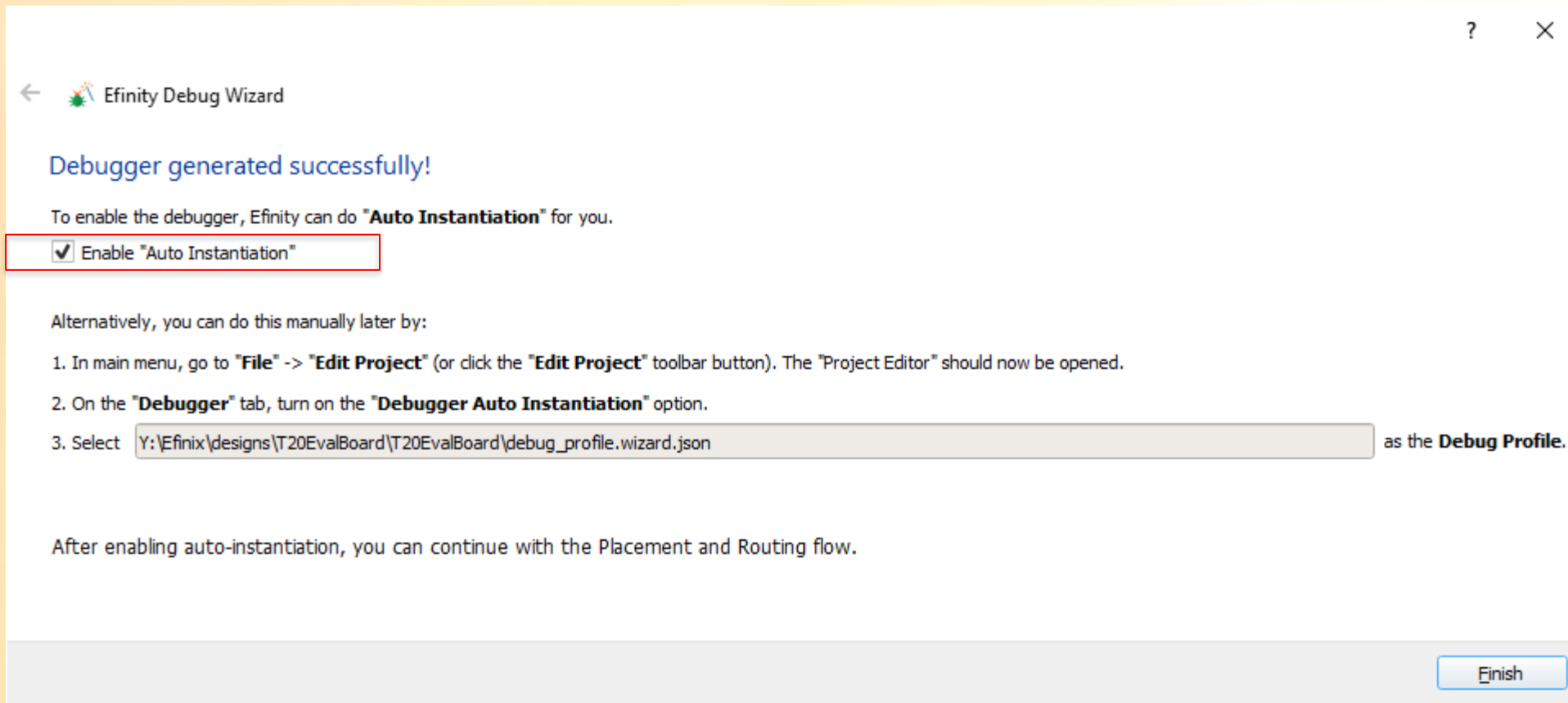
2. Start Debugger Wizard



Select cnt and Dataout and klick >>



Click Finish



Enable Auto
instantiation

Click OK and run the whole flow with clicking



The screenshot shows the Efinity Software interface. The 'Project' panel on the left lists various project files under 'Routing'. The 'Console' window on the right displays log messages from the automated flow. A 'Project Edited' dialog box is open in the center, warning that the debugger status has changed and advising to rerun the flow from placement. The background shows the 'dashboard' with icons for different project stages and a table of core resources.

Core Resource	
Inputs	3 / 470
Outputs	5 / 595
Clocks	1 / 16
Logic Elements	38 / 19728
Memory Blocks	0 / 204
Multipliers	0 / 36
Interface	
Missing Interface Pins	0

Console Log:

```
Finished parsing ipin pattern file 'C:/Efinity/2019.3/arch/./ipin_oph.xdb'.
Finished parsing switch_block file 'C:/Efinity/2019.3/arch/./sb_connectivity_su
Generated 1169277 RR nodes and 4443471 RR edges
This design has 0 global control net(s). See Y:/Efinity/designs/T20EvalBoard/T20
/new_project.pnr.rpt for details.
Reading route file, Y:/Efinity/designs/T20EvalBoard/T20EvalBoard/outflow/new_prc
Reading core interface constraints from 'Y:/Efinity/designs/T20EvalBoard/T20Eval
new_project.interface.csv'.
Successfully processed interface constraints file "Y:/Efinity/designs/T20EvalBoa
outflow/new_project.interface.csv".
...
Do März 19 20 10:09:19 - Flow data refreshed. Elapsed time = 0m 6.396s VM : 498
524.712 MB
Do März 19 20 10:09:19 - Running automated flow starting from placement done. I
23.616s
Do März 19 20 10:12:46 - Running Efinity Programmer...
Do März 19 20 10:17:50 - Efinity Programmer finished. Exit code = 0 Exit status
Do März 19 20 10:28:45 - Signal Profile exists, open debugger wizard
Do März 19 20 10:28:45 - Running Efinity Debugger...
Do März 19 20 10:33:24 - Efinity Debugger finished. Exit code = 0 Exit status :
```

- If the Automated flow button is grayed out click on the button to activate the automated flow.



- Click on the synthesis icon and the flow will run automatically



Check static timing

The screenshot displays the Efinix Software interface with three main panels: Project, Console, and Code Editor.

Project Panel: Shows the project structure for 'new_project'. The 'Routing' section is expanded, showing files like 'new_project.place', 'new_project.place.rpt', 'new_project.place.out', 'new_project.route.rpt', 'new_project.timing.rpt', and 'new_project.route.out'. The 'Core Resource' table is also visible:

Core Resource	
Inputs	10 / 470
Outputs	6 / 595
Clocks	2 / 16
Logic Elements	2043 / 19728
Memory Blocks	8 / 204
Multiplexers	0 / 36
Interface	
Missing Interface Pins	3
Unassigned Core Pins	0
Timing	
Least Slack	2.232 ns

Console Panel: Displays the netlist pre-processing output, including memory usage and timing information. The output indicates that the timing data is not final.

Code Editor Panel: Shows the 'new_project.timing.rpt' file. The file contains the following information:

```
4 Date: Thu Mar 19 10:37:13 2020
5
6 Copyright (C) 2013 - 2019 Efinix Inc. All rights reserved.
7
8 Top-level Entity Name: new_project
9
10 SDC Filename: Y:/Efinix/designs/T20EvalBoard/T20EvalBoard/counterconstrain.sdc
11
12 Timing Model: C3
13   temperature : 0C to 85C
14   voltage : 1.2V +/-50mV
15   speedgrade : 3
16   technology : s40ll
17   status : preliminary
18
19 NOTE: The timing data is not final.
20
21 ----- Table of Contents (begin) -----
22 1. Clock Frequency Summary
23 2. Clock Relationship Summary
24 3. Path Details for Max Critical Paths
25 4. Path Details for Min Critical Paths
26 ----- Table of Contents (end) -----
27
28 ----- 1. Clock Frequency Summary (begin) -----
29
30 User target constrained clocks
31 Clock Name   Period (ns)   Frequency (MHz)   Waveform   Source Clock Name
32 clk         13.000     76.923           {0.000 6.500}   virtual
33
34 Maximum possible analyzed clocks frequency
35 Clock Name   Period (ns)   Frequency (MHz)   Edge
36 clk         10.768     92.865           (R-R)
37
38 Geomean max period: 10.768
39
40 ----- Clock Frequency Summary (end) -----
41
```

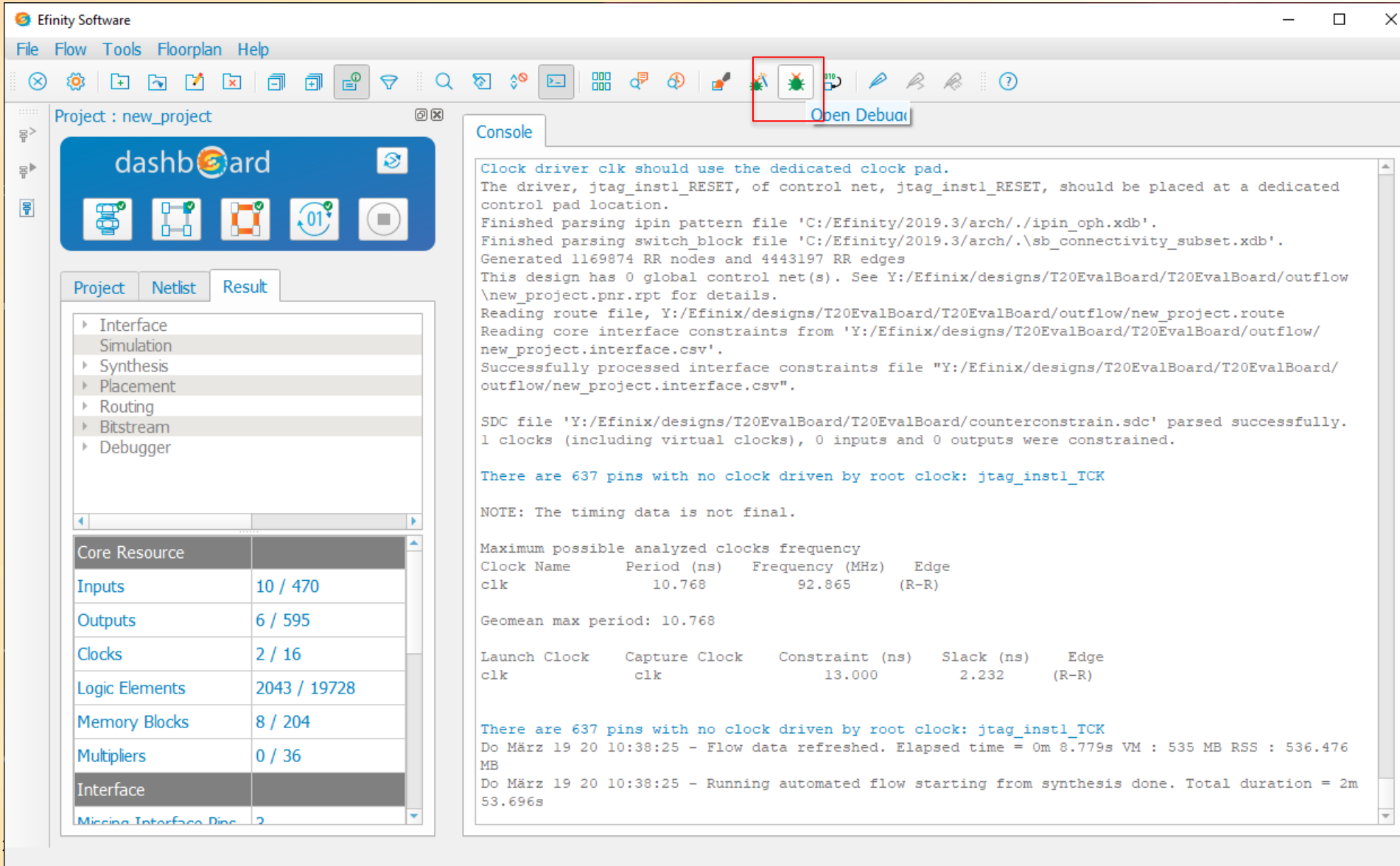
A red oval highlights the 'User target constrained clocks' section in the Code Editor, which shows the clock 'clk' with a period of 13.000 ns and a frequency of 76.923 MHz.

To check the static timing select routing_new_project.timing.rpt.

Here you will find the constrains from the constrain file (clk :13ns) and the result.

With the Debug core the design must meet the timing constrain to ensure correct behavior !

Open Debugger



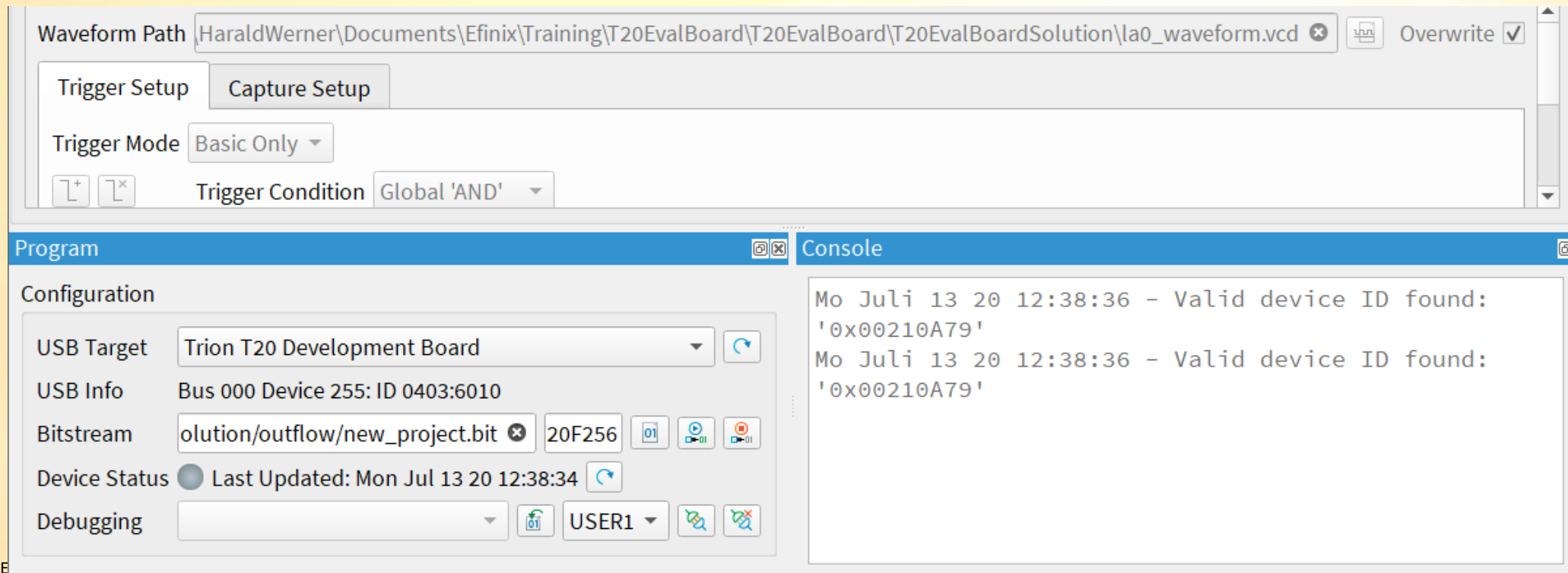
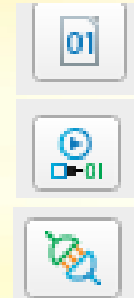
The screenshot shows the Efinity Software interface. The top menu bar includes 'File', 'Flow', 'Tools', 'Floorplan', and 'Help'. The toolbar contains various icons, with the 'Open Debugger' icon (a green bug) highlighted by a red box. Below the toolbar, the 'Project : new_project' section shows a 'dashboard' with icons for 'Interface', 'Simulation', 'Synthesis', 'Placement', 'Routing', 'Bitstream', and 'Debugger'. The 'Project' tab is selected, showing a list of project items. The 'Console' tab is active, displaying the following text:

```
Clock driver clk should use the dedicated clock pad.  
The driver, jtag_inst1_RESET, of control net, jtag_inst1_RESET, should be placed at a dedicated  
control pad location.  
Finished parsing ipin pattern file 'C:/Efinity/2019.3/arch/./ipin_oph.xdb'.  
Finished parsing switch_block file 'C:/Efinity/2019.3/arch/./sb_connectivity_subset.xdb'.  
Generated 1169874 RR nodes and 4443197 RR edges  
This design has 0 global control net(s). See Y:/Efinix/designs/T20EvalBoard/T20EvalBoard/outflow  
\new_project.pnr.rpt for details.  
Reading route file, Y:/Efinix/designs/T20EvalBoard/T20EvalBoard/outflow/new_project.route  
Reading core interface constraints from 'Y:/Efinix/designs/T20EvalBoard/T20EvalBoard/outflow/  
new_project.interface.csv'.  
Successfully processed interface constraints file "Y:/Efinix/designs/T20EvalBoard/T20EvalBoard/  
outflow/new_project.interface.csv".  
  
SDC file 'Y:/Efinix/designs/T20EvalBoard/T20EvalBoard/counterconstrain.sdc' parsed successfully.  
1 clocks (including virtual clocks), 0 inputs and 0 outputs were constrained.  
  
There are 637 pins with no clock driven by root clock: jtag_inst1_TCK  
  
NOTE: The timing data is not final.  
  
Maximum possible analyzed clocks frequency  
Clock Name      Period (ns)      Frequency (MHz)      Edge  
clk              10.768           92.865              (R-R)  
  
Geomean max period: 10.768  
  
Launch Clock      Capture Clock      Constraint (ns)      Slack (ns)      Edge  
clk              clk              13.000              2.232          (R-R)  
  
There are 637 pins with no clock driven by root clock: jtag_inst1_TCK  
Do März 19 20 10:38:25 - Flow data refreshed. Elapsed time = 0m 8.779s VM : 535 MB RSS : 536.476  
MB  
Do März 19 20 10:38:25 - Running automated flow starting from synthesis done. Total duration = 2m  
53.696s
```

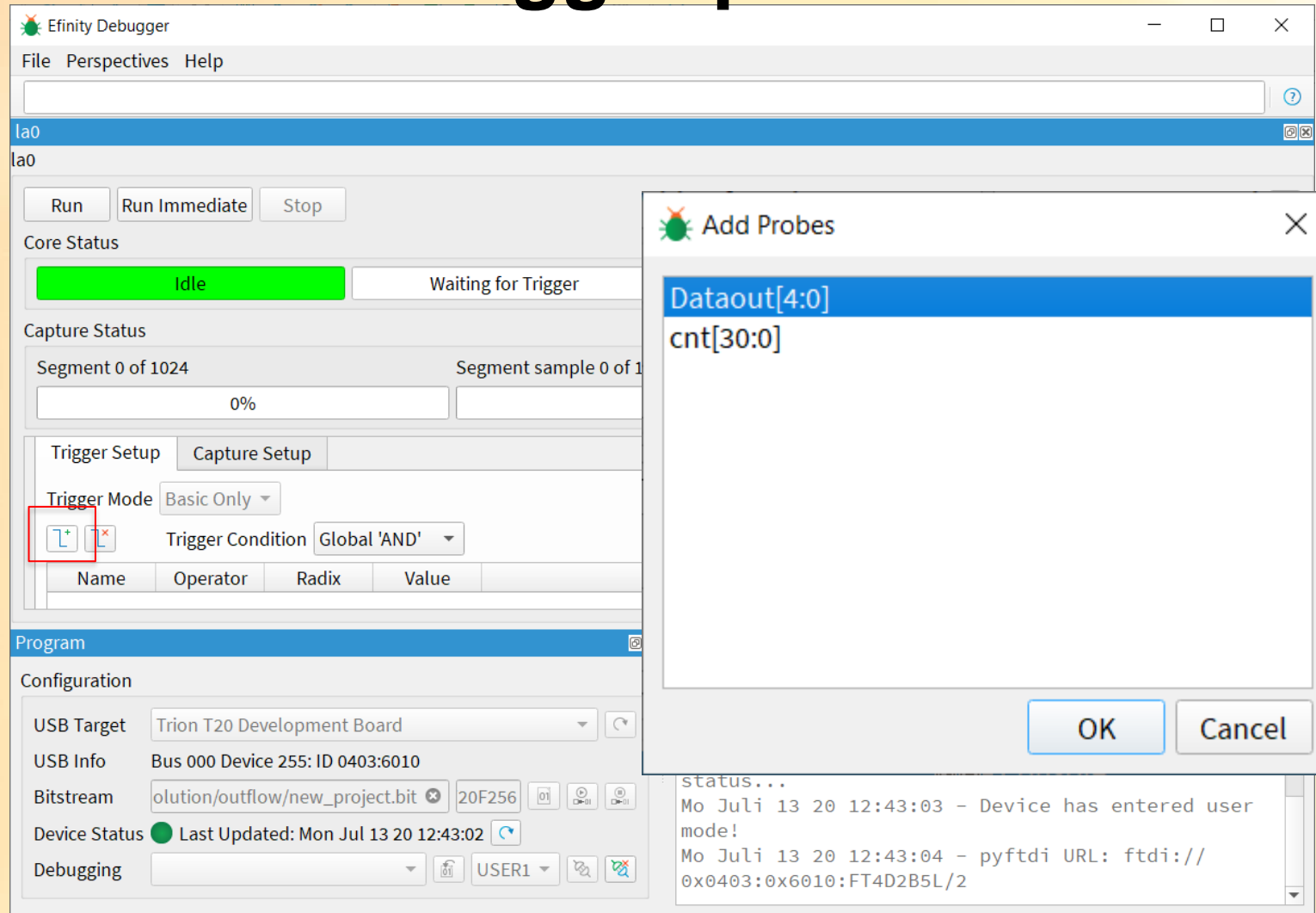
If Debugger
is not
starting,
please
double check
the driver
setting with
ZADIG

Program the Device via JTAG

- Select hex file from you project
- Start programming
- Connect Debugger



Define a trigger point



Select Trigger
Select Dataout

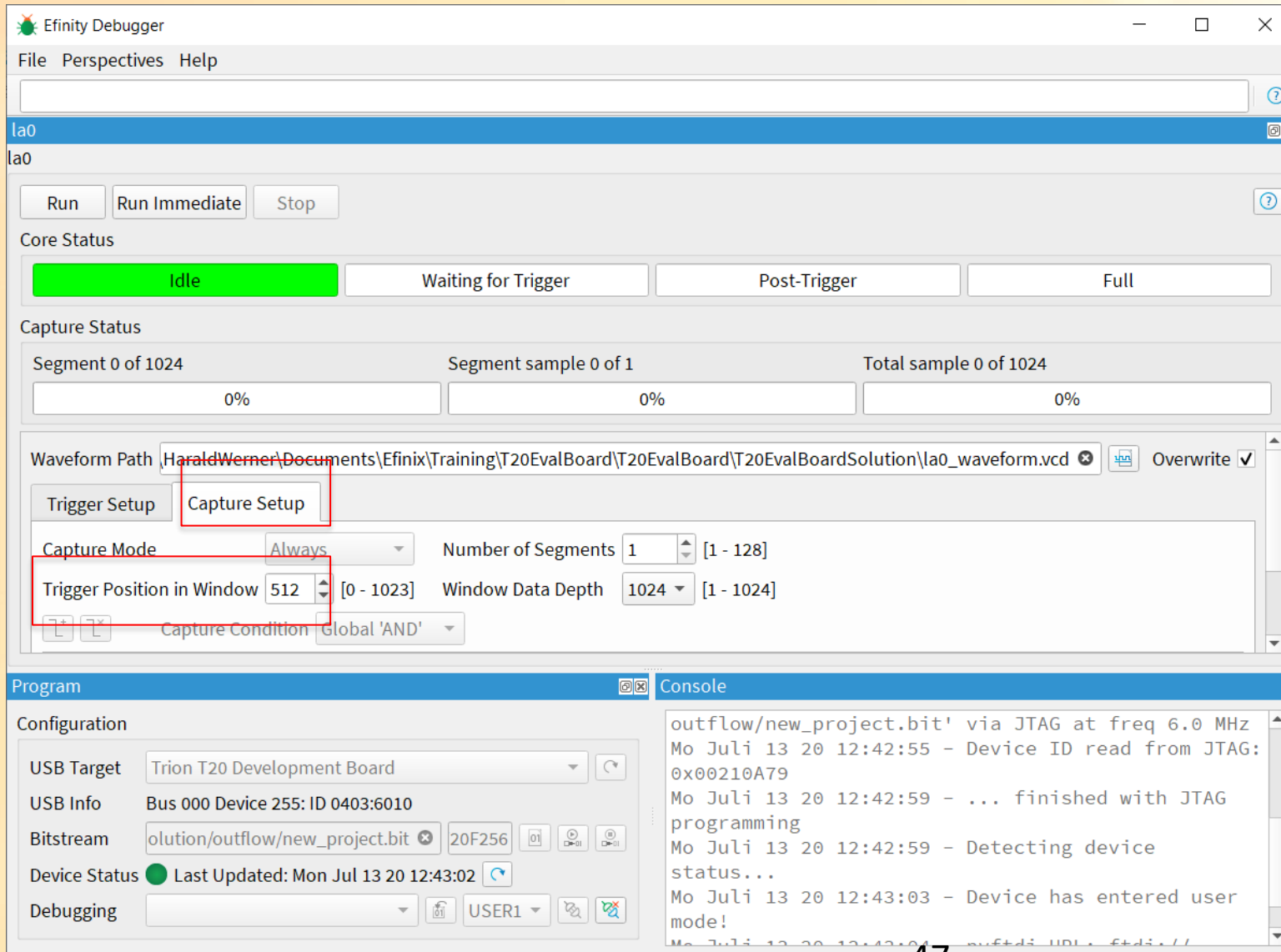
Set trigger value

The screenshot shows the Efinity Debugger interface. At the top, there's a menu bar with 'File', 'Perspectives', and 'Help'. Below it is a search bar. The main area is divided into several sections:

- Core Status:** Shows 'Idle' in a green box, with other options like 'Waiting for Trigger', 'Post-Trigger', and 'Full'.
- Capture Status:** Shows progress bars for 'Segment 0 of 1024', 'Segment sample 0 of 1', and 'Total sample 0 of 1024', all at 0%.
- Table:** A table with columns 'Name', 'Operator', 'Radix', 'Value', and 'Port'. The first row is 'Dataout[4:0] == Bin 10010 probe0[4:0]'. The 'Value' cell '10010' is highlighted with a red box.
- Program Configuration:** Shows settings for 'USB Target' (Trion T20 Development Board), 'USB Info' (Bus 000 Device 255: ID 0403:6010), 'Bitstream' (olution/outflow/new_project.bit), 'Device Status' (Last Updated: Mon Jul 13 20 12:43:02), and 'Debugging' (USER1).
- Console:** A log window showing messages like '0x00210A79', 'Mo Juli 13 20 12:42:59 - ... finished with JTAG programming', 'Mo Juli 13 20 12:42:59 - Detecting device status...', 'Mo Juli 13 20 12:43:03 - Device has entered user mode!', and 'Mo Juli 13 20 12:43:04 - pyftdi URL: ftdi://0x0403:0x6010:FT4D2B5L/2'.

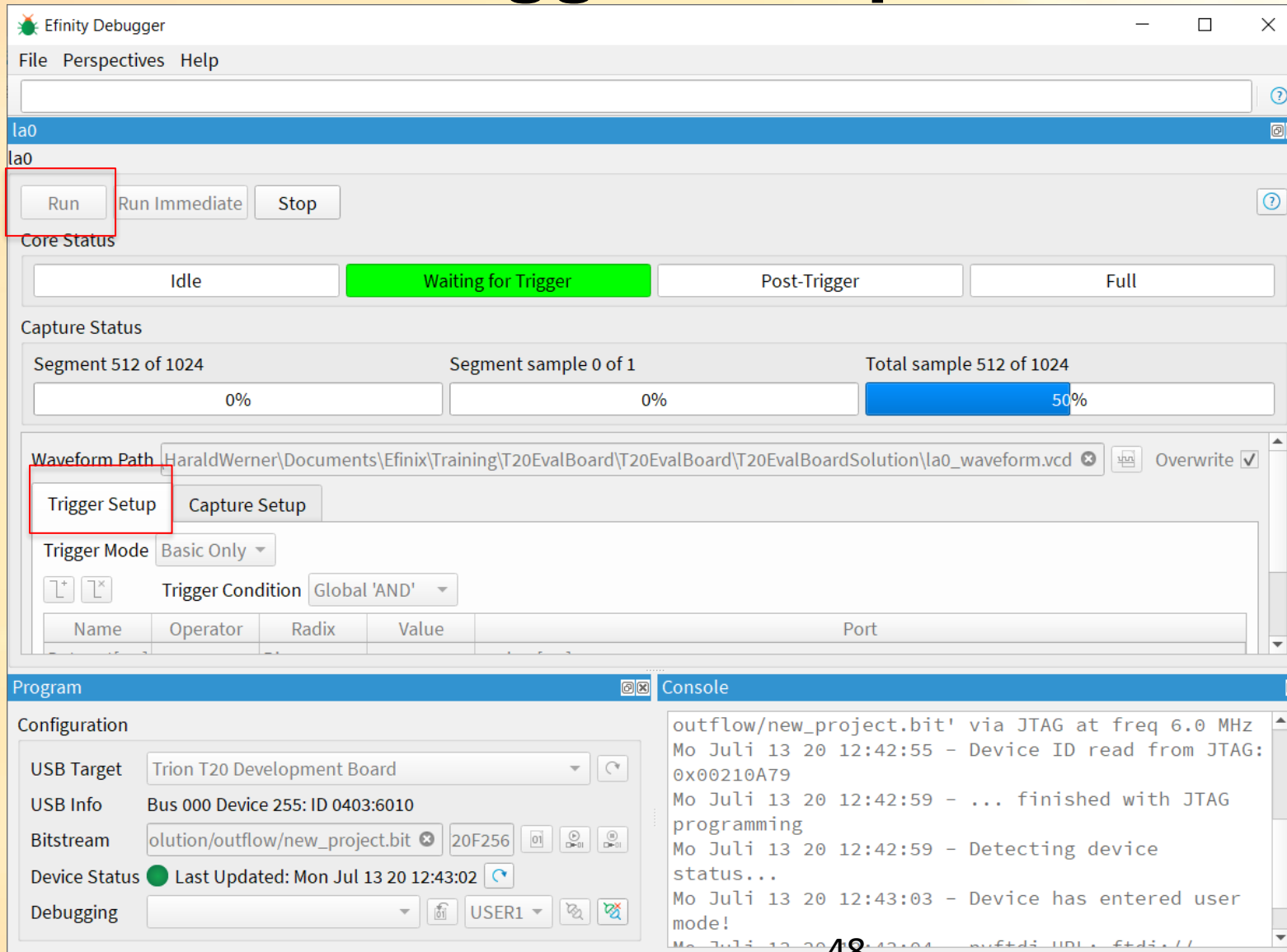
- Select Value
- Enter e.g.: 10010

Set the trigger position with clicking on Capture SETUP

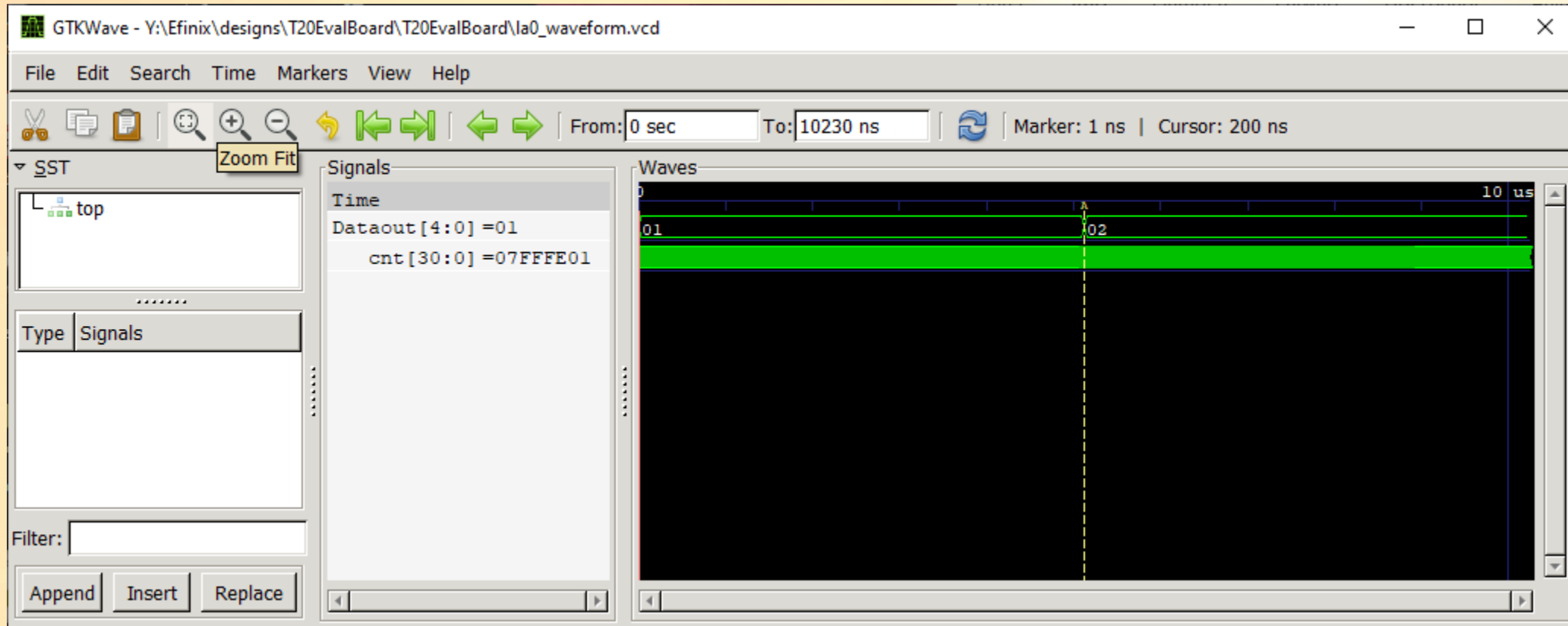


- Trigger position is default in the middle of the memory. Here @512 (of 1024)

Go back to Trigger Setup and run the Core

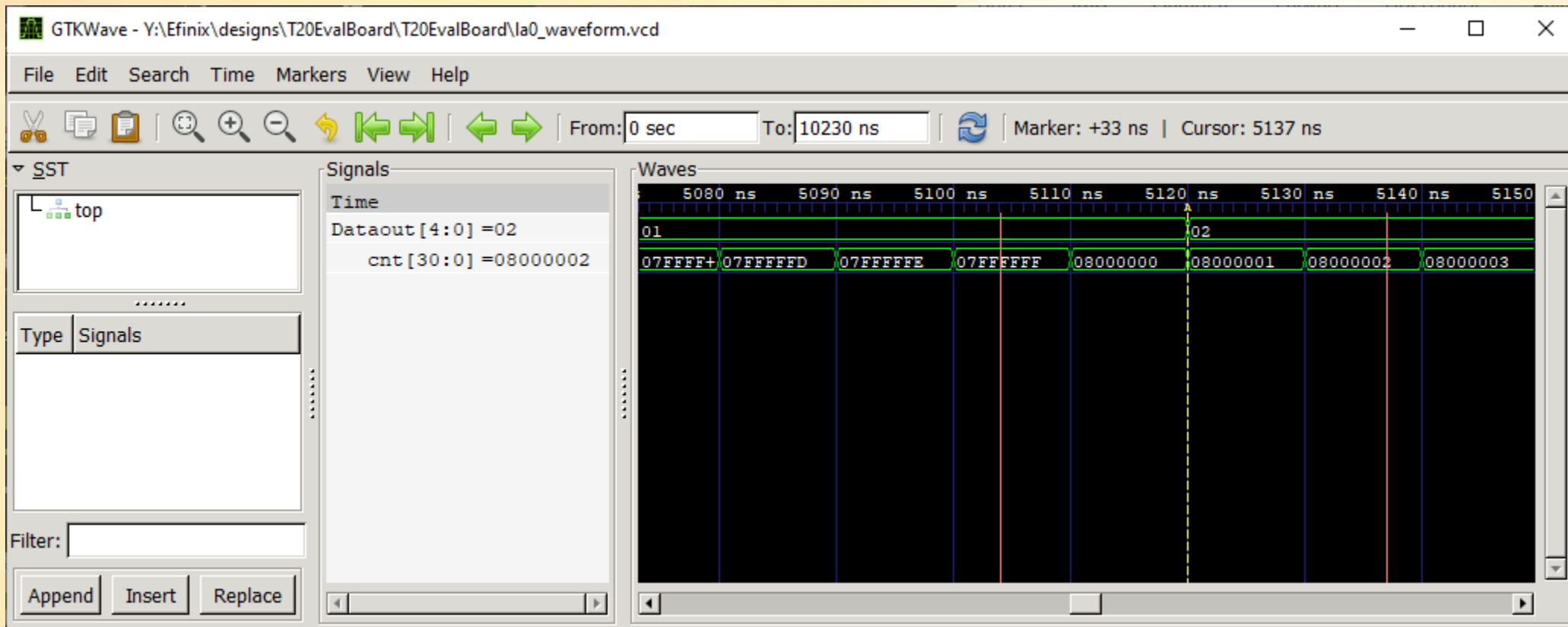


GTKWave will open automatically



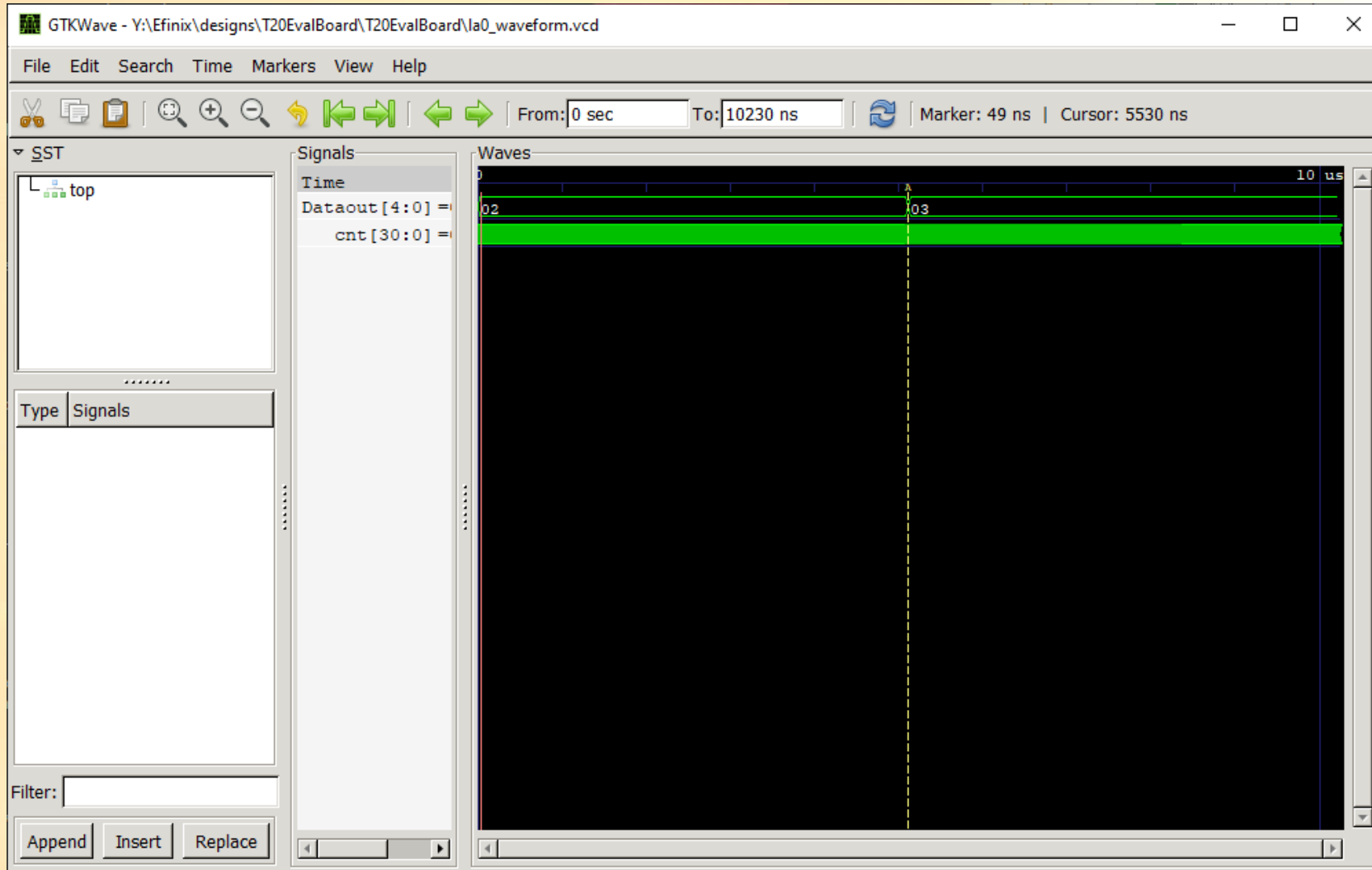
- Click on Zoom fit to see the whole content

With the RMB you can zoom in



- Place the cursor of the area of interest, press RMB and move the cursor, release RMB

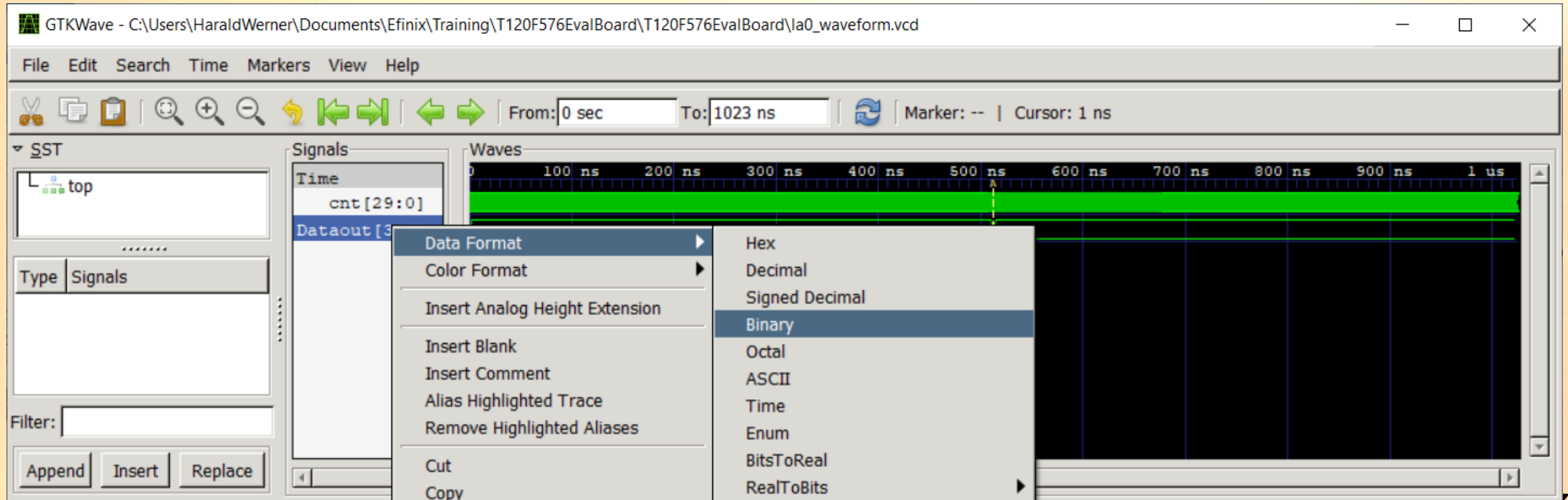
You can change the trigger value and run again



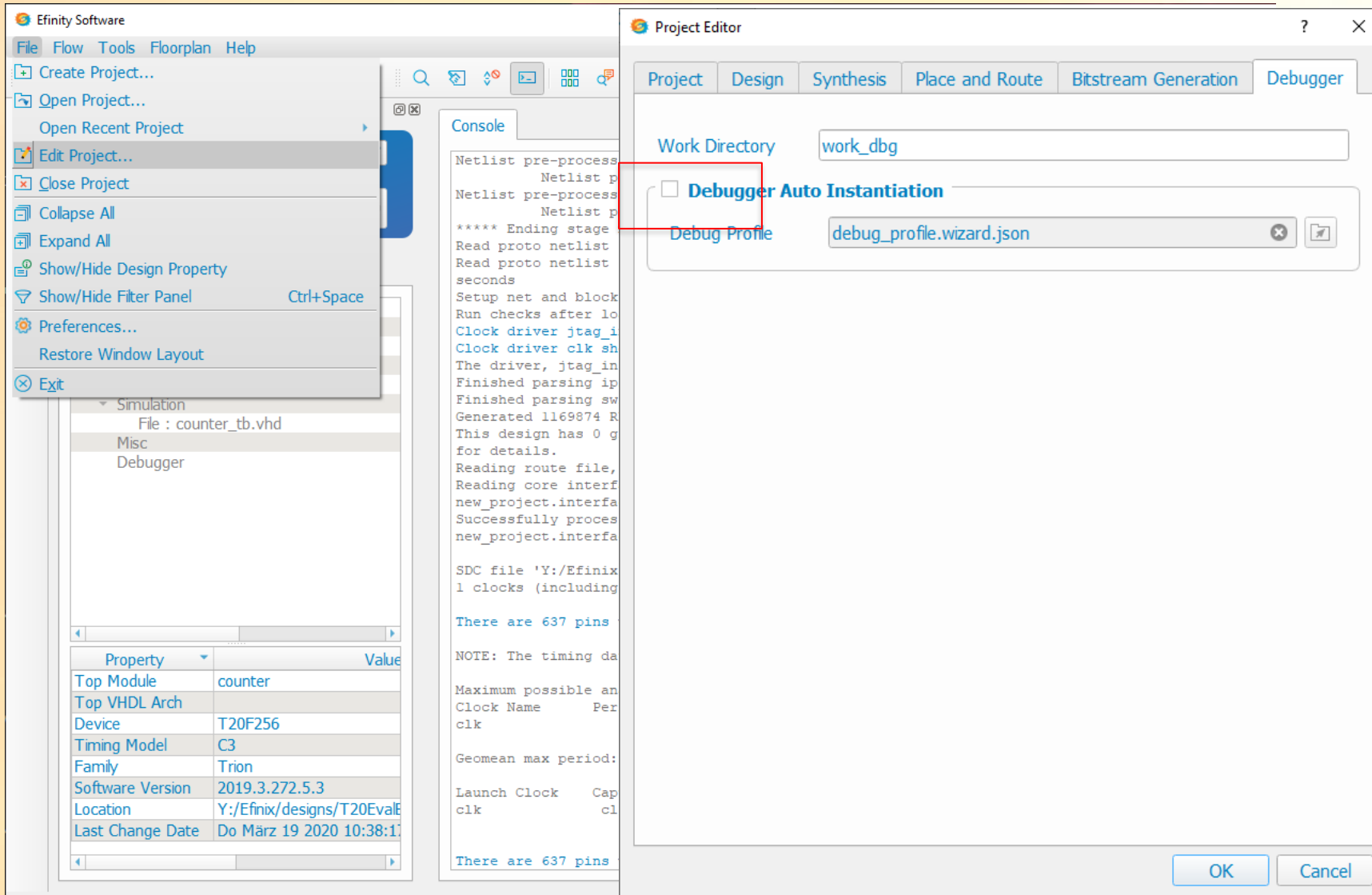
- E.g: change to 00011
- Press Run

Change Radix

- To change the radix of the signal, select the signal, RMB->Data Format->Binary



Remove the debug core



Deselect the
Debugger Auto
Instantiation.

Click OK

Run the whole
Design flow

Information

- If you need the complete Project, extract the T20EvalBoardSolution.zip file. Here you will find the project with the I/O pin assignments.