# TLM 2 Examples Mini Review



Electronic System Level Services

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# **Objectives**

- Provide example system models that communicate TLM 2 capabilities to architects of all types who are new to the OSCI TLM
- Use cases include
  - Early software development
  - Software-hardware integration
  - Software performance analysis
  - System-level architecture analysis
  - Hardware functional verification
- Models should communicate clearly
  - Familiar components, timing and behaviors
  - Minimal documentation brief, complete and clear

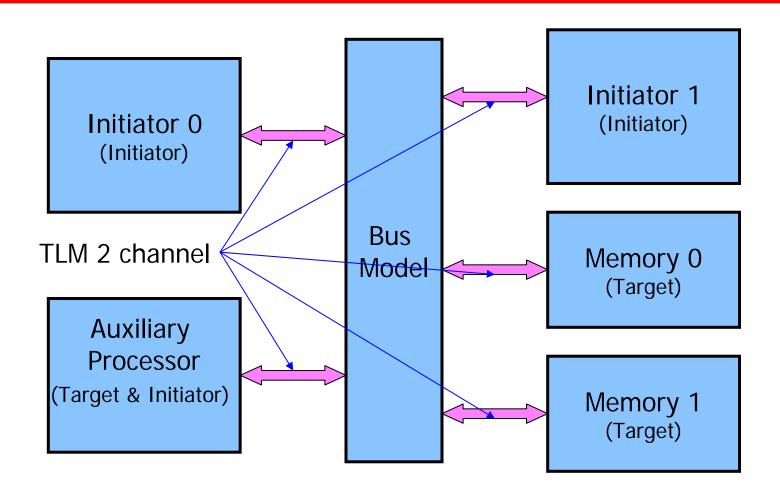


# Unit Tests Currently in TLM 2 Kit

- Bus (using Point-to-Point and SimpleBus components)
- Point 2 Point
  - BaseSocketLT
  - RegisterSocketProcessLT
  - EndEventLT
  - SimpleAT
  - SimpleAT\_TA
  - CoreDecoupling
  - GenericPayload
  - GenericPayloadExtension



# **Example System Model**





# Planned Components (1)

- Target Memory
  - LT timing unique read, write, and refresh timing
  - Parameterized memory small block of real storage (4K)
  - Crude backdoor as parameter for second memory (NV-RAM)
  - Direct Memory Interface (DMI) out-of-scope for now
- Initiator AT and LT (may also need blocking)
  - Multiple sc\_processes
  - Configurable with one or more sc\_processes
    - Block reads (i-cache fetch)
    - Block reads or writes (d-cache activity)
    - Reads and writes (peripheral control)
    - Direct execution



# Planned Components (2)

- Hybrid (target and initiator)
  - AT target, LT and AT initiator (may also need blocking)
  - CSR in bus address space (target)
  - DMA to bus address space (initiator)
- Bus Model
  - Using SimpleBus from current kit
  - Minimum required for functionality
- Possible Bridge
  - Required-extension or other options



# **Initial Example Configuration Options**

#### Option Set #1

- Attributes
  - Generic Payload (GP)
  - Non-blocking transport
  - Mixed LT/AT
- Cases
  - No extension (GP)
  - Ignorable Extension (GP+IE)
  - Non-ignorable Extension (GP+NE)

#### Option Set #2

- Untimed (UT)
  - Generic Payload
  - Blocking transport
- Loosely Timed (LT)
  - Generic Payload
  - Possible Ignorable extension
  - Non-blocking transport
  - Temporal Synchronization
- Approximately Timed (AT)
  - Extended/derived Generic Payload
  - Non-blocking transport
  - Mixed LT and AT components



# Not Planned for Initial Examples

- Interrupts
- Multiple arbitration implementations
- Analysis ports
- Direct Memory Interface (DMI)
- Mode switching (LT -> AT)
- Mixed blocking and non-blocking transport
- Features not required for the example set
  - see previous slide



### Generic Payload Extension Ideas

- Ignorable Extension Options
  - Atomic compare-and-swap (read linked write conditional)
  - Keep a copy of initiator-supplied address (used to process response)
  - Other
- Non-ignorable Extension Options
  - 2D burst transfers
  - Memory without byte read and write support (full cache line only)
  - Other



# Additional Example Configurations (1)

#### The following list is not exhaustive

- Software development platform
  - Simulation performance optimized
  - All components LT
  - Temporal Synchronization
  - Direct Memory Interface
- System-level architecture analysis model
  - Simulation performance is secondary
  - Switching from all LT to LT/AT
  - Direct Memory Interface for LT portion of simulation
  - Analysis port exercised



# Additional Example Configurations (2)

- Software-hardware integration
  - Adapters converts GP to high-fidelity hardware interfaces
    - SystemC Pin-and-Cycle Accurate model
    - RTL model
  - Switching most components from LT to AT
  - DMI for LT operation
- Hardware design verification
  - System software replaced by verification tests
  - Software development models can be used to validate verification tests
  - Adapters convert GP to high-fidelity hardware interfaces
    - Cycle Approximate (CA)
    - Pin-and-Cycle Accurate (PCA)



# Additional Example Configurations (3)

- Non-MMB interconnect models implemented using TLM 2
  - Demonstrates flexibility of TLM 2's transport
  - Payload is unique or derived from GP
  - Possibly non-MMB (switched network or network-on-a-chip)
- Exclusively blocking UT model (GP only)
- Mixed blocking and non-blocking LT model (GP only)
- Exclusively non-blocking LT model (GP only)
- Pure AT model (may require GP with extensions)

