UNIT-III

Transistor Biasing and stabilization

Need for transistor biasing

- In order to produce distortion free output, the transistor must be operated in active region. that means the operating point established in this region.
- To establish an operating point proper voltage (V_{CE}) and resistance should be chosen (proper collector current I_C and V_{CE}). in the circuit.
- The process of choosing proper voltages and resistances to obtain desired operating point or Q-point of transistor is called biasing and the ckt used for transistor biasing is called as biasing ckt.

There are 4 conditions to be met by transistor to act as faithful amplifier

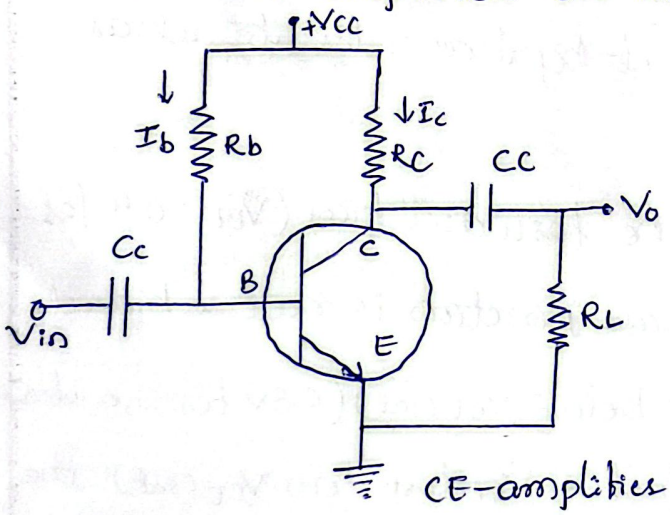
1. Emitter base junction must be forward bias ($V_{BE} = 0.7$ for Si, 0.2V for Ge) and collector base junction is reverse biased.
2. V_{CE} voltage should not fall below $V_{CE(sat)}$ (0.3V for Si, 0.1V for Ge) for any part of the i/p signal. for V_{CE} less than $V_{CE(sat)}$ the collector base junction is not probably reverse biased.
3. The value of I_C is at least equal to maximum when no signal is applied.

4. The maximum rating of transistor $I_{C(max)}$, $V_{CE(max)}$ and $P_{D(max)}$ should not be exceeded at any value of input signal

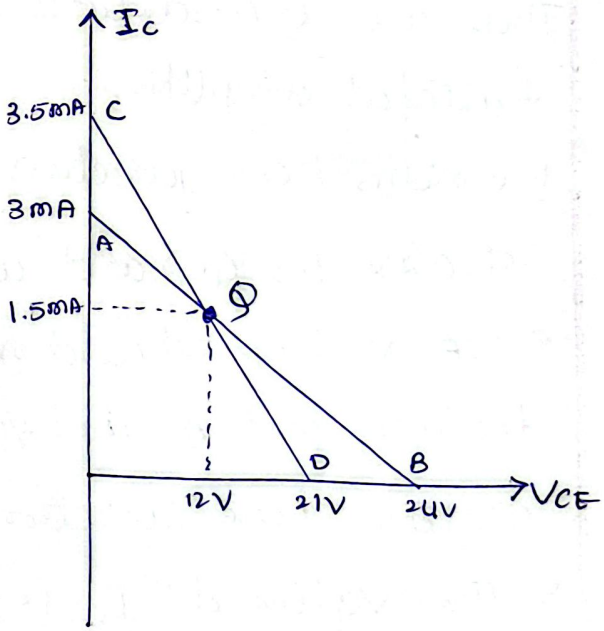
- To achieve faithful amplification the input junction must be properly forward biased and o/p junction must be reverse bias.
- There are three types of Biasing techniques/circuits.
  1. Fixed bias (or) Base bias.
  2. Collector to base bias (or) biasing with feed back resistor.
  3. Self bias (or) Voltage divider bias (or) Universal bias

DC load line

- From the circuit, the values of V_{CC} and R_C are fixed and I_C, V_{CE} are depends on R_B.



CE-amplifier circuit



Apply KVL to the collector circuit

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C$$

- The straight line represented by AB is called DC load line. The coordinates of the end point A is obtained by substituting $V_{CE}=0$ in above equation, then $I_C = \frac{V_{CC}}{R_C}$
  Therefore the coordinates of A are $(0, \frac{V_{CC}}{R_C})$
- The coordinates of B are obtained by substituting $I_C=0$ in above equation, then $V_{CE} = V_{CC}$
  Therefore the coordinates of B are $(V_{CC}, 0)$
- Thus the d.c load line drawn if the values of R_C and V_{CC} are known.
- The optimum point / Q-point located at the midpoint of d.c load line AB. between the saturation and cut off regions.
- In order to get faithfull amplification, the Q-point must be within the active region of transistor.
- It is very important to ensure that the operating point remains stable where it is originally fixed.
- If Q-point shifts nearer to either A or B, the output voltage and currents get clipped, there by o/p signal is distorted.
- In practice, the Q-point tends to shift its position due to any or all of the following reasons.

1. Reverse saturation current I_{CO}, which doubles for every $10^{\circ}C$ raise in temperature.

2. Base emitter voltage V_{BE} which decreases by $2.5 mV/^{\circ}C$

3. Transistor current gain, h_{fe} or β which increases with temperature.

AC load line:- The a.c load line also pass through the operating point. the effective a.c load resistance $R_{a.c}$ is combination of R_C and R_L i.e $R_{a.c} = R_C // R_L$

- The slop of a.c load line CQD will be $\left(-\frac{1}{R_{a.c}}\right)$
- To draw an a.c load line two end points maximum V_{CE} and maximum I_C (i.e AC saturation point and cut off point)
- The saturation point is at coordinate $(0, I_{Csat})$ and cut off point at $(V_{CEoff}, 0)$

⇒ Saturation point: $(0, I_{Csat})$ where

$$I_{Csat} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} \quad \text{(at point 'C')}$$

⇒ cut off point: $(V_{CEoff}, 0)$ where

$$V_{CEoff} = V_{CEQ} + I_{CQ} \cdot R_{a.c} \quad \text{(at point D)}$$

- By joining points C and D, a.c load line CD constructed

As $R_C > R_{a.c}$, the dc load line is less steep than the a.c load line.

- The intersection of d.c and a.c load lines is the operating point 'Q'

stability factor (S)

- The collector current I_C is stabilised with varying I_{CO} is measured by a stability factor 'S'. It is defined as the rate of change of collector current I_C with respect to the collector base leakage current I_{CO}. by keeping I_B and β are constant.

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}, \quad \beta \,\&\, I_B \text{ constant} \quad \text{——— (1)}$$

- The collector current for a CE amplifier is given by

$$I_C = \beta I_B + (\beta+1) I_{CO} \quad \text{——— (2)}$$

Differentiate above equation w.r.t I_C

$$1 = \beta \frac{dI_B}{dI_C} + (\beta+1)\frac{dI_{CO}}{dI_C}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta+1)}{S} \qquad \left[\because S = \frac{dI_C}{dI_{CO}}\right]$$

$$\boxed{S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}} \quad \text{——— (3)}$$

- From the above equation it is clear that the stability factor (S) should be small as possible to have better stable thermal stability.

stability factors S' and S'' :-

- The stability factor S' is defined as the rate of change of I_C with V_{BE}, by keeping I_{CO} and β constant

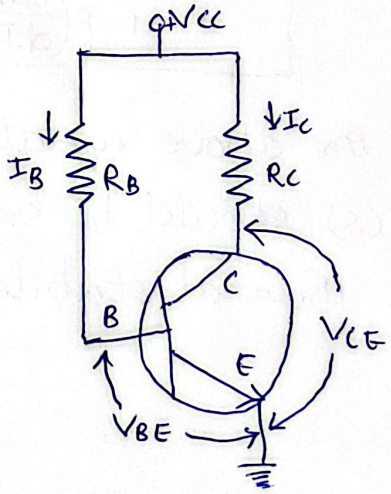
$$\boxed{S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}}$$

- The stability factor S'' is defined as the rate of change of I_C with respect to β, keeping I_{CO} and V_{BE} constant

$$\boxed{S'' = \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta}}$$

Fixed bias/ Base Bias

- The Figure shows a fixed bias circuit.
- Here the input junction is forward biased and output junction is reverse biased. through base resistor
- ~~VCE~~, V_{BE}, V_{CC}, R_B are fixed values.



- Apply KVL to input loop

$$V_{CC} = I_B R_B + V_{BE} \quad \text{—— (4)}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

- Apply KVL at o/p loop

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

- Since the equation $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ is independent of current I_C, $\frac{\partial I_B}{\partial I_C} = 0$

- Then stability factor $S = \left(\frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}\right)$ reduces to $(1+\beta)$

$S = 1+\beta$ (Fixed bias)

if $\beta = 100$

$S = 1+100 = 101$

- The change in collector current is 101 times of reverse saturation current. which is undesirable

- In this method β, V_{CC} are fixed values hence it is known as fixed bias method.

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}, \quad \frac{\partial I_B}{\partial I_C} = 0$$

$$R_B = \frac{V_{CC}}{\frac{I_C}{\beta}}$$

<u>Advantages:-</u>

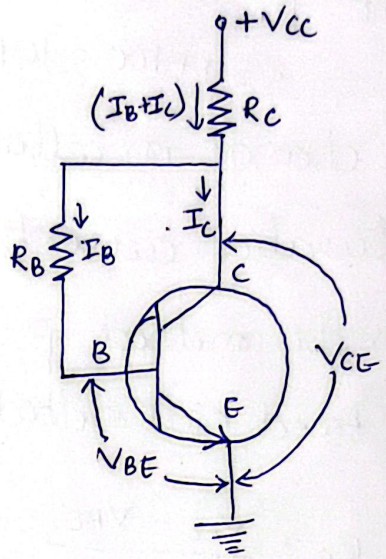
1. Simplicity
2. small number of components required
3. If supply voltage very large as compared to V_{BE}, then the base current becomes largely independent of the voltage V_{BE}

Disadvantage :-

1. There is no stability
2. There is no protection for transistor against temparature variations.

Collector to base bias / Biasing with feedback resistor.

- The collector to base bias circuit shown in the figure is with common emitter mode.
- The input junction is forward biased and output junction is reverse biased through feed back resistor R_B.
- through feed back resistor R_B Collector is connected to base
- The circuit provides stability against temparature variations.



- From input loop

$$V_{CC} = (I_C + I_B)R_C + I_B R_B + V_{BE} \quad \text{——— (5)}$$

$$V_{CC} = I_C R_C + I_B(R_B + R_C) + V_{BE}$$

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_B + R_C} \quad \text{——— (6)}$$

Differentiate above equation with respect to I_C

$$\frac{dI_B}{dI_C} = -\frac{R_C}{R_C + R_B} \quad \text{——— (7)}$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)} \qquad \left[\because S = \frac{1+\beta}{1+\beta\left(\frac{dI_B}{dI_C}\right)}\right] \quad \text{——— (8)}$$

- The value of stability factor is smaller than fixed bias circuit. The stability can be improved by making R_B smaller or R_C large
- If R_C is very small then $S=(\beta+1)$ i.e stability is very poor. hence the value of R_C must be quite large for good stabilization.

Advantages:-

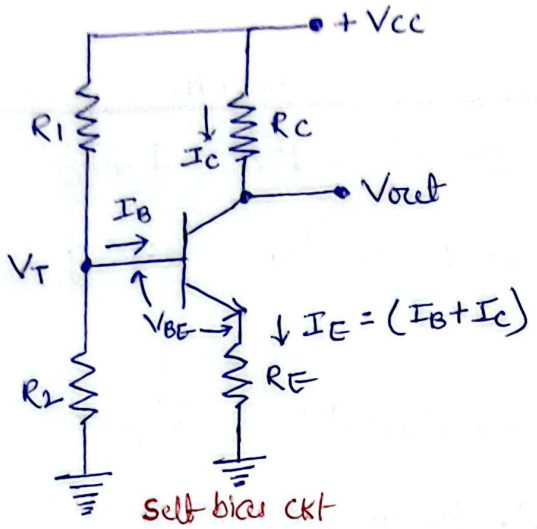
1. The circuit provides stability against temparature variations

Disadvantages:-

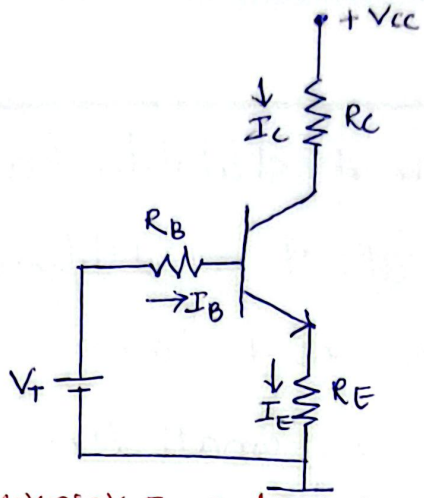
1. Gain decreases, output is connected to input

Self bias / Voltage divider bias/Universal bias./Emitter Bias.

- It is a simple circuit used to establish a stable operating point is the self biasing configuration.
- The self bias circuit have two biasing resistors R_1 and R_2 R_E is emitter resistor and R_C is collector resistor
- Input junction is forward biased and output junction is reverse biased through biasing resistors R_1 and R_2
- R_1 and R_2 forms a potential divider across V_{CC} to achieve best stability R_1 and R_2 must be small.
- The required base bias is obtained from the power supply through the potential divider network of R_1 and R_2



Self bias ckt



Thevenin's Equivalent ckt

→ Use of self bias circuit as constant current circuit

- If I_c tends to increase, due to increase in I_{co} with temperature, the current in R_E increases.

If $I_{co}\uparrow$, $I_c\uparrow$, $I_E\uparrow$

- Hence voltage drop across R_E increases thereby decreasing the base current $V_{RE}\uparrow$, $V_{R_2}\uparrow$, $I_B\downarrow$

as a result, I_c is maintained almost constant

Applying Thevenin's theorem

$$V_T = \frac{R_2 V_{cc}}{R_1+R_2} \quad \text{and} \quad R_B = \frac{R_1 R_2}{R_1+R_2}$$

The loop equation around the base circuit can be written as

$$V_T = I_B R_B + V_{BE} + (I_B+I_c)R_E$$

Differentiate above equation w.r.t I_c

$$\frac{dI_B}{dI_c} = -\frac{R_E}{R_B+R_E}$$

stability factor $$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)} = (1+\beta)\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}} \quad \text{—— (9)}$$

- The value of S is equal to one of the ratio R_B/R_E is very small as compared to 1

- As this ratio becomes comparable to unity and beyond towards infinity, the value of stability factor goes on increasing till $S = 1+\beta$
- The stability factor for self bias circuit is equal to one this can be achieved with proper design

Advantage:-

1. Good stability.

Disadvantage:-

1. output voltage coupled with input through emitter resistor
2. There is a possibility for the reduction of Gain
3. To overcome reduction of gain emitter bypass capacitor is connected across RE.

Name of the bias	Advantage	Disadvantage
Fixed bias	Easy to design	poor stability
collector to base bias	Good stability can be achieved with proper design	Reduction in Gain
Voltage Divider bias	Excellent stability. Stability factor = 1	Good gain By Keeping emitter bypass capacitor reduction of gain can be eliminated

To determine stability factor S'

- The stability factor S' is defined as the rate of change of I_C with V_{BE}, by keeping I_{CO}, β constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \simeq \frac{\Delta I_C}{\Delta V_{BE}}$$

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$= I_B[R_B + R_E] + I_C R_E + V_{BE} \quad (\because I_E = I_B + I_C) \quad \text{——— (10)}$$

From eq (2)

$$I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta} \quad \text{——— (11)}$$

substitute equation (11) in equ (10)

$$V_T = \frac{I_C}{\beta}(R_B + R_E) + V_{BE} + I_C R_E + \frac{I_{CO}}{\beta}(1+\beta)\{R_B + R_E\} \quad \text{— (12)}$$

Differentiate above equation w.r.t to V_{BE}

$$0 = \frac{dI_C}{dV_{BE}}\left(\frac{R_B + R_C}{\beta}\right) + 1 + R_E\left(\frac{dI_C}{dV_{BE}}\right) + 0$$

$$-1 = \frac{dI_C}{dV_{BE}}\left[\frac{R_B + (1+\beta)R_E}{\beta}\right]$$

$$\boxed{\therefore S' = \frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B + (1+\beta)R_E}} \quad \text{——— (13)}$$

To determine the stability factor S''

- The stability factor S'' is defined as the ratio of change of I_C w.r.t to β, by keeping I_{CO} and V_{BE} constant.

Reassange equation (12)

$$I_C = \frac{\beta(V_T - V_{BE})}{R_B + (1+\beta)R_E} + \frac{\beta\left(\frac{1+\beta}{\beta}\right) I_{CO}(R_B + R_E)}{R_B + (1+\beta)R_E} \quad \text{——— (14)}$$

Since $\beta >> 1$, then the numerator of the second term can be written as $(R_B+R_E)\left(\frac{1+\beta}{\beta}\right)I_{CO} \approx (R_B+R_E)I_{CO}$ ——— (15)

substitute equation (15) in (14)

$$I_C = \frac{\beta(V_T - V_{BE})}{R_B + (1+\beta)R_E} + \frac{\beta(R_B+R_E)I_{CO}}{R_B+(1+\beta)R_E}$$

$$\therefore \quad I_C = \frac{\beta(V_T - V_{BE} + (R_B+R_E)I_{CO}}{R_B + (1+\beta)R_E}$$

Let $V' = (R_B + R_E)I_{CO}$

$$\therefore \quad I_C = \frac{\beta(V_T - V_{BE} + V')}{R_B + (1+\beta)R_E} \quad \text{——— (16)}$$

Differentiate above equation w.r.t β and and simplified

$$S'' = \frac{dI_C}{d\beta} = \frac{I_C}{\beta\left[1+\beta\left(\frac{R_E}{R_E+R_B}\right)\right]} = \frac{SI_C}{\beta(1+\beta)} \quad \text{——— (17)}$$

Thermal Runaway:-

- The maximum power dissipation may lie in the range of few milli watts to 200 watts
- This maximum power is limited by collector junction that it can withstand.
- For silicon transistor 150° to 225°C for germanium 60°C to 100°C

- The junction temperature may raise either because of ambient temperature or because of self heating.
- As the junction temperature increases, I_{CO} increases which will further increase I_C. Again heat dissipates causing the temperature to increase.
- It is a cumulative process, which will cause the transistor to burn out.
- The collector current for CE circuit is given by

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

- The three variables β, I_B and I_{CO} increases with rise in temperature.
- In particular, the reverse saturation current or leakage current I_{CO} change with temperature. specially it doubles for every 10°C rise in temperature.
- The collector current I_C causes the temperature increase at collector base junction, increase I_{CO}, as a result I_C also increase
- This process cumulatively leading to thermal runaway
- If ratings of transistor are exceeded which may destroy the transistor itself. the emitter in order to help dissipate the heat developed at collector junction.
- The base current I_B is decrease automatically with rise in temperature then the decrease in βI_B will compensate for increase in $(1+\beta) I_{CO}$, by keeping I_C almost constant.

ROLL No ..... SHEET No. .....

- In power transistors, the heat developed at the collector junction may be removed by use of heat sink, which is a metal sheet fitted to the collector and whose surface radiates heat quickly.