Design of Pipelined RISC Processor

(Self Project submission for resume verification)

Name: Aditya Ajay Wani **Roll No: 193079020**

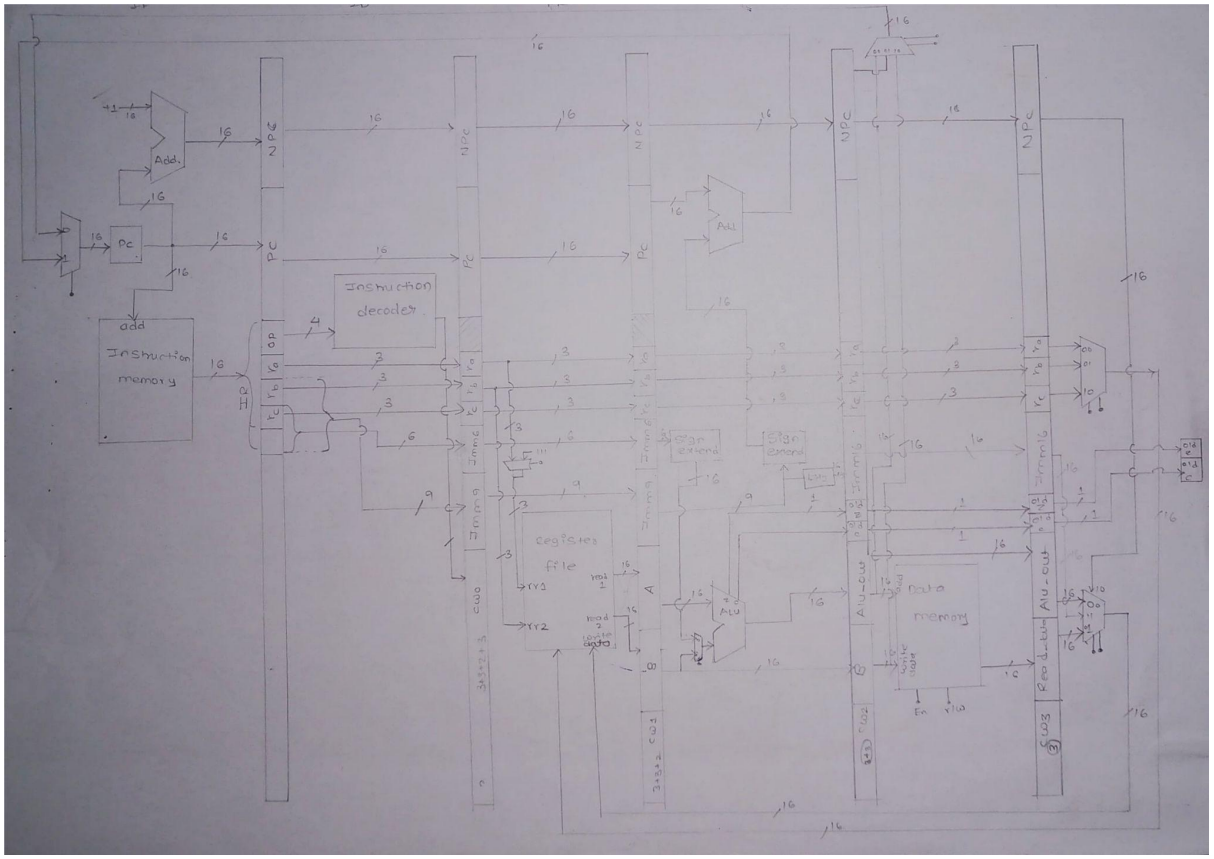
Github Repo: https://github.com/25Aditya25/IITB-Risc

Introduction:

This implementation of 6 stages pipelined processor is based on the problem statement given as a project for the course EE739 Processor Design at IIT Bombay by Prof. Virendra Singh.

The 16 bit ISA used is called IITB-RISC and has 15 instructions consisting of R, I, and J type instructions, 8 registers, branch predictor, and multi-cycle instructions. The architecture is based on the Little computer architecture.

Pen-Paper implementation:



Sorry about the visibility. The thing was drawn with a pencil and more than 16 months ago. The pen-paper implementation was to get an overview of the implementation. The Verilog implementation is behavioral and was done with different variable names.

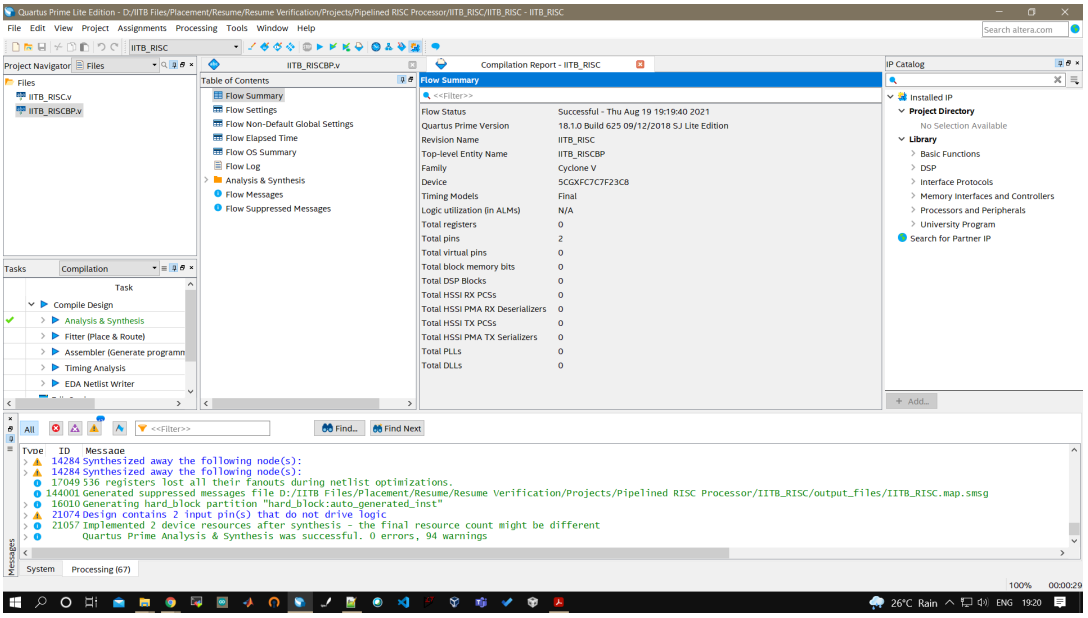
Verilog Implementation:

The file *IITB_RISCBP.v* contains the top-level entity *IITB_RISCBP*. This is a behavioral description of the module. The IITB_RISCBP module consists of 6 always blocks each concerning one of the 6 stages of the pipeline.

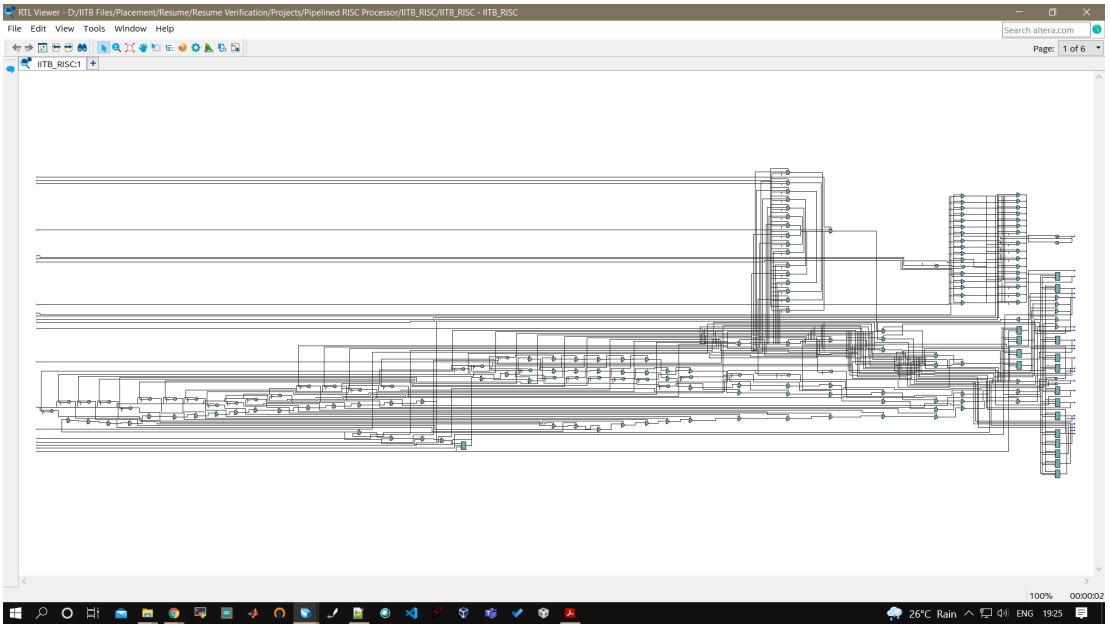
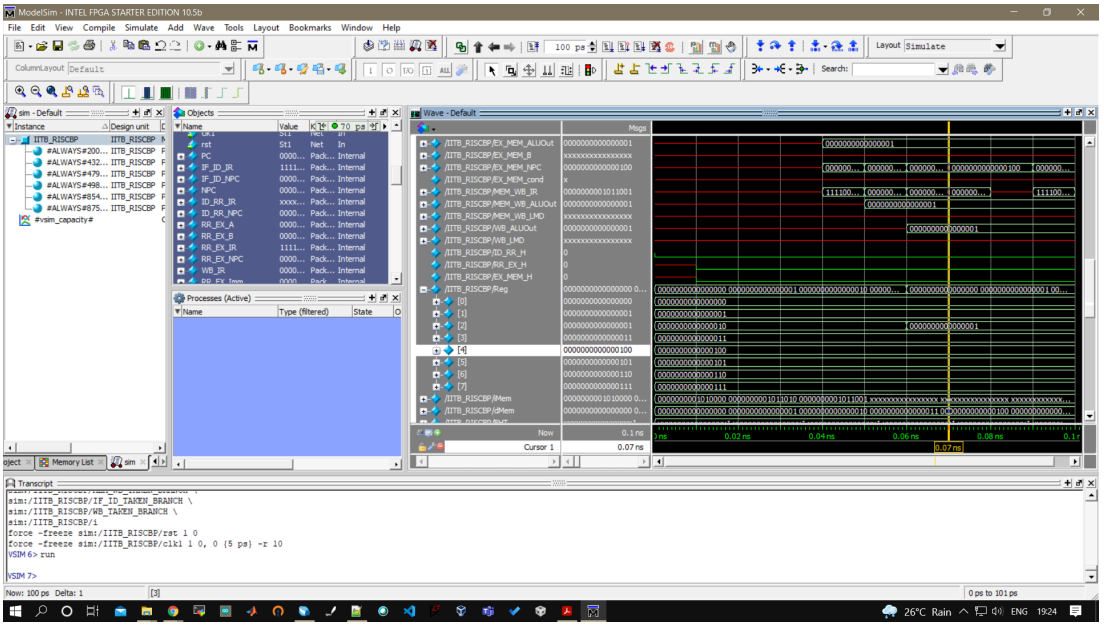
The initialization of the instruction and data memory is done in the initial block. The code has some commented-out instruction sequences that were used to verify the functionality of the design. The Data hazards for different instruction type combinations were identified and resolved using data forwarding wherever possible.

A branch history table was implemented with 1 bit to store history and the pc address.

The Quartus implementation screen is shown below:



The netlist view in Quartus is shown below:



The modelsim implementation screenshot is shown below: