Mike Mock

TI Designs – Precision: Verified Design

0-1A, Single-Supply, Low-Side, Current Sensing Solution Reference Design

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Circuit Description

This single-supply, low-side, current sensing solution accurately detects load current between 0 and 1A. The OPA320 features wide bandwidth and low offset voltage making it an excellent amplifier for this design. With a single 5V supply, the LM7705 negative bias generator extends the linear output range of the amplifier below 0V. This enables the op-amp to produce a linear output for a zero-input current condition. The wide sensing range of the design allows for precise measurement of small load-currents (i.e. low-power or shutdown modes) as well as higher currents up to 1A.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
OPA320	Product Folder
LM7705	Product Folder

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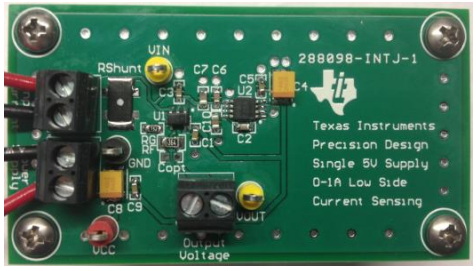
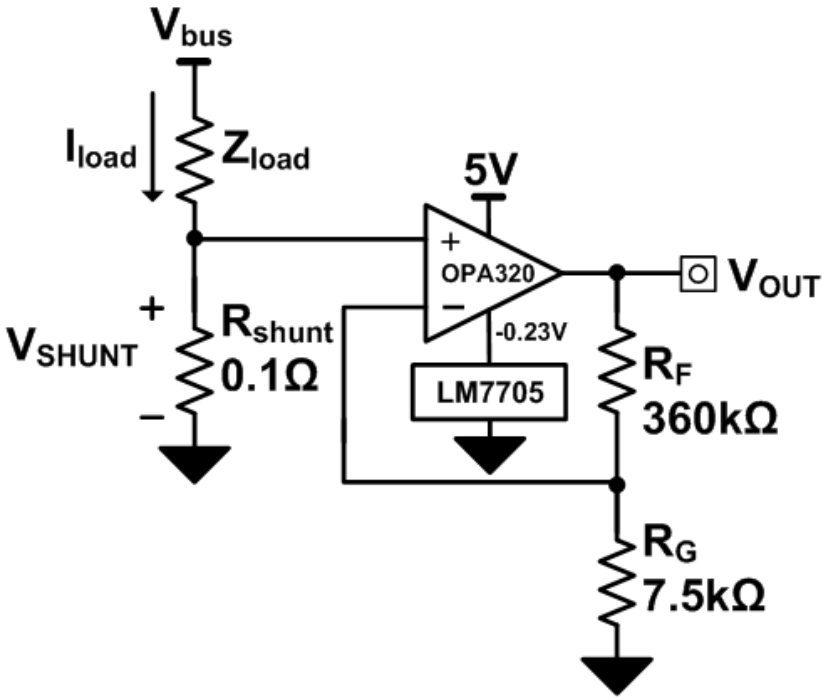


PCB is shown to scale.
Dimensions are 2.45" (L) x 1.35" (W)



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1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5 V
- Input: 0 – 1A
- Output: 0 – 4.9 V
- Maximum Shunt Voltage: 100 mV

The design goals and measured performance are summarized in Table 1. The plot in Figure 1 contains 1,000 calibrated operating points of the circuit's measured dc transfer function. As shown in Figure 2, the circuit is accurate to within ±0.003% full-scale error after applying a 2-point calibration. A description of the circuit's uncalibrated performance is included in Appendix A.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Uncalibrated	Calibrated
Full Scale Range Error (0-1A)	±0.1%	±0.108%	±0.055%	±0.003%
Zero-Current Error	±0.1%	-0.034%	-0.052%	-0.0002%

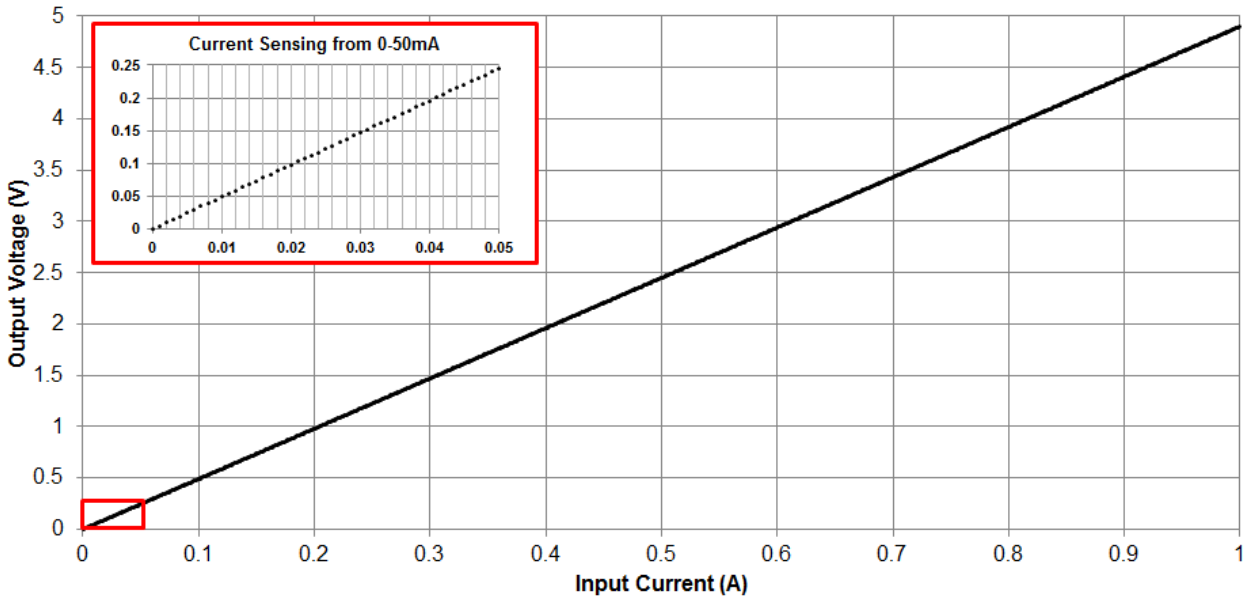

Figure 1. Calibrated DC Transfer Function (V_{OUT} vs. I_{IN})

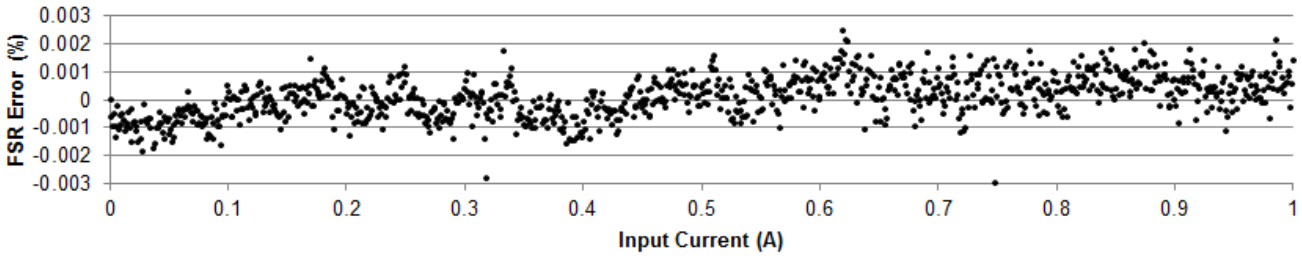

Figure 2. Calibrated Full-Scale Range Error vs. Input Current

2 Theory of Operation

This low-side current sensing solution uses the LM7705 with a rail-to-rail op-amp (U1) to accurately sense load-current between 0-1A. A simplified schematic for the circuit is shown below in Figure 3. The transfer function detailing the relationship between V_{OUT} and I_{LOAD} is shown in Equation 1.

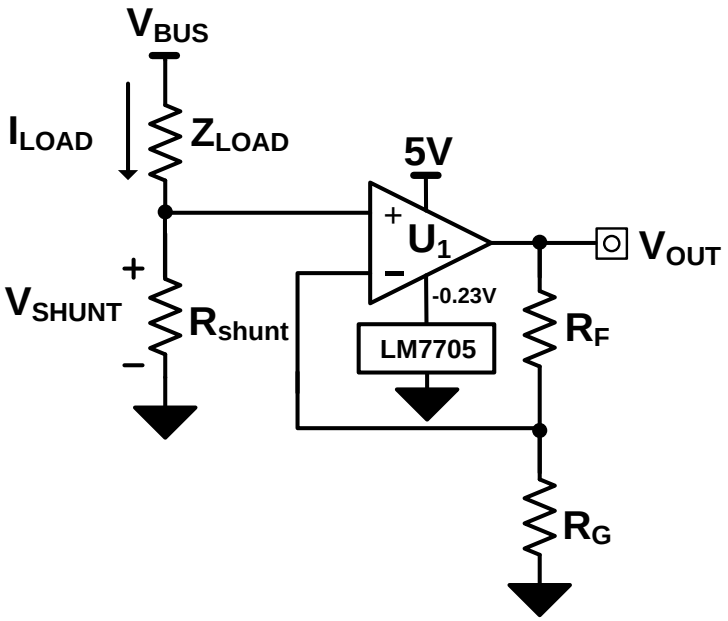

Figure 3. Simplified Schematic of Low-Side Current Sensing Solution

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \left(1 + \frac{R_F}{R_G}\right) \quad (1)$$

2.1 Sources of Output Error

The physical construction of the circuit and the component tolerances will introduce error in the transfer function. A schematic, with several practical sources of error, is shown in Figure 4.

2.1.1 *Gain Error*

The largest source of gain error comes from the tolerance of $R_{SHUNT,}$ R_F and $R_{G.}$ Small trace impedance in a poorly placed Kelvin connection, R_{KELVIN}, will also add additional gain error. Any potential, V_{GND}, between GND and the low-side of R_G will introduce gain error in the output. The effect of gain error appears as a change in the slope of the transfer function as shown in Figure 5 (left).

2.1.2 *Offset Error*

The amplifier's offset voltage (V_{OS}) is the dominant source of offset error in this design. The magnitude of offset error at the output will equal the product of the amplifier's gain and offset voltage. Ideally, the offset error is linear across the entire input range and appears as a vertical shift (up or down) in the transfer function as shown in Figure 5 (right).

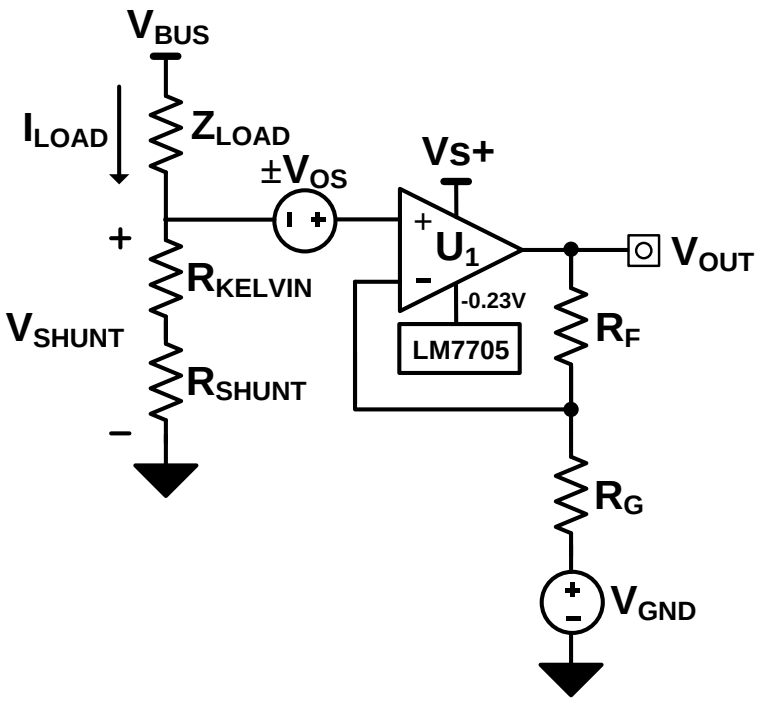

Figure 4. Schematic Showing Sources of Output Error

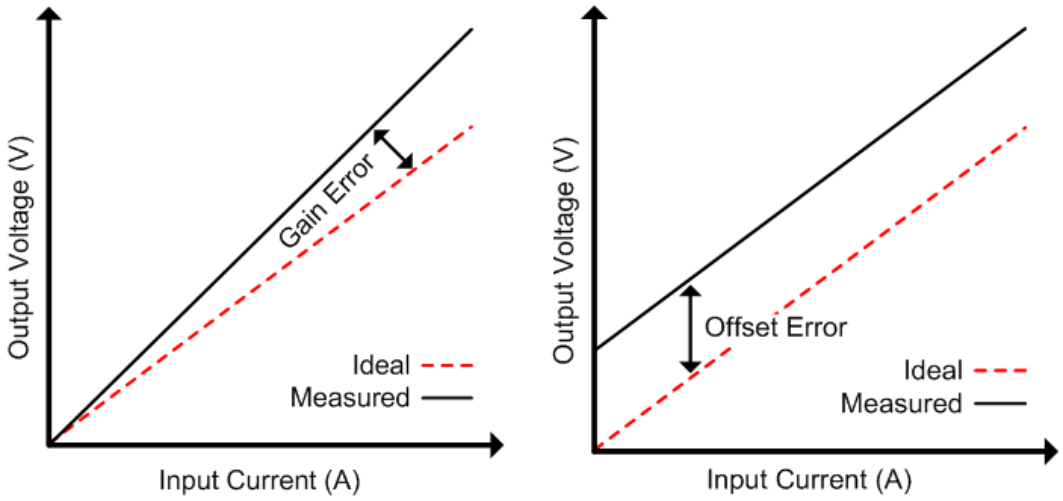

Figure 5. Gain Error (Left) and Offset Error (Right)

2.1.3 *Removing Error with Calibration*

A 2-point calibration is used in this design to remove linear sources of gain and offset error in the dc transfer function. A description of the calibration procedure is included in Appendix A.

2.1.4 *Full-Scale Error*

The full-scale error (%FSR) of the output is calculated using Equation 2.

$$\text{Full-Scale Error (\%FSR)} = 100 \times \frac{V_{OUT\_MEASURED} - V_{OUT\_IDEAL}}{V_{OUT\_IDEAL\_MAX} - V_{OUT\_IDEAL\_MIN}} \quad (2)$$

2.1.5 *Output Voltage Swing*

For most single-supply applications, the negative power supply (V_{S-}) is fixed at GND or 0V. Output stage limitations of the amplifier will induce non-linear saturation as the output approaches the negative supply. A depiction of this near-zero saturation is shown in Figure 6. A 2-point calibration will only remove linear sources of gain and offset error and will not cancel the zero-current error. In order for the amplifier to create a linear output down to 0V, the negative supply must be at least 100mV less than system GND. The LM7705 inverting charge pump generates a -0.23V supply for this purpose.

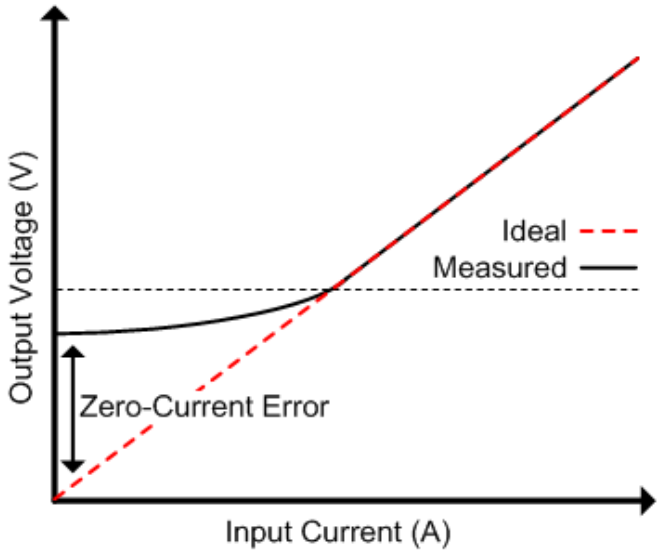

Figure 6. Output Saturation near the Negative Supply Rail

3 Component Selection

3.1 Amplifier

This design requires an amplifier with a rail-to-rail input/output and a relatively low offset voltage. To sense current within a wide frequency range, the OPA320 was chosen for its bandwidth and low offset voltage. Datasheet specifications that benefit the design are listed in Table 2. As shown, the OPA320 has a maximum offset voltage of 150 µV and a unity-gain bandwidth of 20MHz.

Table 2. OPA320 Datasheet Specifications

Amplifier	Max Supply Voltage (V)	Max Quiescent Current (µA)	Max Offset Voltage (µV)	Max Offset Drift (µV/ºC)	Bandwidth (MHz)	Output Swing (mV from Negative Rail)
OPA320	5.5	1750	150	5	20	20

3.2 LM7705

The LM7705 functions as an inverting charge pump and regulates its output to -0.23V when powered from a single supply. By biasing the negative supply (V_S-) of the op-amp to -0.23V, the linear output range of the device is extended below 0V. A linear output at 0V allows a calibrated measurement of zero-input current as shown in Figure 7.

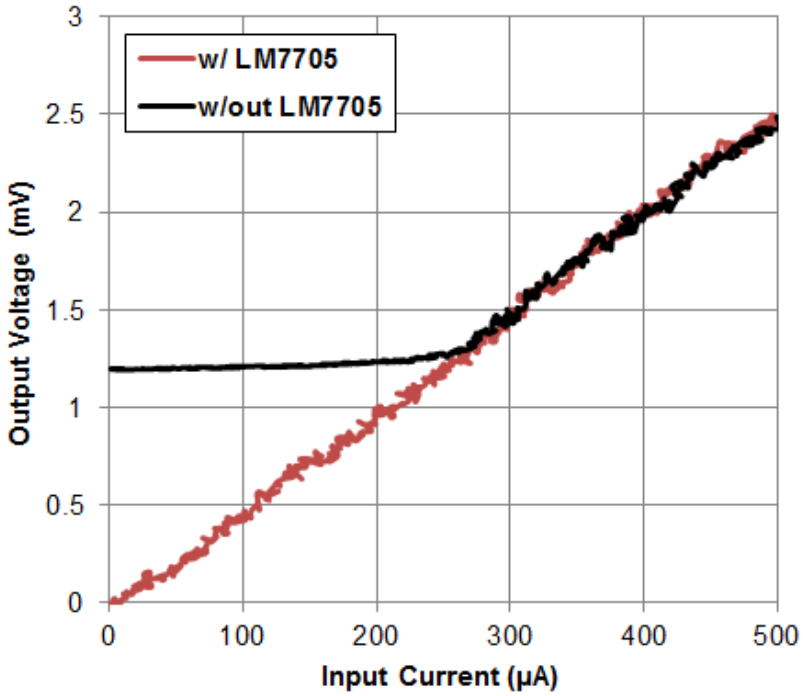

Figure 7. Measured Output Saturation w/out the LM7705

3.3 Shunt Resistor

To keep the shunt voltage, V_{SHUNT}, below 100mV at maximum load current, the largest shunt resistor value was defined using Equation 3.

$$R_{SHUNT\_MAX} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (3)$$

To maximize V_{SHUNT} for a given load current, a 100mΩ (±0.1%) shunt resistor was selected for this design. At max load current, the shunt will dissipate 100mW.

3.4 Gain-Setting Resistors

After selecting R_{SHUNT} to be 100mΩ, the maximum V_{SHUNT} is limited to 100mV at 1A load current. The resistors in the feedback network of the amplifier, R_F and R_G, were chosen to provide a fixed gain of 49 V/V which increases the output range to the desired 0-4.9V.

The closest ratio of manufactured resistor values that provides a non-inverting gain of 49 V/V was a 360kΩ (±0.05%) resistor for R_F and a 7.5kΩ (±0.05%) for R_G as shown in Equation 4.

$$Gain = 1 + \frac{R_F}{R_G} = 1 + \frac{360k\Omega}{7.5k\Omega} = 49\frac{V}{V} \quad (4)$$

3.5 Other Components

Other components included in the design were standard decoupling capacitors and the passives used in the LM7705 circuitry. The values selected for the LM7705 circuit were standard components recommended in the datasheet and product evaluation board documentation. Large 10µF tantalum bulk-capacitors were placed directly at the board's power supply connection as well as the input to the LM7705. When possible, passives were selected in 0603 packages to minimize the footprint of the circuit.

4 Simulation

A simulation of the circuit was performed using TINA-TI™ software. The schematic used in simulation is shown in Figure 8. The LM7705 was simulated by placing a -230mV voltage reference (V2) at the negative rail of the OPA320.

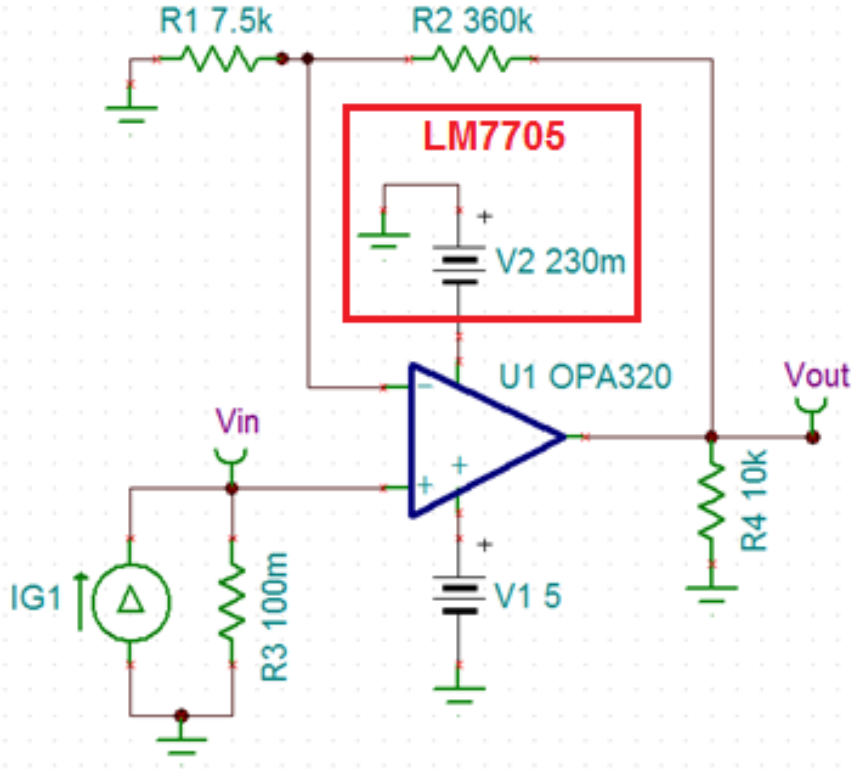

Figure 8. TINA-TI™ Simulation Schematic

4.1 Simulated DC Transfer Function

The simulated dc transfer function is shown in Figure 9. Using ideal component values, the simulation shows uncalibrated performance of -1.655mV at zero-input current and 4.898V at 1A.

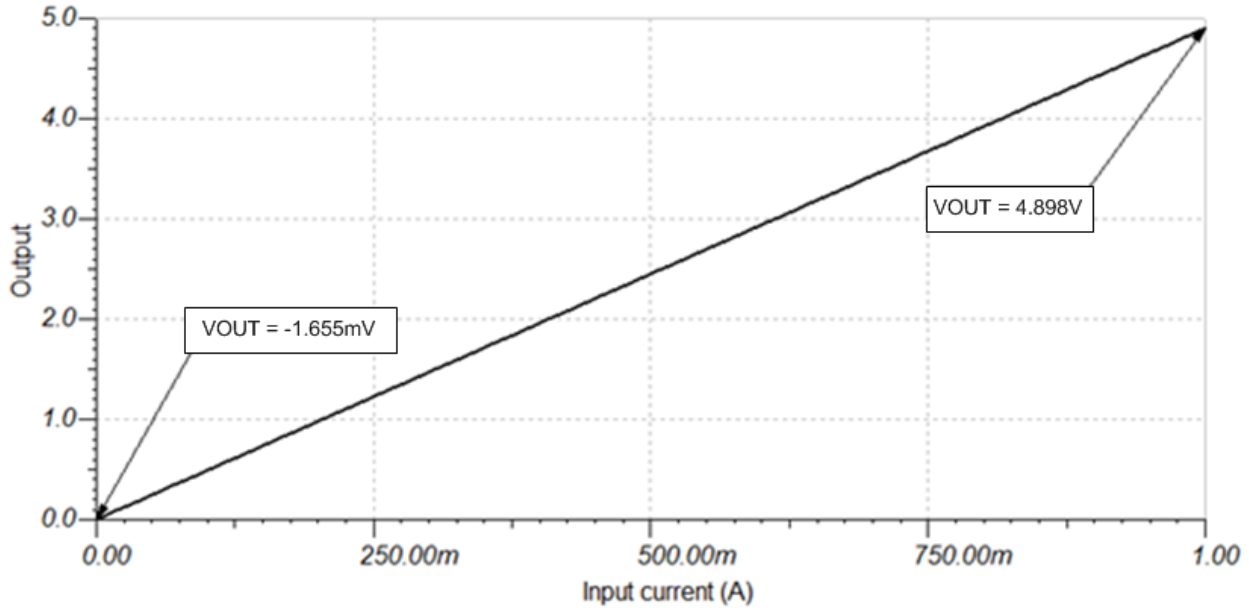

Figure 9. Simulated Transfer Function (V_{OUT} vs. I_{IN})

4.2 Monte Carlo Simulation

To analyze error due to the tolerance of R_{SHUNT}, R_F, and R_G, a 1,000 point Monte-Carlo simulation was run at 0A and 1A input current. The results of the Monte-Carlo simulation are shown in Table 3.

Table 3. DC Transfer Results from Calibrated Monte-Carlo Analysis

	Average (μ)	Std. Dev. (σ)	Nominal
V_{OUT} (V) at 0A	-1.655041m	224.104785n	-1.655052m
V_{OUT} (V) at 1A	4.898204	1.175525m	4.898282

Using the mean (μ) and standard deviation (σ) from the Monte-Carlo simulation, a Six Sigma (-3σ to 3σ) prediction of full-scale error (%FSR) is calculated using Equation 5.

$$\text{Percent Error (\%FSR)} = \frac{(\mu \pm 3\sigma) - V_{OUT\_EXPECTED}}{4.9} \times 100 \quad (5)$$

With 99.7% confidence, the maximum simulated full-scale error at 1A (full-scale range) is ±0.108%. The maximum simulated zero-current error is -0.034%.

4.3 Simulated Results Summary

The simulation results are compared against the design goals in Table 4.

Table 4. Design Goals with Simulated Performance

	Goal	Simulated
Full Scale Error	±0.1%	±0.108%
Zero-Current Error	±0.1%	-0.034%

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The two-layer printed circuit board (PCB) used in this design measures 2.45” x 1.35” as shown in Figure 10. The sensing circuitry occupies the top-copper layer. The bottom-copper layer contains a solid ground plane which provides a low-impedance path for return currents.

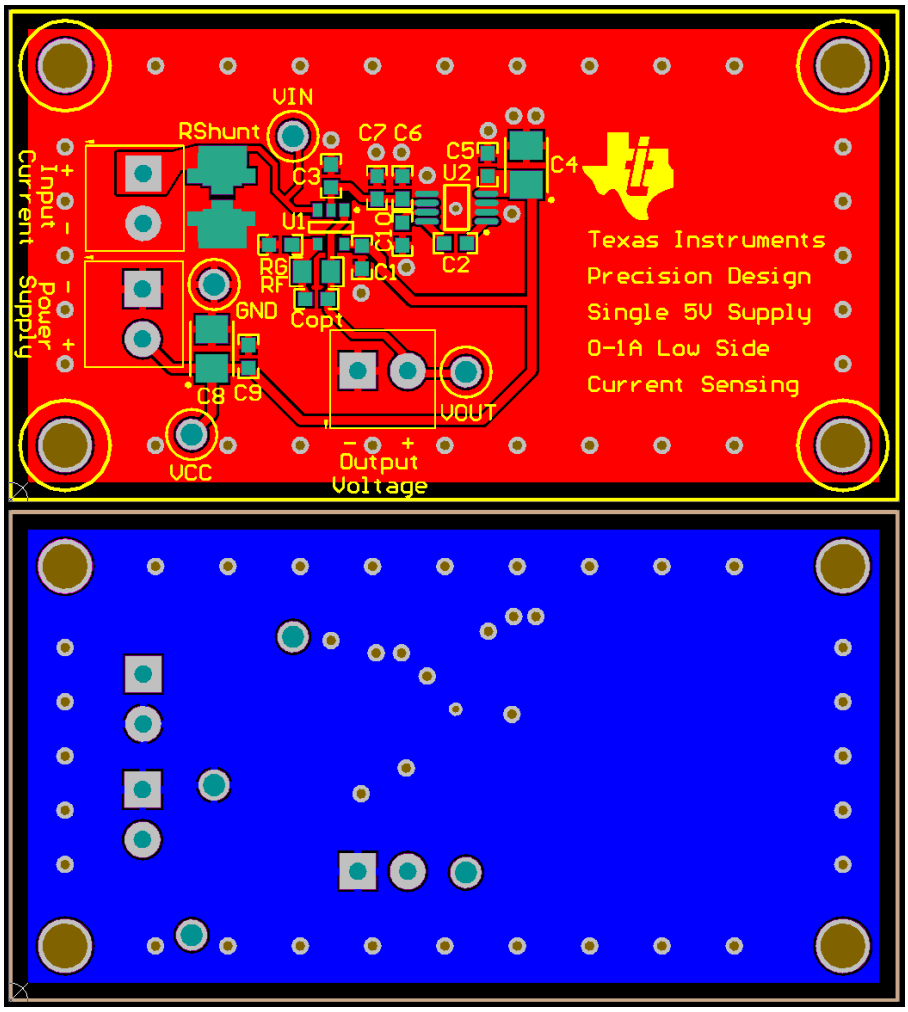

Figure 10. PCB Layout

5.2 PCB Layout Considerations

The terminal blocks for the input current and power supply share a common ground connection at the left side of the board. The shunt resistor, R_{SHUNT}, is located very close to the input terminal block. This shortens the path of load current on the PCB and minimizes the trace-impedance from R_{SHUNT} to GND. The op-amp’s feedback network (R_F and R_G) is positioned such that ground-side of R_{SHUNT} and R_G are near each other. This results in an accurate measurement across R_{SHUNT} using a single Kelvin connection and minimizes a potential source of gain error. The pad for R_{SHUNT} can fit any surface mount resistor between 0805 and 2512; however the placement of the Kelvin connection is optimized for a 2512 package. The output of the LM7705 is located near the negative supply pin of the op-amp, which minimizes the length of the connecting trace. All decoupling capacitors are placed near their designated power pins on the IC’s.

6 Verification & Measured Performance

A LabVIEW VI allowed for automated control (GPIB) of a source meter and two multimeters to measure dc transfer characteristics. A fixed 5V power supply provided power to the circuit. The automated testing setup allowed fast and repeatable measurement and analysis of the circuit's dc operating points across the entire input range of 0-1A. The circuit's uncalibrated performance is listed in Appendix A.

6.1 Measured DC Transfer Function

The output voltage was measured at 1,000 steps across the full range of current sensing (1mA/step). After post-processing with a 2-point calibration, the measured dc transfer function is shown in Figure 11.

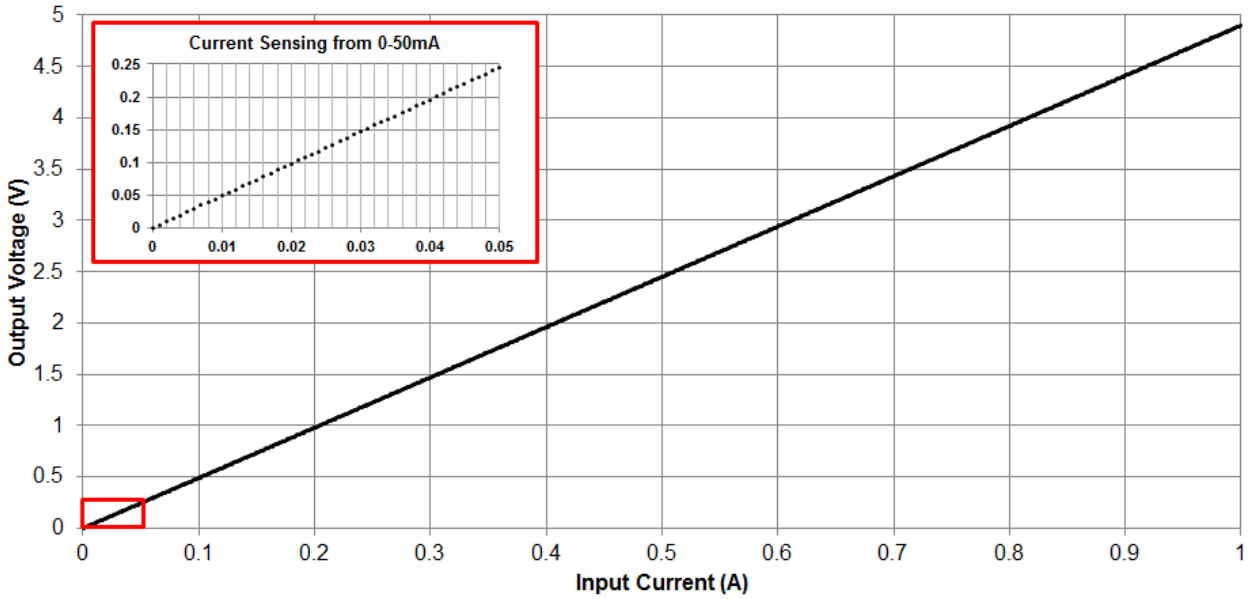

Figure 11. Calibrated DC Transfer Function (V_{OUT} vs. I_{IN})

6.2 Full-Scale Error Analysis

After calibration, the circuit's full-scale range error (%FSR) was calculated using Equation 2 and plotted over the input range in Figure 12. As shown, the calibrated circuit is capable of sensing load current within ±0.003% error across the entire input range.

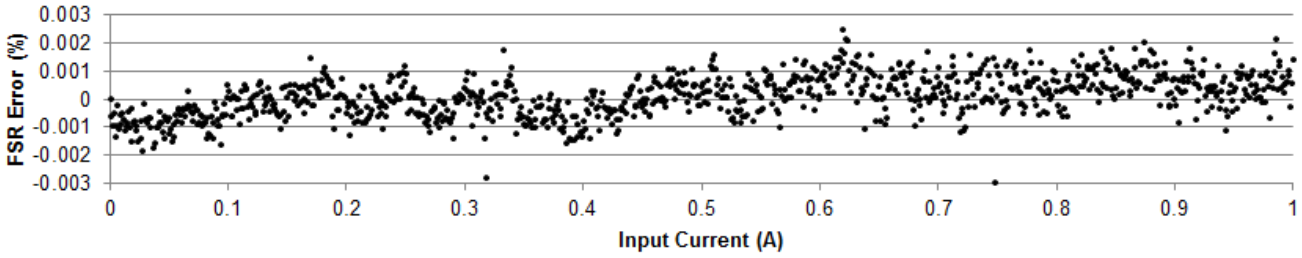

Figure 12. Calibrated Full-Scale Range Error vs. Input Current

6.3 Measured Results Summary

The measured results are compared against the design goals in Table 5.

Table 5. Measured Performance Summary

	Goal	Uncalibrated	Calibrated
Full Scale Range Error (0-1A)	±0.1%	±0.055%	±0.003%
Zero-Current Error	±0.1%	-0.052%	±0.0002%

7 Modifications

7.1 Alternative Components

Although the PCB pad for R_{SHUNT} can fit a variety of shunt resistors, the Kelvin connection is optimized for a 2512 package. Alternative shunt resistors can be selected to meet different application needs (i.e. power dissipation, current range, size, cost, precision, etc.). The tolerance of R_F and R_G can also be adjusted to increase uncalibrated accuracy or to minimize cost.

An optional capacitor C_{OPT} can be placed in parallel with R_F to introduce a pole in the circuit transfer function and reduce high frequency noise/bandwidth. The frequency of the pole is determined using Equation 6.

$$f_{POLE} = \frac{1}{2\pi \times R_F \times C_{OPT}} \quad (6)$$

A variety of precision amplifiers meet the rail-to-rail and low offset requirements for this design. Table 6 shows a comparison of several alternative amplifiers and their relevant specifications. Alternative amplifiers may be selected to meet the needs for many different applications (i.e. bandwidth, operating temperature, battery life, etc.) If wide bandwidth is not a concern and higher uncalibrated performance is desired, the OPA333 is an excellent alternative for this design.

If wide bandwidth is needed and a calibration is performed, the OPA322 is another option to decrease design costs while maintaining higher frequency performance.

Table 6. Alternative Op-Amps

Amplifier	Max Supply Voltage (V)	Max Quiescent Current (µA)	Max Offset Voltage (µV)	Max Offset Drift (µV/ºC)	Bandwidth (MHz)	Output Swing (mV from Negative Rail)	Cost ($/1ku)
OPA170	36	145	1800	2	1.2	8	0.4
OPA322	5.5	1900	2000	6	20	20	0.5
OPA376	5.5	950	25	1	5.5	20	0.65
OPA365	5.5	5000	200	1	50	20	0.65
OPA378	5.5	150	50	0.25	0.9	8	0.7
OPA320	5.5	1750	150	5	20	20	0.8
OPA333	5.5	25	10	0.05	0.35	50	0.95

7.2 Dual Power Supply

A dual supply enables an amplifier to easily output 0V without the LM7705. Using a dual power supply could be beneficial for bi-directional current sensing applications. Typically external components and increased cost are incurred when implementing a dual power supply in a design. For singe supply applications, the LM7705 biasing scheme improves the near-zero performance as shown in this design.

8 About the Author

Mike Mock joined the Applications Engineering Rotational Program at Texas Instruments in July 2013. He completed his first rotation with the Precision Linear Applications team in Dallas, Texas. Mike received his BSEE from Michigan State University.

9 Acknowledgements

The author would like to give a special thanks to Peter Semig and Collin Wells for their assistance and guidance throughout the design process, and to Greg Hupp for his assistance with the development the LabVIEW program used to collect the dc operating points used to measure the transfer function and error.

10 References

1. *P. Semig and C. Wells. (2012, February 8). A Current Sensing Tutorial Parts I-IV. Available: http://www.eetimes.com/design/industrial-control*

2. *B. Trump (2012, May 8). The Signal – Op-Amp Voltage Ranges – Input and Output. Available:*

   http://e2e.ti.com/blogs_/archives/b/thesignal/archive/2012/05/08/op-amp-voltage-ranges-input-and-output-clearing-some-confusion.aspx

Appendix A.

A.1 Uncalibrated Performance

The circuit's uncalibrated dc transfer function is shown in Figure 13. The output voltage at zero-load current was measured at -2.54mV which results in -0.052% full-scale error. At full-load current (1.00022A) the output measured was 4.90194V with approximately 0.02% full-scale error.

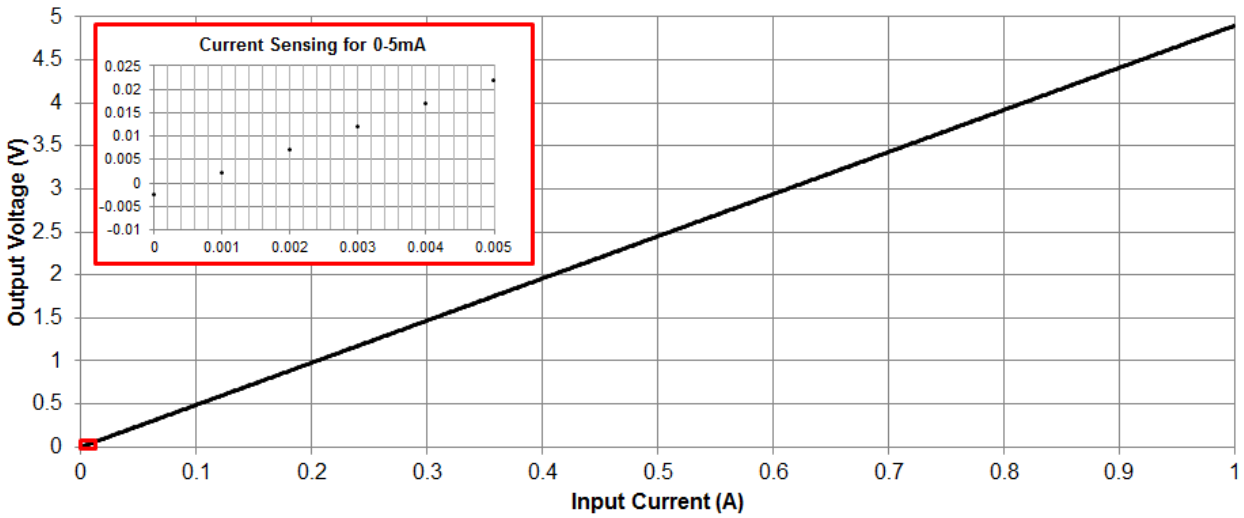

Figure 13. Uncalibrated DC Transfer Function (V_{OUT} vs. I_{IN})

A plot of full-scale error vs. input current is shown in Figure 14. As shown, the gain error and offset error are linear across the input range which allows them to be removed with a 2-point calibration.

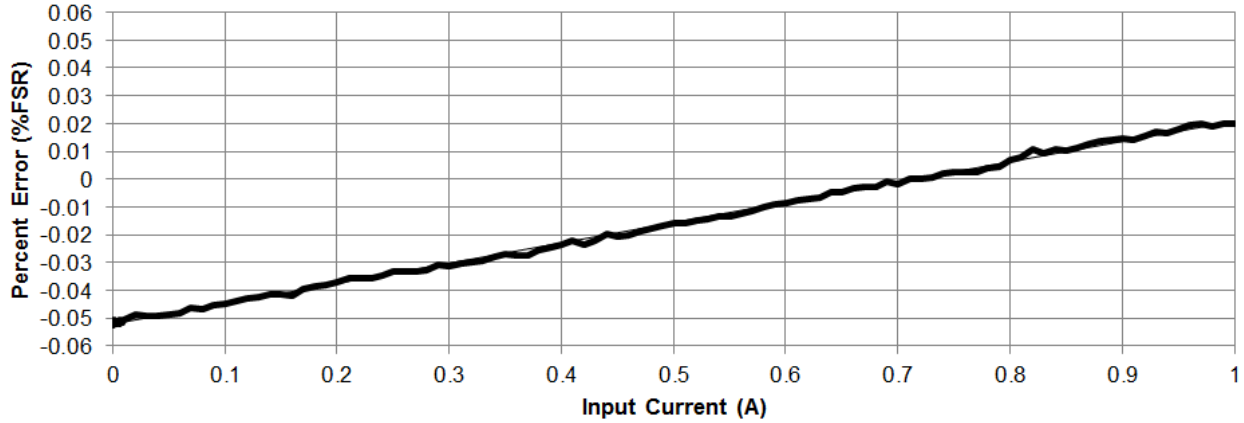

Figure 14. Uncalibrated Full-Scale Range Error vs. Input Current

A.2 Uncalibrated Results Summary

The uncalibrated results are compared against the design goals in Table 7.

Table 7. Uncalibrated Performance Error Summary

	Goal	Uncalibrated	Calibrated
Full Scale Range Error (0-1A)	±0.1%	±0.055%	±0.003%
Zero-Current Error	±0.1%	-0.052%	±0.0002%

A.3 2-Point Calibration

A 2-point calibration applied in post-processing can essentially remove linear sources of gain and offset error. Only two measured points of the circuit's dc transfer function (B_1 and B_2) are needed. For this circuit, the calibration measurements are taken at 0A and 750mA load current. With input current as the independent variable (X) and output voltage as the dependent variable (Y), the two measurements B_1 and B_2 are defined below and shown in Figure 15.

$$B_{1\_MEASURED@0A} = (X_1, Y_3)$$
$$B_{2\_MEASURED@750mA} = (X_2, Y_4)$$

In order to calculate the gain correction factor α and the offset correction β, the ideal output voltage is found for each input current using the ideal transfer function from Equation (1). This theoretical calculation results in two additional points (A_1 and A_2) that fit along the line of the ideal transfer function as shown in Figure 15.

$$A_{1\_IDEAL@0A} = (X_1, Y_1)$$
$$A_{2\_IDEAL@750mA} = (X_2, Y_2)$$

The gain correction factor α and offset correction factor β are then found using Equation 7.

$$\alpha = \frac{\left(\frac{Y_2 - Y_1}{X_2 - X_1}\right)}{\left(\frac{Y_4 - Y_3}{X_2 - X_1}\right)} = \frac{Y_2 - Y_1}{Y_4 - Y_3} \qquad \beta = \alpha \times Y_3 - Y_1 \tag{7}$$

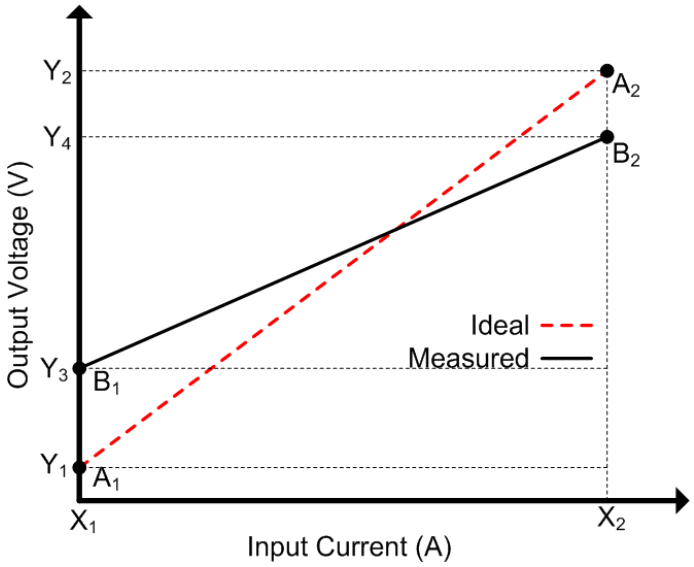

Figure 15. Calculated Points (A_1 and A_2) and Measured Points (B_1 and B_2)

To calibrate the load current, Equation 8 is applied in post-processing to the circuit's output voltage.

$$I_{LOAD\_CALIBRATED} = \frac{\left(V_{OUT\_UNCALIBRATED} - \beta\right) \times \alpha}{R_{SHUNT} \times \left(1 + \frac{R_F}{R_G}\right)} \tag{8}$$

A.4 Electrical Schematic

The Altium electrical schematic for this design can be seen in Figure 16.

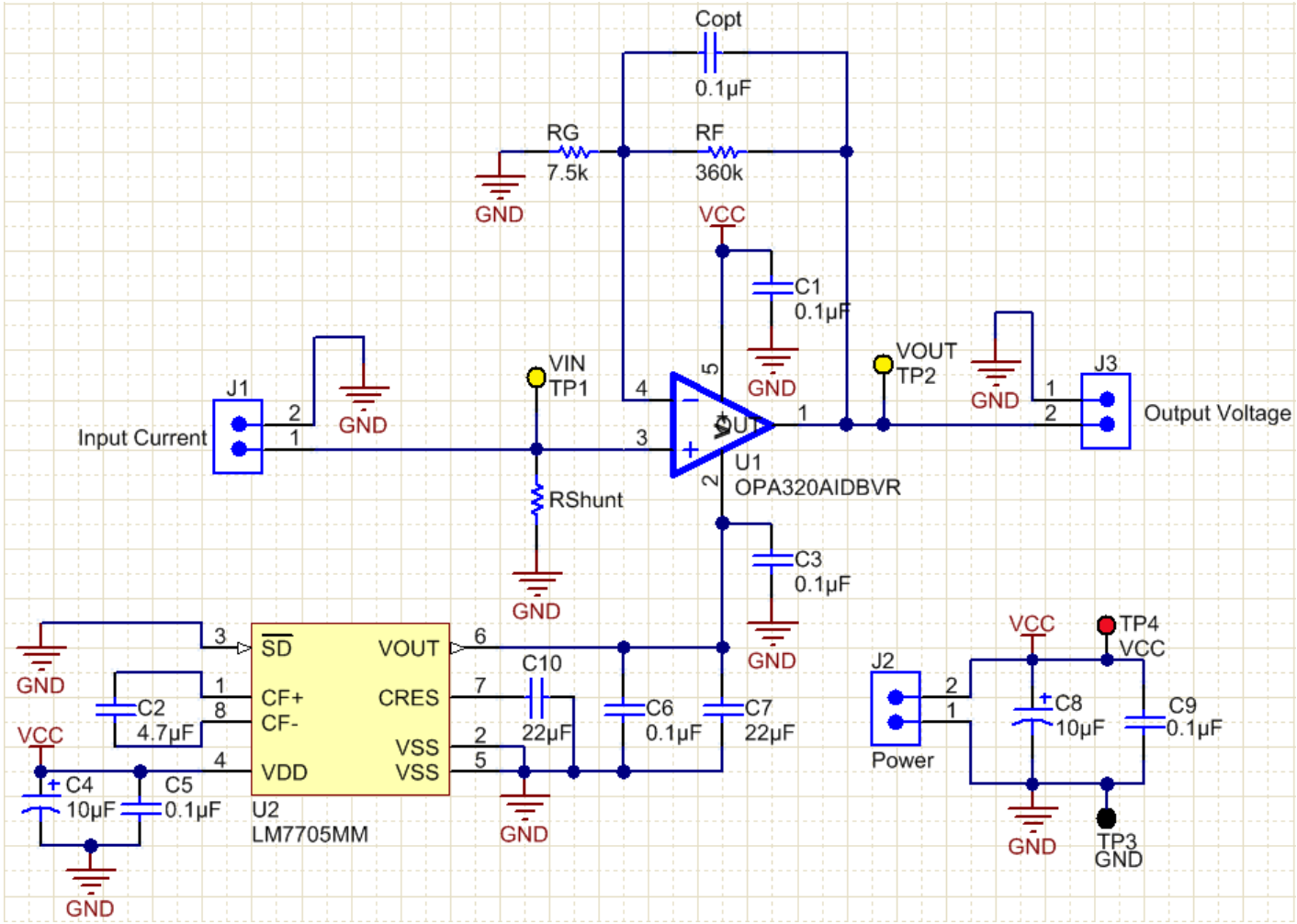

Figure 16. Altium Schematic

A.5 Bill of Materials

The bill of materials for this design is listed in Table 8.

Table 8. Bill of Materials

Item #	Qty	Value	Designator	Description	Manufacturer	Part Number	Supplier Part Number
1	6	0.1uF	C1, C3, C5, C6, C9, Copt	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A	478-3726-1-ND
2	1	4.7uF	C2	CAP CER 4.7UF 16V 20% X5R 0603	TDK Corporation	C1608X5R1C475M080AC	445-7479-1-ND
3	2	10uF	C4, C8	CAP, TANT, 10uF, 20V, +/-20%, 1 ohm, 3528-21 SMD	AVX	TPSB106M020R1000	478-4087-1-ND
4	2	22uF	C7, C10	CAP, CERM, 22uF, 10V, +/-20%, X5R, 0603	Samsung	CL10A226MP8NUNE	1276-1274-1-ND
5	1	360k	RF	RES 360K OHM 1/8W .05% 0805 SMD	Susumu	RG2012N-364-W-T1	RG20N360KWCT-ND
6	1	7.5k	RG	RES 7.5K OHM 1/10W .05% 0603 SMD	Susumu	RG1608N-752-W-T1	RG16N7.5KWCT-ND
7	1	0.1	Rshunt	RES 0.1 OHM 1W .1% 2512	Vishay Foil Resistors	Y14870R10000B9W	Y1487-.1-ND
8	2		TP1, TP2	Test Point, TH, Compact, Yellow	Keystone	5009	5009K-ND
9	1		TP4	Test Point, TH, Compact, Red	Keystone	5005	5005K-ND
10	1		TP3	Test Point, TH, Compact, Black	Keystone	5006	5006K-ND
11	3		J1, J2, J3	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS	ED1514-ND
15	1		U1	OPA320_SOT23-5 DBV	Texas Instruments	OPA320	OPA320AIDBVR DBV
16	1		U2	LM7705 Low Noise Negative Bias Generator	Texas Instruments	LM7705	LM7705MME/NOPB DGK
Hardware							
17	4		S1, S2, S3, S4	STANDOFF HEX 4-40THR ALUM 1L"	Keystone	2205	2205K-ND
18	4		S5, S6, S7, S8	MACHINE SCREW PAN PHILLIPS 4-40	B&F Fastener Supply	PMSSS 440 0025 PH	H703-ND

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