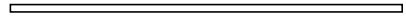
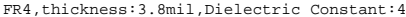



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- 03.Block Diagram
- 04.Power Tree
- 05.System Power
- 06.RK3288 USB/HSIC Controler
- 07.USB HOST Port
- 08.RK3288 RAM Controler
- 09.RAM-DDR3-4X16bit
- 10.Nand FLASH/eMMC/TF Card
- 11.RK3288 GPIO/POWER
- 12.HDMI OUT
- 13.RK3288 LCDC/I2S Controler
- 14.RK1000-S-AV OUT
- 15.S/PDIF OUT
- 16.RK3288 Ethernet MAC Controler
- 17.10/100/1000M-PHY
- 18.RK3288 SDIO0 Controler
- 19.AP6XXX-WIFI/BT
- 20.USB WIFI-(option)
- 21.MIPI Interface
- 22.DTV-(Reserve)
- 23.HDMI IN
- 24.VGA OUT


6 LAYERS PCB STACK

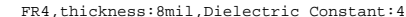
TOP(Signall)  Cu,thickness:0.7mil,Plating to 1oz


GND1  FR4,thickness:3.8mil,Dielectric Constant:4.3

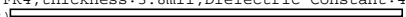
POWER  FR4,thickness:8mil,Dielectric Constant:4.3


FR4,thickness:adjust thickness according to the thickness of board ,Dielectric Constant:4.3


Signal2  Cu,thickness:1.5mil, 1oz


GND2  FR4,thickness:8mil,Dielectric Constant:4.3

BOTTOM(Signal3)  FR4,thickness:3.8mil,Dielectric Constant:4.3

 Cu,thickness:1.5mil, 1oz

 Cu,thickness:1.5mil, 1oz

 Cu,thickness:1.5mil, 1oz

 Cu,thickness:0.7mil,Plating to 1oz

Rackchip
瑞芯微电子 福州瑞芯微电子有限公司

Title: Index

File: RK3288_BOX_Ref

REV:3.0

Create Date: Sunday, January 26, 2014

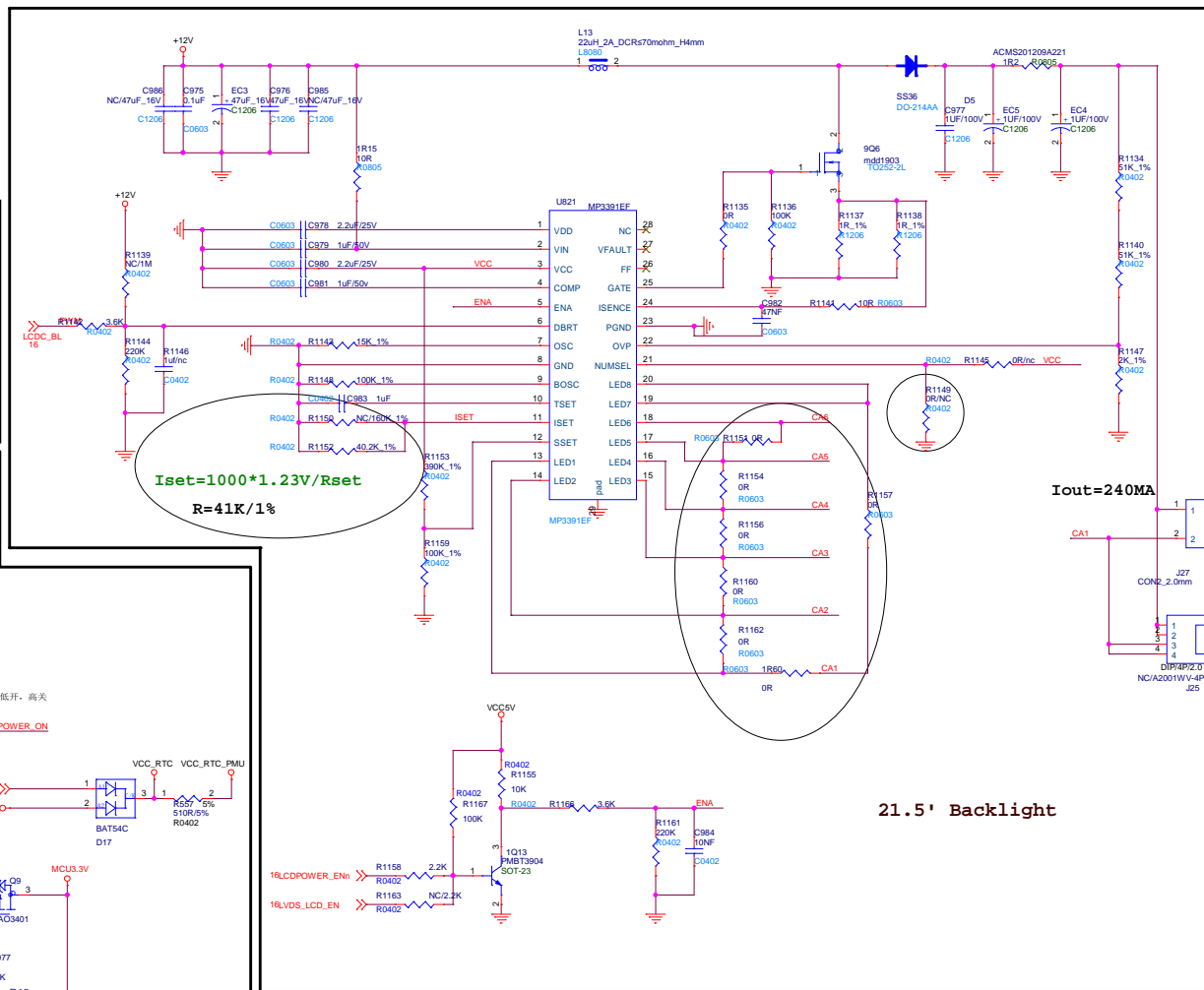
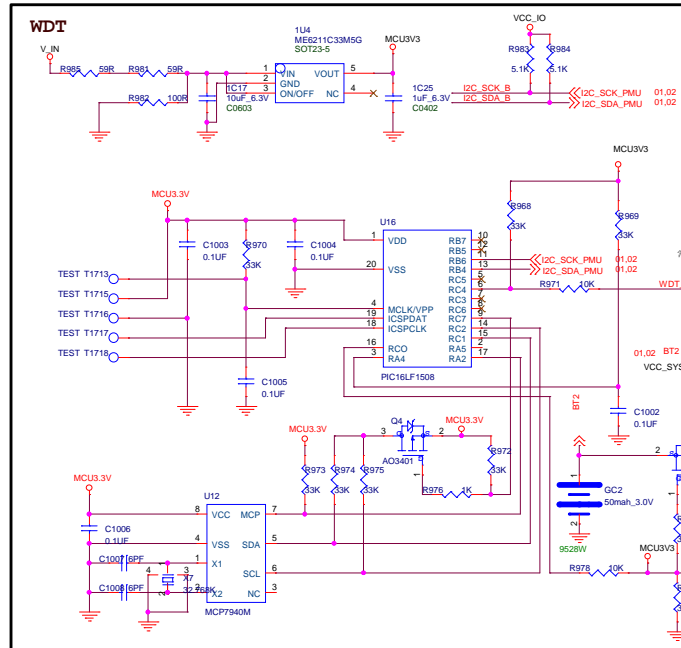
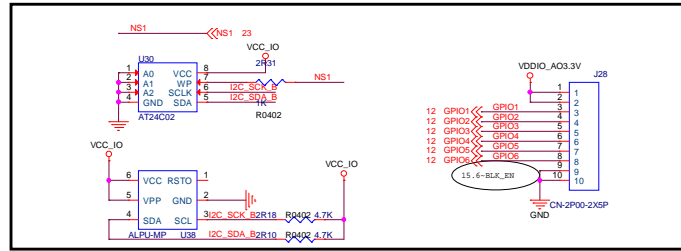
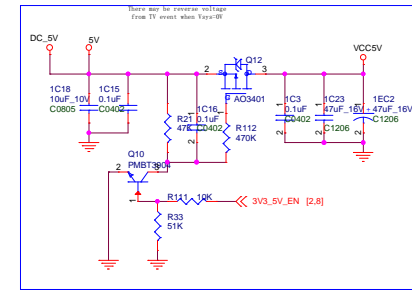
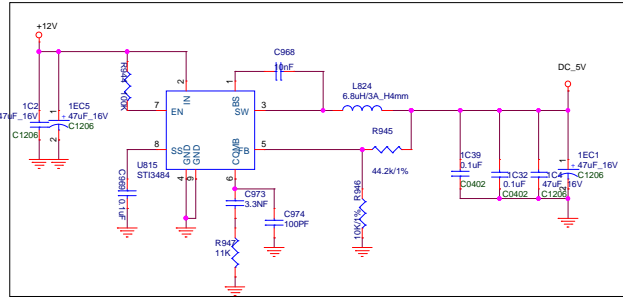
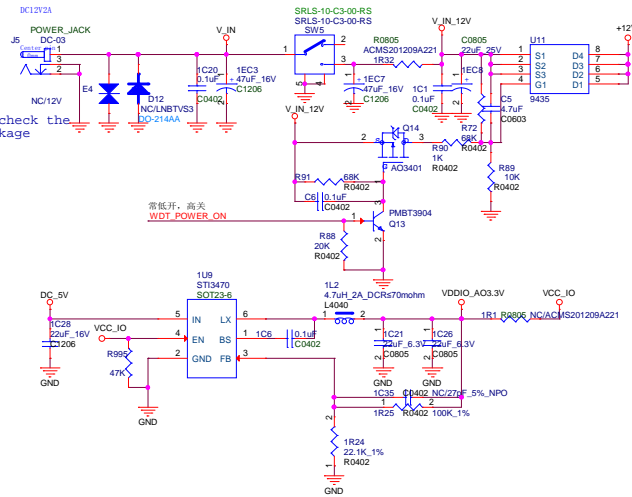
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Modify Date: Monday, July 03, 2017

Page Total: 24

DC power supply input

Please check the PCB package



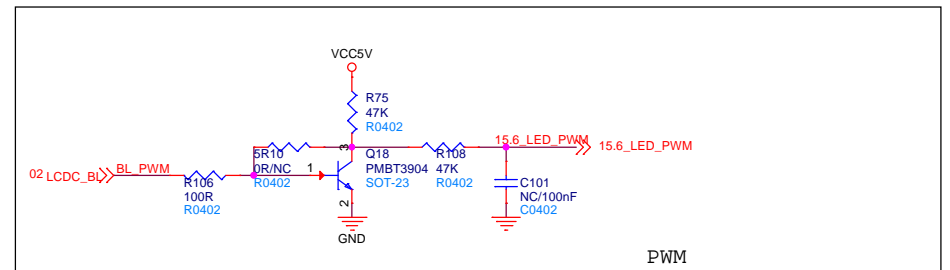
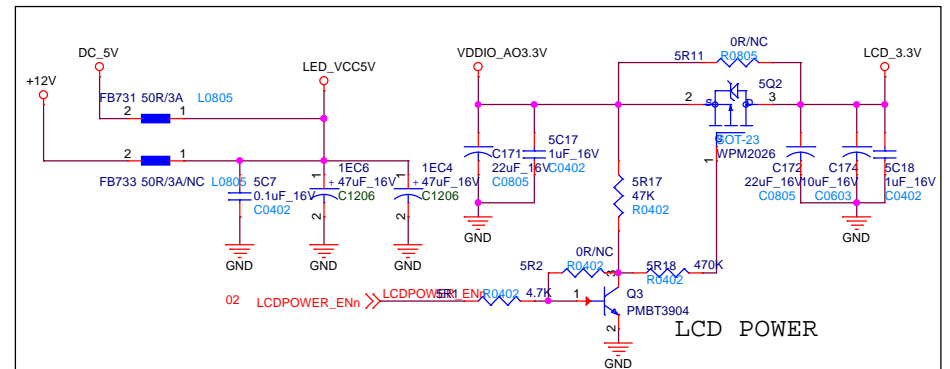
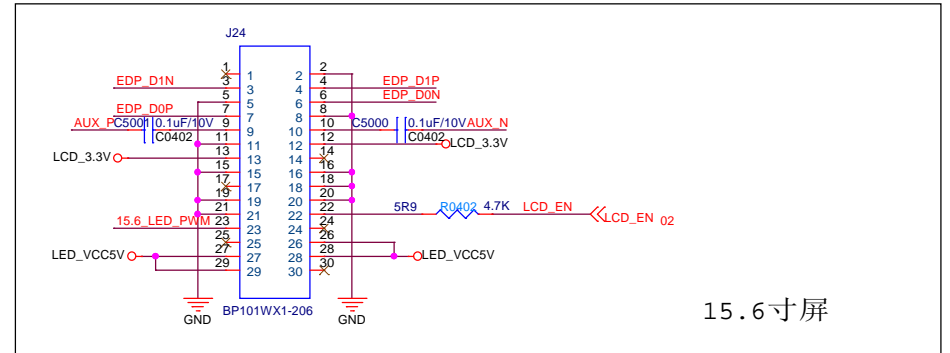
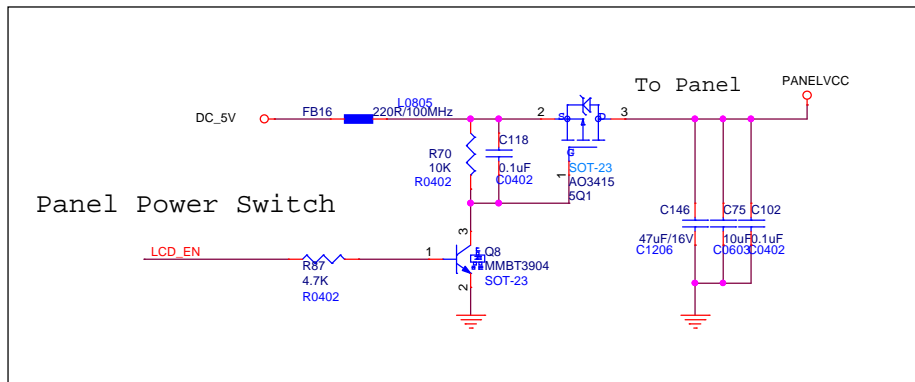
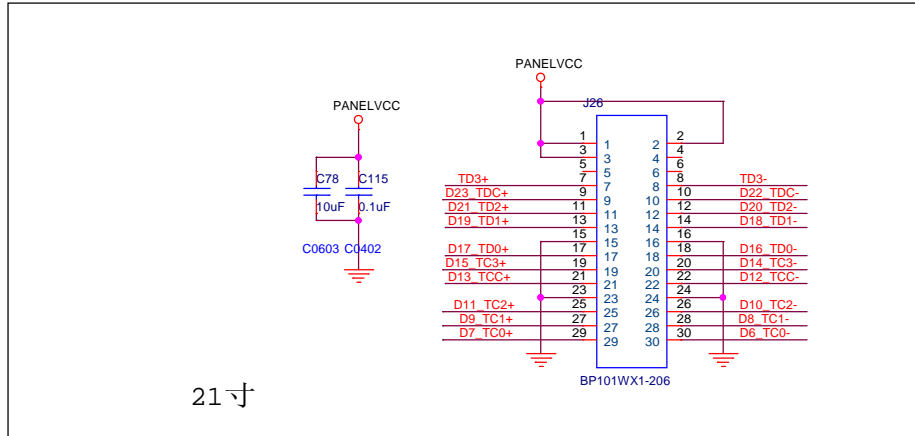
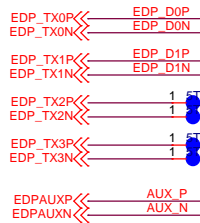
$$I_{set} = 1000 \times 1.23V / R_{set}$$

$$R = 41K / 1\%$$

I_{out}=240mA

21.5" Backlight

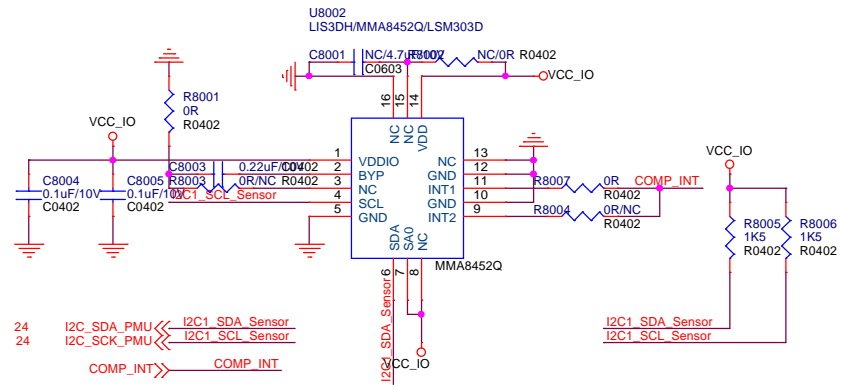
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C	<Doc>		
Date	Thursday, August 24, 2017	Sheet	1 of 1



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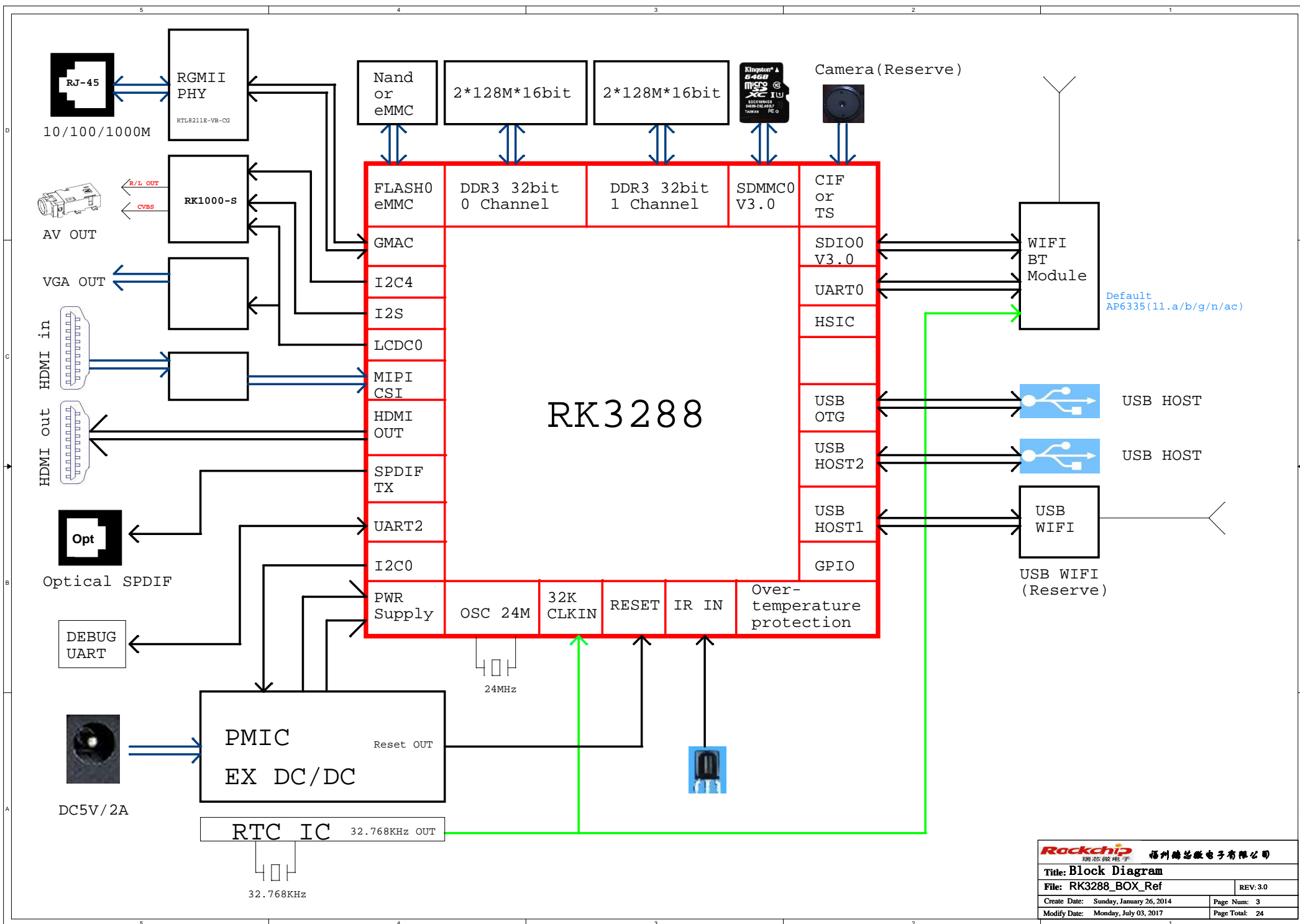
LSM303D with 3D Gsensor and E-compass

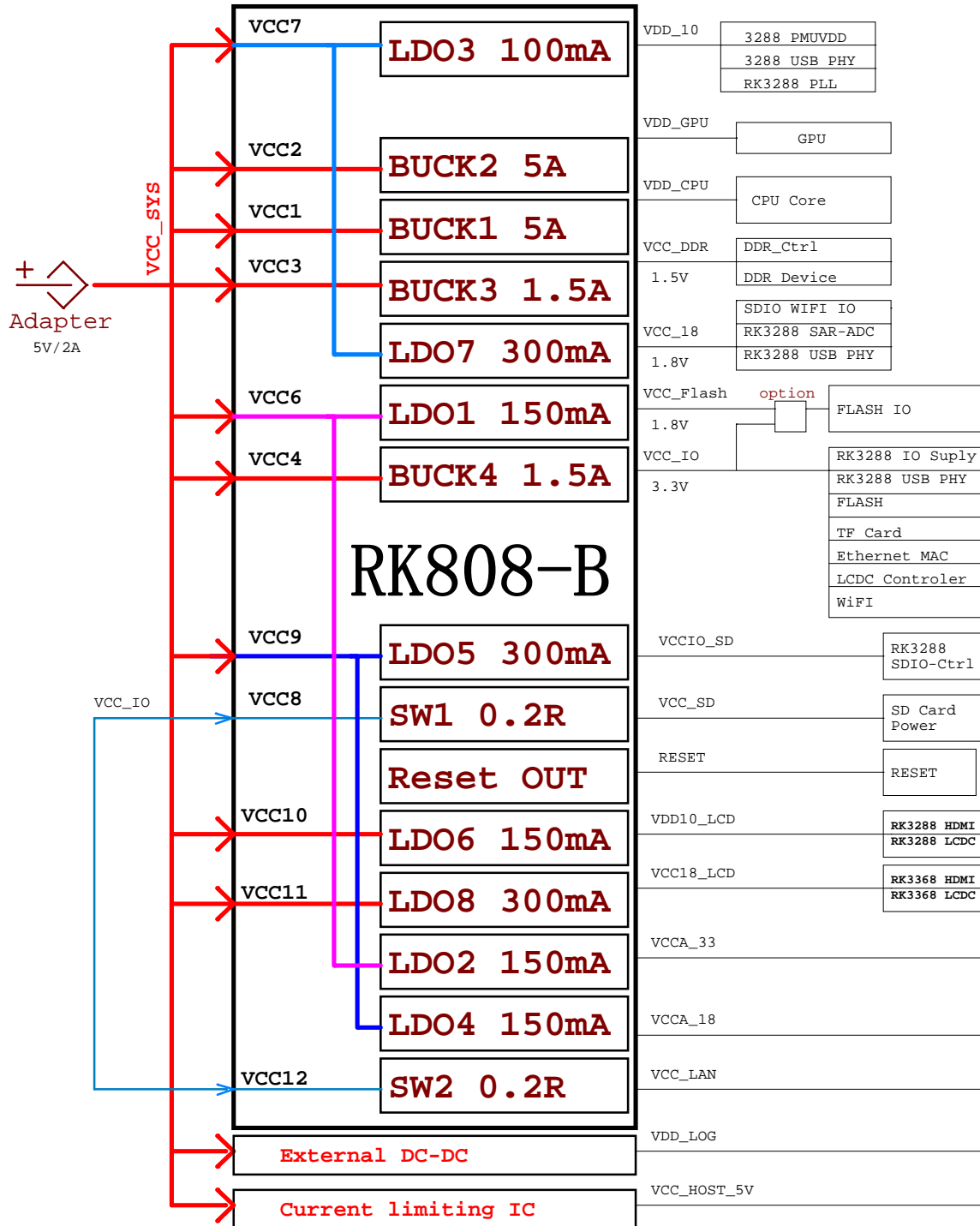
	LIS3DH	MMA8452Q	LSM303D
C8001	NC	NC	4.7uF
R8002	0ohm	NC	NC
R8001	NC	0ohm	NC
C8003	NC	0.1uF	0.22uF
R8003	NC	NC	0R
R8004	NC	NC	0R



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Date:	Thursday, August 03, 2017	Sheet	1 of 1

Version	Date	Author	Change Note	Approved
Beat V0.1	20140217	ZDZ	First edictor	
Beat V0.2	20140227	ZDZ	1:PMIC_SLEEP更改接RK3288-J28管脚 2:ROUT/LOUT耦合电容前后网络名一致, 耦合电容前网络更改为RK1000-ROUT/LOUT 3:各电源的电容优化 4:S/PDIF电源预留可使用VCCA_33, 待机时可以关掉。 5: AV OUT座子的CVBS输出管脚和LOUT对掉 6:SPK_CTL更改接RK3288-G24管脚	
V1.0	20140422	ZDZ	1: 见修改文档.	
V1.1	20140516	ZDZ	1: RK3288 PIN AB23,Y12更改接VCCA_33 2: ACT8846和复位IC之间预留一个0R电阻(R203)。如果使用MCU, 需用外部的复位IC。R203不贴。 3: 以太网的TX信号增加上拉电阻, 增强驱动能力。 4: ACT8846 DC4要用上, 否则上电不了。 5: ACT8846 INL3输入电源默认用VCC_20供电。 6: 解决HDMI CEC漏电问题 7: R85更改成510R 8: 增加VDD_CPU,VDD_GPU电容,降低纹波 9: R146更改22R, 原来是NC不贴。 10: 增加Audio Line Driver 11: 修改eMMC电源, 默认支持1.8V的高速eMMC。 12: ACT8846型号修正, 配RK3288的型号为ACT8846QM490-T 13: RTC IC电源增加预留VCC_SYS供电 14: HDMI ESD器件型号修改 15: 更新原理图框图, POWER TREE, 原来有误。 16: L26,L27更改成SWPA5020SR24NT/5A	
V1.2	20140805	ZDZ	1: 修改记录请见RK3288_BOX_REF_V1.2_20140806原理图修改点	
V1.3	20140926	ZDZ	1: 修改记录请见RK3288_BOX_REF_V1.3_20140928原理图修改点	
V1.4			1: 在V1.3上增加HDMI IN功能, 没有对应的PCB。	
V1.5	20150628	ZDZ	1: 在V1.3基础上, HDMI座子由贴片修改成插件。	
V2.0	20150915	ZDZ	1: 增加HDMI IN和VGA OUT功能 2: 删掉MIC, 摄像头接口 3: 删掉单片机预留	
V3.0	20151224	LCH	1: 将PMIC由ACT8846-490修改为RK808-B	



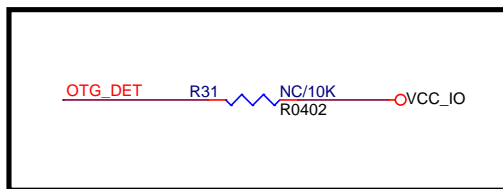
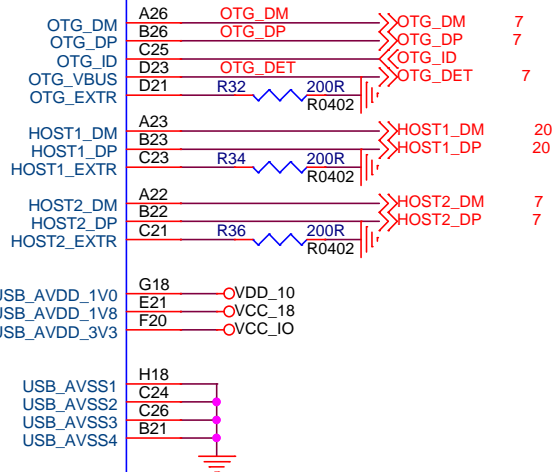


Power up Timing

PowerName	RK808-B Channel	timer 2mS	Default voltage	Normal voltage
VDD_10	LDO3	Slot:1	1.0V	1.0V
VDD_CPU	BUCK1	Slot:2	1.1V	DVFS
VDD_GPU	BUCK2	Slot:3	1.1V	DVFS
VDD_LOG	External DC-DC	Slot:4A	1.0V	DVFS
VCC_DDR	BUCK3	Slot:3	1.5V	1.5V
VCC_18	LDO7	Slot:3	1.8V	1.8V
VCC18_FLASH	LDO1	Slot:4	1.8V	1.8V
VCC_IO	BUCK4	Slot:4	3.3V	3.3V
VCCIO_SD	LDO5	Slot:5	3.3V	1.8V or 3.3V
VCC_SD	SW1	Slot:5	3.3V	3.3V
Reset		16*2mS+50mS		
VDD10_LCD	LDO6	OFF	0V	1.0V
VCC18_LCD	LDO8	OFF	0V	1.8V
VCCA_33	LDO2	OFF	0V	3.3V
VCCA_18	LDO4	OFF	0V	1.8V
VCC_LAN	SW2	OFF	0V	3.3V

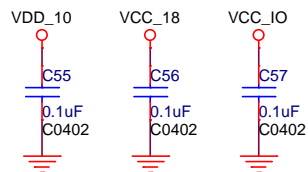
SPDIF
RK3288 I2S
RK1000-S
Audio Line Driver IC
RK3288 LCDC
RK1000-S
Ethernet PHY
Logic
USB HOST
USB HOST

U1E
MCU_RK3288

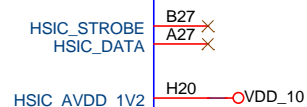


HOST1仅支持USB2.0外设，应用时需注意！

RK3288_E

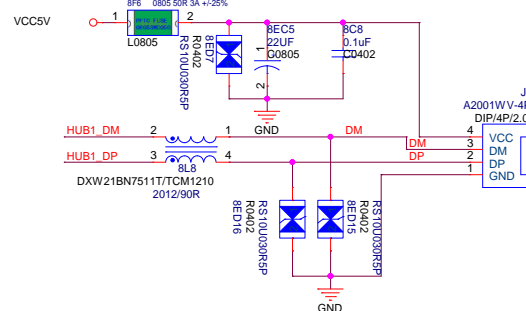
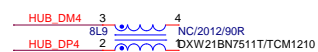
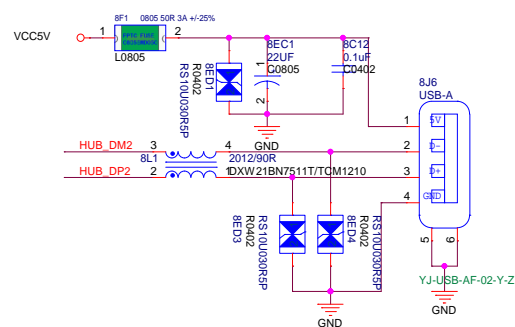
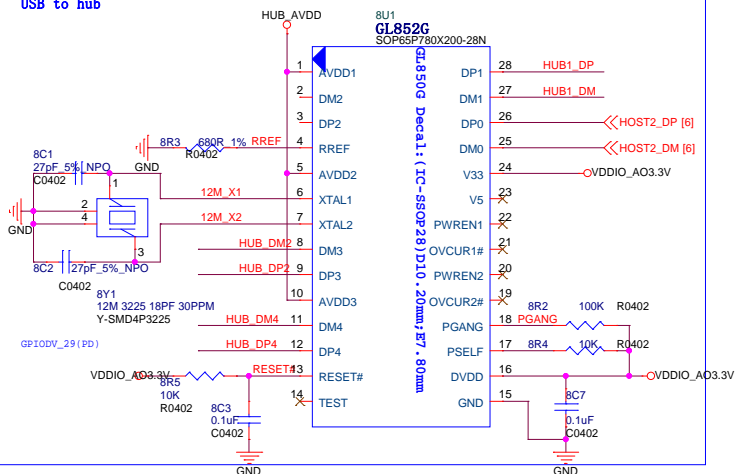
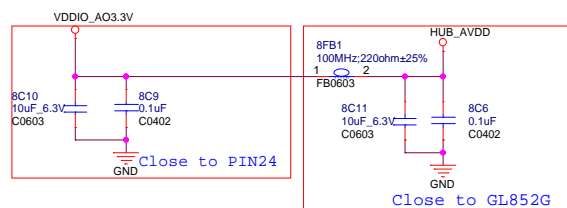
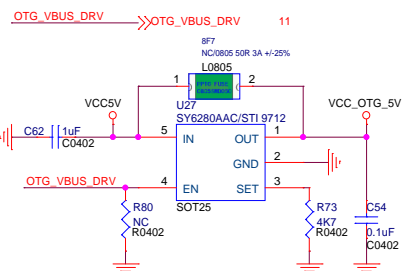


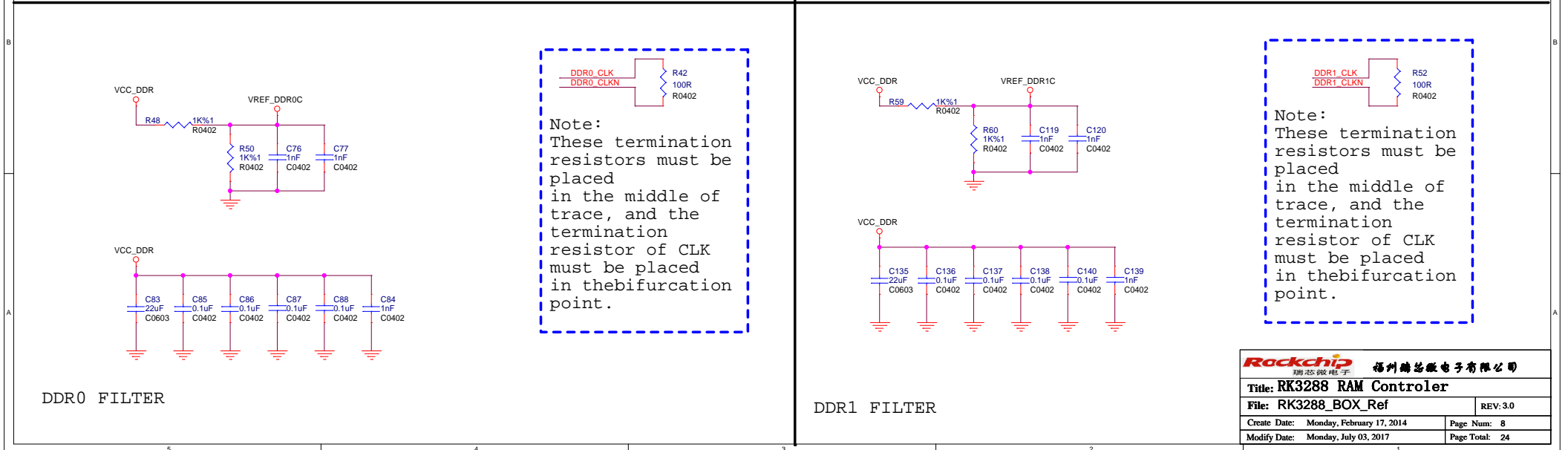
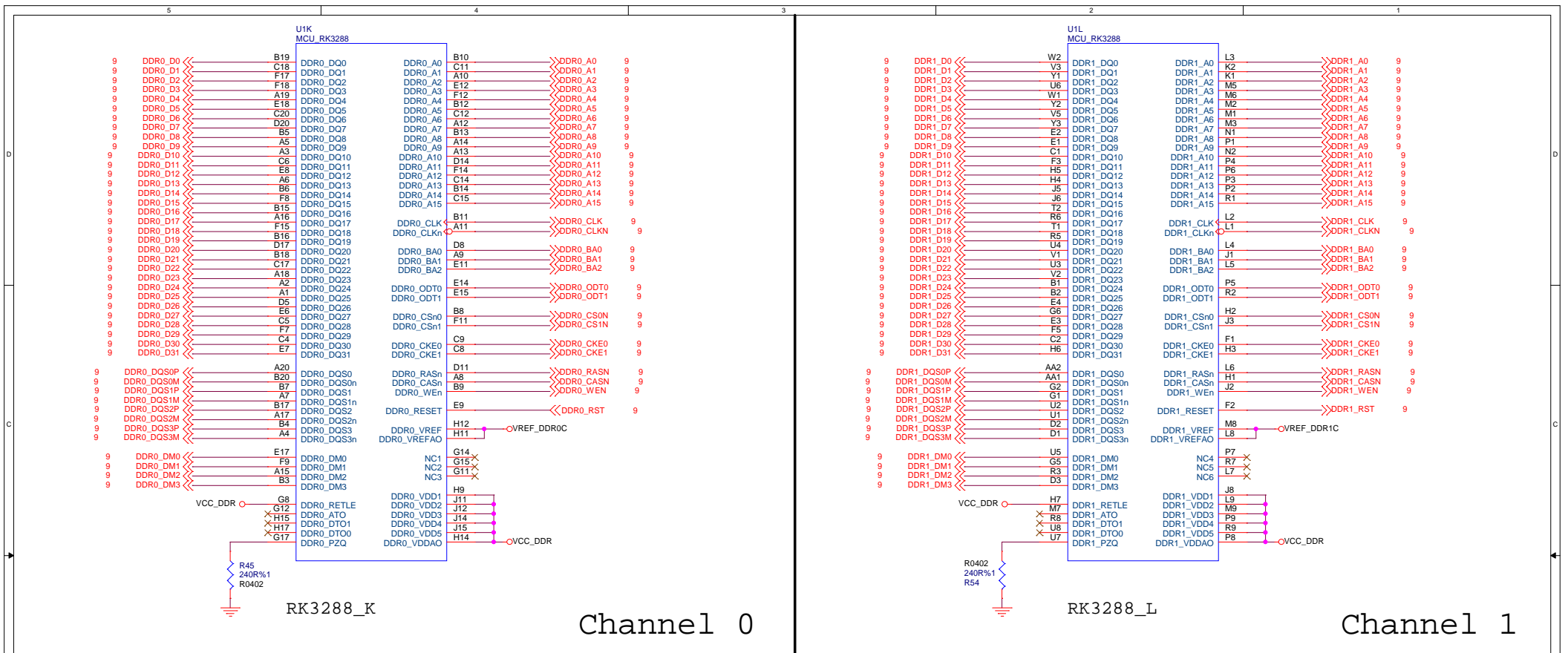
U1U
MCU_RK3288



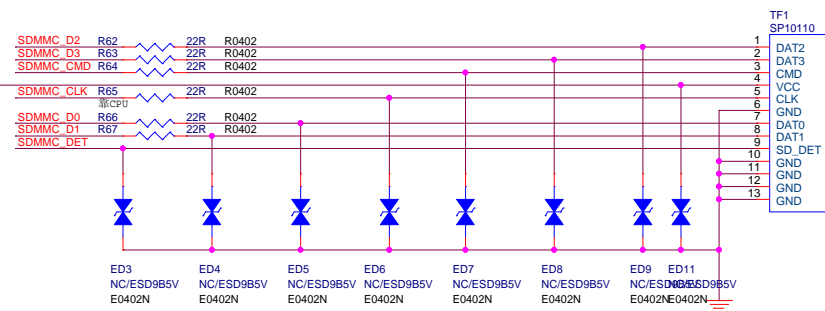
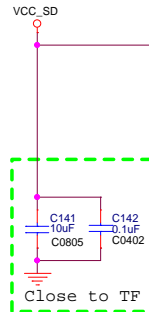
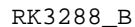
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Modify Date: Monday, July 03, 2017		Page Total: 24	

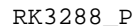






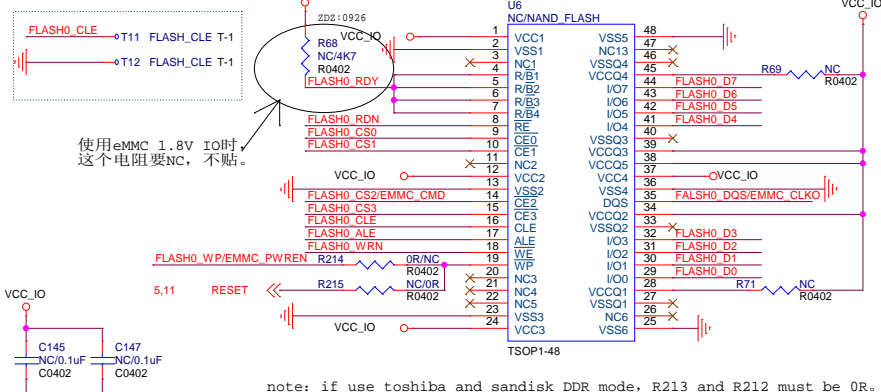


TF Card

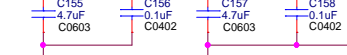
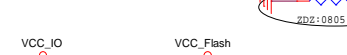
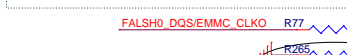
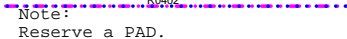


NAND FLASH(Option1)

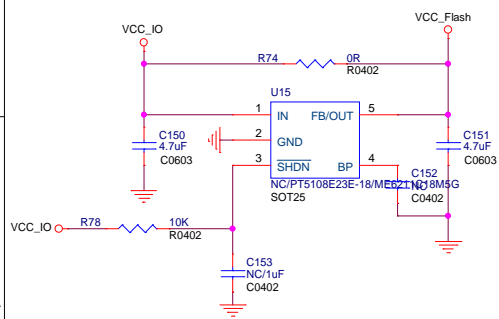
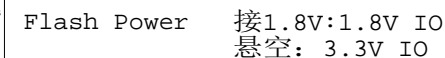
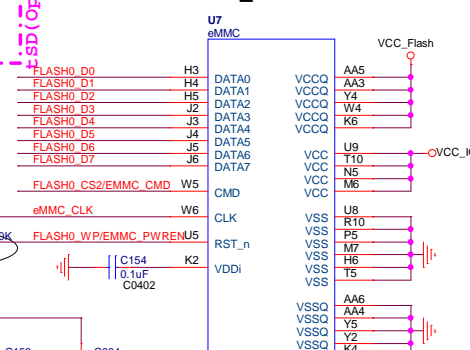
Note:
Reserve a PAD.



note: if use toshiba and sandisk DDR mode, R213 and R212 must be 0R.



Pull-up select



	Flash IO voltage		
eMMC (Default)	1.8V (VCCQ<150mA)	R74: DNP U15: DNP R532: 0R	Default
	1.8V (VCCQ>150mA)	R74: DNP U15: PT5108E23E-18 (500mA) R532: DNP	请确认所使用的 eMMC颗粒的 VCCQ峰值电流。
	3.3V	R74: 0R U15: DNP R532: DNP	
Nand Flash	1.8V (VCCQ<150mA)	R74: DNP U15: DNP R532: 0R	
	1.8V (VCCQ>150mA)	R74: DNP U15: PT5108E23E-18 (500mA) R532: DNP	请确认所使用的 Nand颗粒的 VCCQ峰值电流。
	3.3V	R74: 0R U15: DNP R532: DNP	

U10
MCU_RK3288

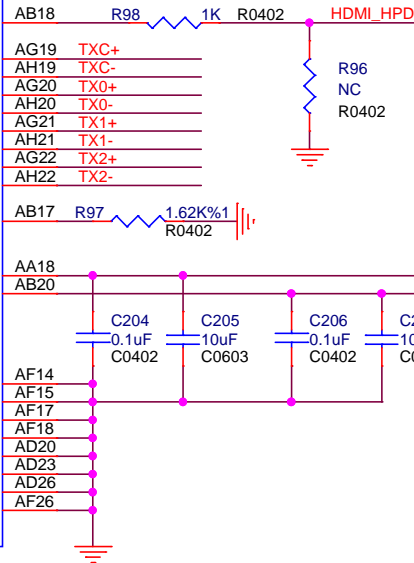
HDMI_HPD_d

HDMI_TXCP
HDMI_TXCN
HDMI_TX0P
HDMI_TX0N
HDMI_TX1P
HDMI_TX1N
HDMI_TX2P
HDMI_TX2N

HDMI_EXTR

HDMI_AVDD_1V0
HDMI_AVDD_1V8

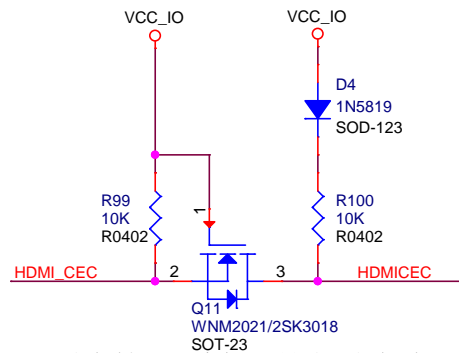
AVSS1
AVSS2
AVSS3
AVSS4
AVSS5
AVSS6
AVSS7
AVSS8



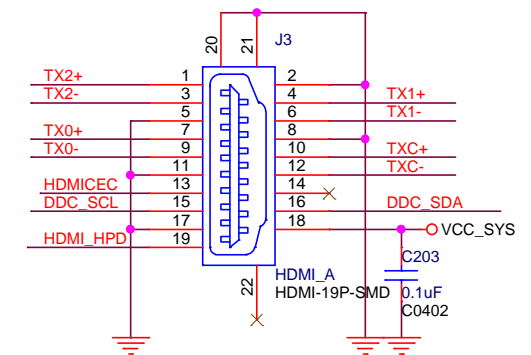
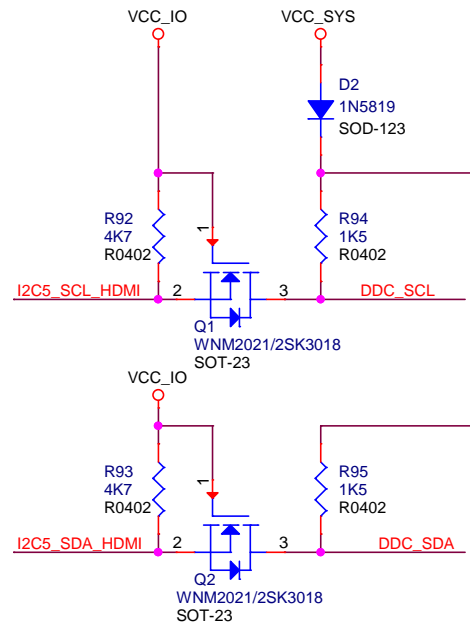
RK3288_O

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I2C5_SCL_HDMI >> I2C5_SCL_HDMI 11

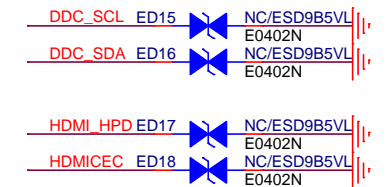
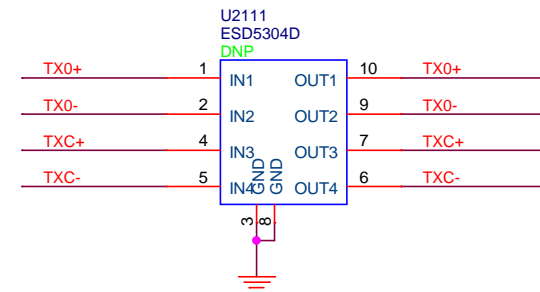
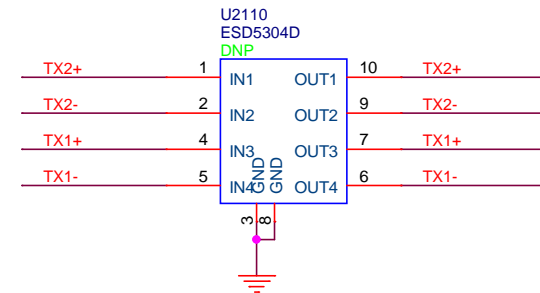
HDMI_CEC >> HDMI_CEC 11



注：需支持CEC功能，这部份电路要贴上。



HDMI OUT



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Create Date: Sunday, January 26, 2014		Page Num: 12	
Modify Date: Thursday, August 03, 2017		Page Total: 24	

U1A
MCU_RK3288

LCDC domain

LCDC0_HSYNC/GPIO1_D0_d
LCDC0_VSYNC/GPIO1_D1_d
LCDC0_DEN/GPIO1_D2_d
LCDC0_DCLK/GPIO1_D3_d

AA23
AB24
AA22
AA24

TRACE_D0/LCDC0_D0/LVDS_D0P
TRACE_D1/LCDC0_D1/LVDS_D0N
TRACE_D2/LCDC0_D2/LVDS_D1P
TRACE_D3/LCDC0_D3/LVDS_D1N
TRACE_D4/LCDC0_D4/LVDS_D2P
TRACE_D5/LCDC0_D5/LVDS_D2N
TRACE_D6/LCDC0_D6/LVDS_D3P
TRACE_D7/LCDC0_D7/LVDS_D3N
TRACE_D8/LCDC0_D8/LVDS_D4P
TRACE_D9/LCDC0_D9/LVDS_D4N
TRACE_D10/LCDC0_D10/LVDS_CLK0P
TRACE_D11/LCDC0_D11/LVDS_CLK0N
TRACE_D12/LCDC0_D12/LVDS_D5P
TRACE_D13/LCDC0_D13/LVDS_D5N
TRACE_D14/LCDC0_D14/LVDS_D6P
TRACE_D15/LCDC0_D15/LVDS_D6N
TRACE_CLK/LCDC0_D16/LVDS_D7P
TRACE_CT/LCDC0_D17/LVDS_D7N
LCDC0_D18/LVDS_D8P
LCDC0_D19/LVDS_D8N
LCDC0_D20/LVDS_D9P
LCDC0_D21/LVDS_D9N
LCDC0_D22/LVDS_CLK1P
LCDC0_D23/LVDS_CLK1N

LVDS_EXTR

LVDS domain

LVDS_AVDD_1V0
LVDS_AVDD_1V8
LVDS_AVDD_3V3

T27
T28
U27
U28
W27
W28
Y27
Y28
AA27
AA28
V27
V28
U25
U26
V25
V26
AA25
AA26
AB27
AB28
AC25
AC26
Y25
Y26

LVDS_D0P
LVDS_D0N
LVDS_D1P
LVDS_D1N
LVDS_D2P
LVDS_D2N
LVDS_D3P
LVDS_D3N
LVDS_D4P
LVDS_D4N
LVDS_CLK0P
LVDS_CLK0N
LVDS_D5P
LVDS_D5N
LVDS_D6P
LVDS_D6N
LVDS_D7P
LVDS_D7N
LVDS_D8P
LVDS_D8N
LVDS_D9P
LVDS_D9N
LVDS_CLK1P
LVDS_CLK1N

Dual
LVDS
odd

Dual
LVDS
even

LVDS_D0P
LVDS_D0N
LVDS_D1P
LVDS_D1N
LVDS_D2P
LVDS_D2N
LVDS_D3P
LVDS_D3N
LVDS_CLK0P
LVDS_CLK0N
LVDS_D5P
LVDS_D5N
LVDS_D6P
LVDS_D6N
LVDS_D7P
LVDS_D7N
LVDS_D8P
LVDS_D8N
LVDS_CLK1P
LVDS_CLK1N

V24 R1702 2K%1 R0402

AA20 VDD10_LCD
AB21 VCC18_LCD
AB23

R103 0R R0402 VCCA_33
C327 0.1uF C0402

RK3288_A

U1I
MCU_RK3288

I2S_SCLK/GPIO6_A0_d
I2S_LRCK_RX/GPIO6_A1_d
I2S_LRCK_TX/GPIO6_A2_d
I2S_SDI/GPIO6_A3_d
I2S_SDO0/GPIO6_A4_d
I2S_SDO1/GPIO6_A5_d
I2S_SDO2/GPIO6_A6_d
I2S_SDO3/GPIO6_A7_d
I2S_CLK/GPIO6_B0_d
I2C2_SDA/GPIO6_B1_u
I2C2_SCL/GPIO6_B2_u

SPDIF_TX/GPIO6_B3_d

APIO4_VDD

AD11
AG11
AF11
AE11
AG12
AH13
AG13
AH12
AC12
AF12
AD12

I2S0_SCLK
I2S0_LRCK_RX
I2S0_LRCK_TX
I2S0_SDI
I2S0_SDO0
I2S0_CLK
I2C2_SDA_AUDIO
I2C2_SCL_AUDIO

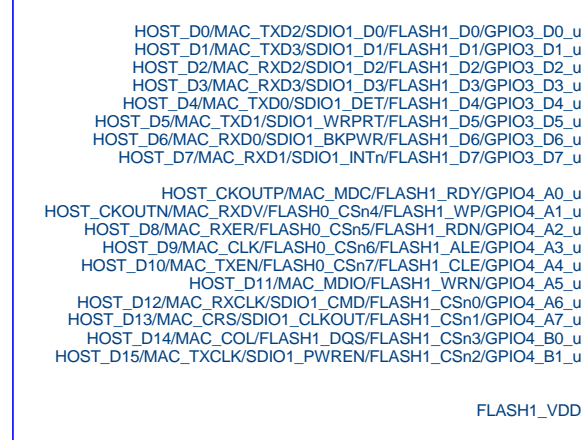
AE12
Y12

C239 0.1uF C0402

RK3288_I

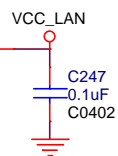
 瑞芯微电子		福州瑞芯微电子有限公司	
Title: RK3288 LCDC/I2S Controller			
File: RK3288_BOX_Ref			REV:3.0
Create Date: Monday, February 17, 2014		Page Num: 13	
Modify Date: Monday, July 03, 2017		Page Total: 24	

U1Q
MCU_RK3288



RK3288_Q

Y4
V6
AB1
AC1
AD1
AB2
AA3
AA4
AC3
AC2
AE1
AE2
AD2
Y5
AB5
AA6
AA5
V7
V8

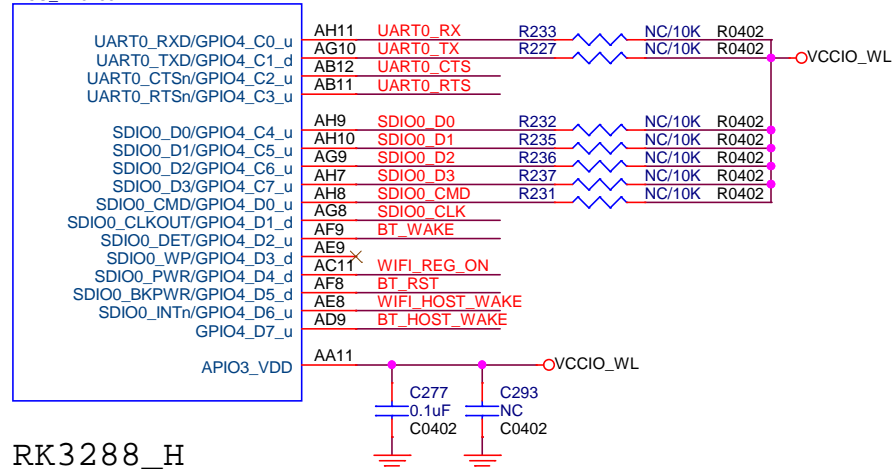


MAC_MDIO R137 1K5 R0402 VCC_LAN

17 PHY_TXEN << >> RMII_TX_EN
17 PHY_TXD1 << >> RMII_TXD1
17 PHY_TXD0 << >> RMII_TXD0
17 MAC_RXD0 << >> RMII_RX_D0
17 MAC_RXD1 << >> RMII_RX_D1
17 MAC_MDC << >> MAC_MDC
17 MAC_CRXER << >> RXER/FXEN
17 MAC_MDIO << >> RMII_MD
17 MAC_MDC << >> RMII_MDCLK
17 PHY_RST << >> RMII_RST
17 MAC_CRSD << >> RMII_CSR_VALID
17 MAC_CLK << >> RMII_CLK

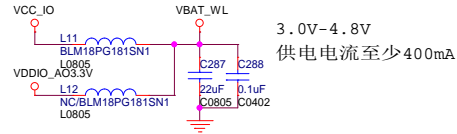
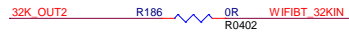
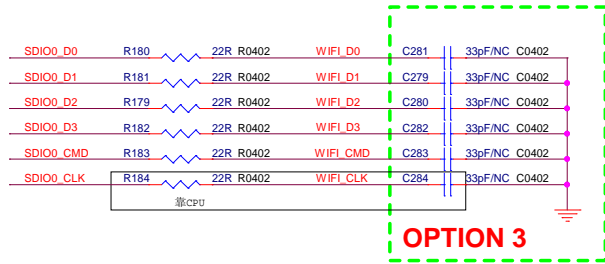
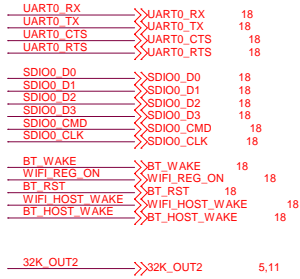
PHY_TXD0 R167 4K7 R0402 VCC_LAN
PHY_TXD1 R185 4K7 R0402

U1H
MCU_RK3288

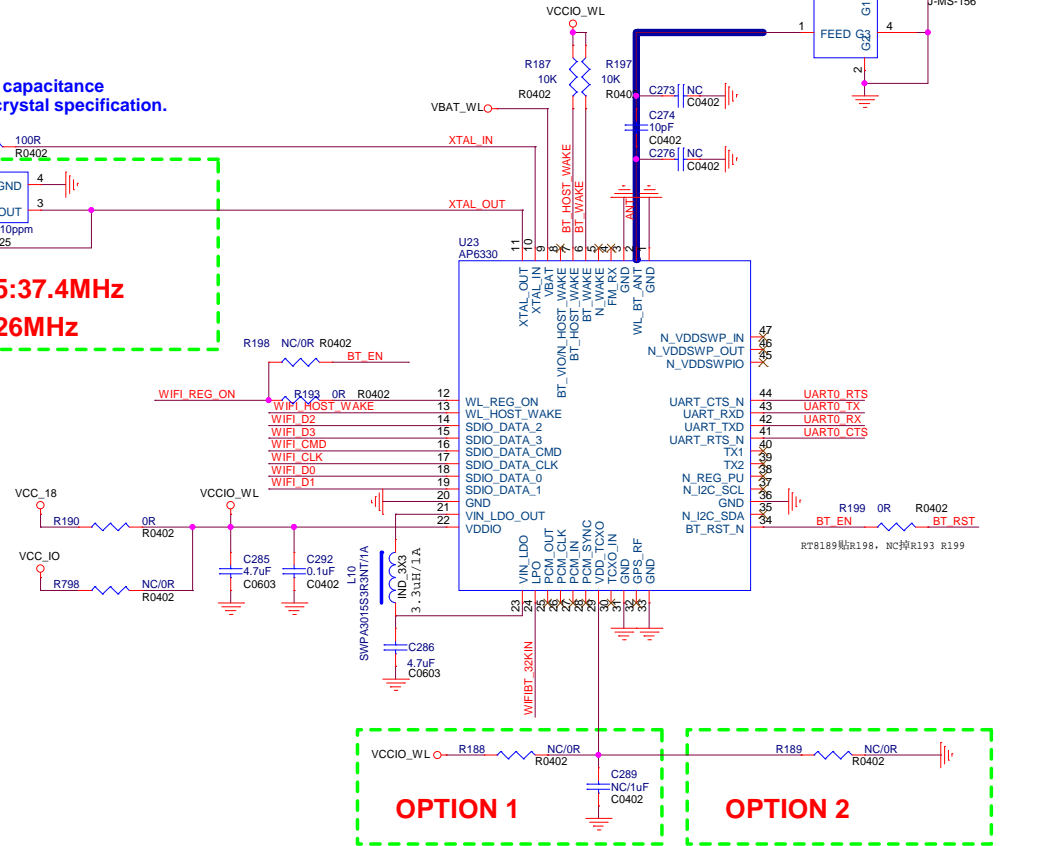
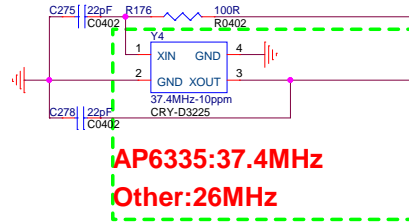


RK3288_H

UART0_RX	>>UART0_RX	19
UART0_TX	>>UART0_TX	19
UART0_CTS	>>UART0_CTS	19
UART0_RTS	>>UART0_RTS	19
SDIO0_D0	>>SDIO0_D0	19
SDIO0_D1	>>SDIO0_D1	19
SDIO0_D2	>>SDIO0_D2	19
SDIO0_D3	>>SDIO0_D3	19
SDIO0_CMD	>>SDIO0_CMD	19
SDIO0_CLK	>>SDIO0_CLK	19
BT_WAKE	>>BT_WAKE	19
WIFI_REG_ON	>>WIFI_REG_ON	19
BT_RST	>>BT_RST	19
WIFI_HOST_WAKE	>>WIFI_HOST_WAKE	19
BT_HOST_WAKE	>>BT_HOST_WAKE	19



Note:
 Adjusted the load capacitance
 according to the crystal specification.

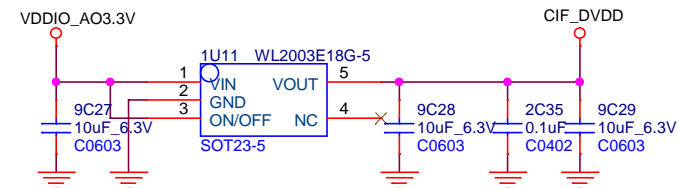
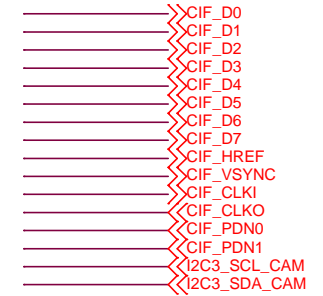


OPTION	WIFI				BT4.0	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6181		Yes				26MHz	1.71-3.6V
AP6212		Yes			Yes	26MHz	1.71-3.6V
XZ3538		Yes			Yes	26MHz	1.71-3.6V
XZ3660	Yes	Yes		Yes	Yes	26MHz	1.2-2.9V
AP6330	Yes	Yes		Yes	Yes	26MHz	1.2-2.9V
AP6335 (Default)	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.63V

OPTION	1	2	3
AP6181	No	No	No
AP6212	No	No	No
XZ3538	No	No	No
XZ3660	No	No	No
AP6330	No	No	No
AP6335 (Default)	No	Yes	Yes

Note:
 Yes:框内要贴
 No:框内不贴

A



[illegible]