The Eight-bit Johnson Counter

Johnson counter also known as the creeping counter is an example of a synchronous counter. In the Johnson counter, the complemented output of the last flip flop is connected to the input of the first flip flop, and to implement the n-bit Johnson counter we require n flip-flops. Generally, it is implemented using D-Flip Flops. It is one of the most important types of shift register counters. It is formed by the feedback of the output to its own input.

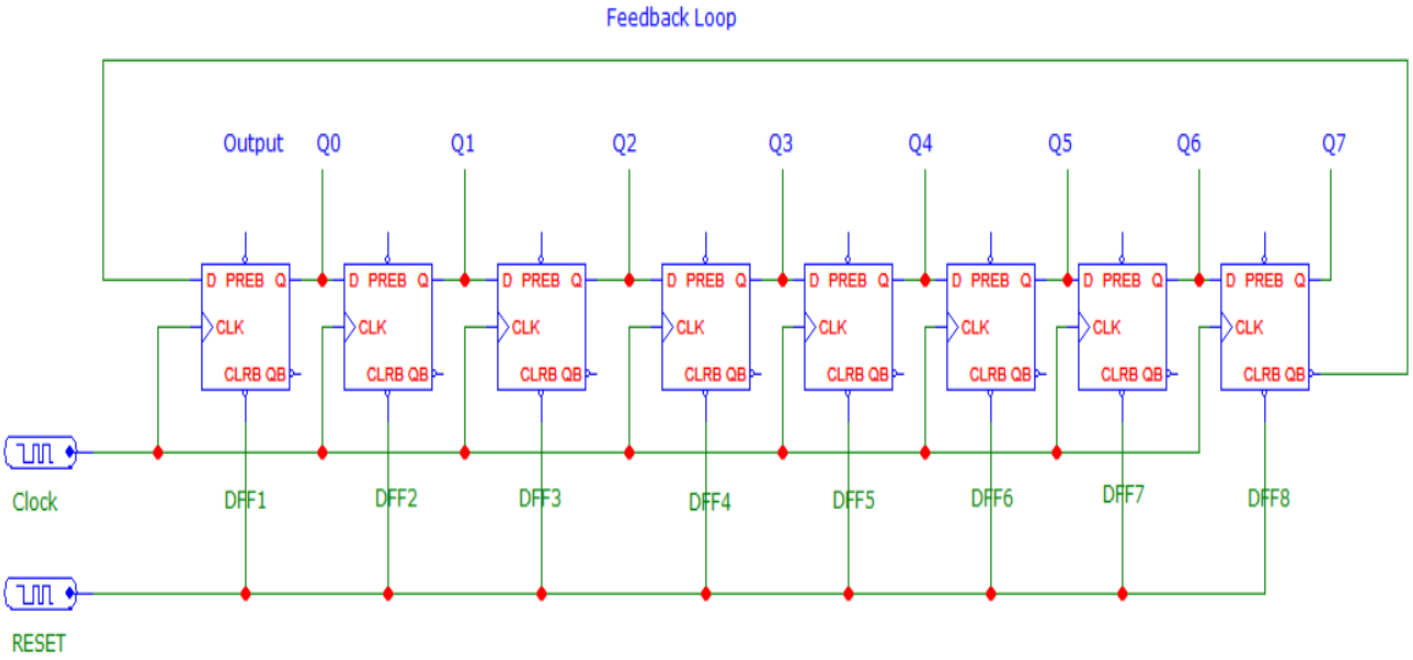
Total number of used and unused states in n-bit Johnson counter:

number of used states=2n

number of unused states=2^n – 2*n

Circuit Diagram:

The johnson counter circuit diagram is the cascaded arrangement of 'n' flip-flops. In such a design, the output of the proceeding flip-flop is fed back as input to the next flip-flop. For example, the inverted output of the last flip-flop '$\bar{Q}$n' is fed back to the first flip-flop in the sequence bit pattern. The counter registers cycles in a closed-loop i.e circulates within the circuit.



Reset pin acts as an on/off switch. So, the flip-flops can be enabled by clicking the Reset switch.

CLK pin is used to observe the changes in the output of the flip-flops.

Truth Table:

Consider the truth table of the 8-bit Johnson counter. The output of the proceeding flip-flop is connected as the input of the next flip-flop. The clock signal(CLK) is used to know the changes in the output. It contains 8 flip-flops, Q0, Q1... Q7 are the outputs of the flip-flops. The counter counts the state of cycles in a continuous closed loop.

State	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	1	1	1	1	0	0	0	0
6	1	1	1	1	1	0	0	0
7	1	1	1	1	1	1	0	0
8	1	1	1	1	1	1	1	0
9	1	1	1	1	1	1	1	1
10	0	1	1	1	1	1	1	1
11	0	0	1	1	1	1	1	1
12	0	0	0	1	1	1	1	1
13	0	0	0	0	1	1	1	1
14	0	0	0	0	0	1	1	1
15	0	0	0	0	0	0	1	1
16	0	0	0	0	0	0	0	1

Working of Eight-Bit Johnson Counter:

The above table state that

- The counter produces the output 00000000 when there is no clock input passed(at time t = 0).
- The counter produces the output 10000000 when the 1st clock pulse(1st posegde of the clock) is passed to the flip flops.
- The counter produces the output 11000000 when the 2nd clock pulse(2nd posedge of clock) is passed to the flip flops.
- The counter produces the output 11100000 when the 3rd clock pulse is passed to the flip flops.
- The counter produces the output 11110000 when the 4th clock pulse is passed to the flip flops.

..... and so on. (can be seen from the truth table).

Timing Diagram: