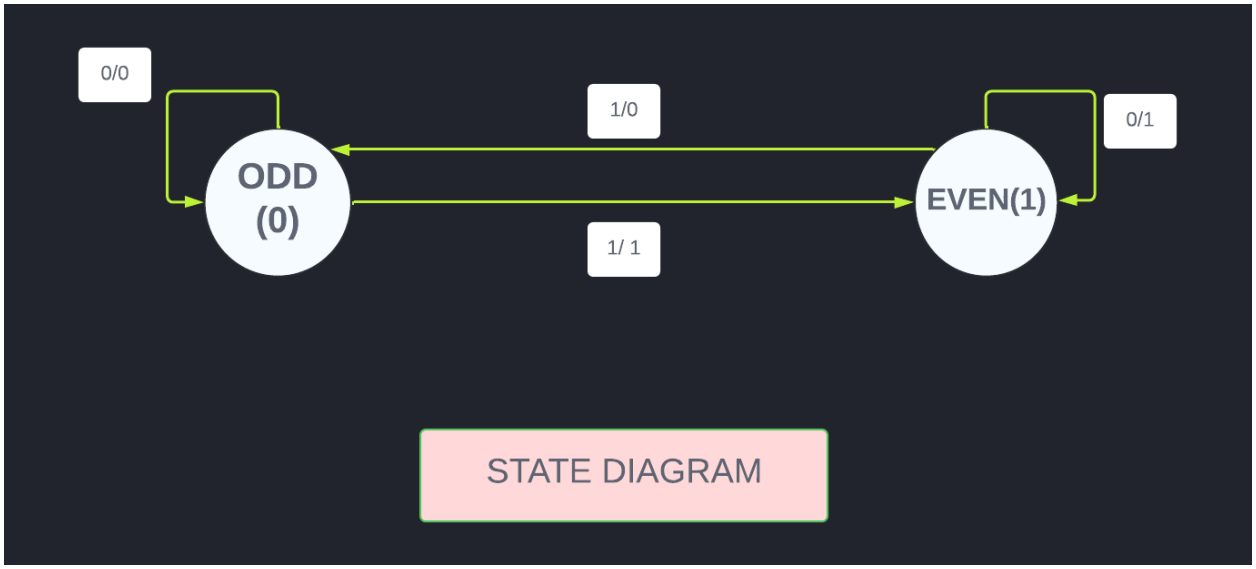
THREE BIT ODD PARITY BIT GENERATOR

STATE DIAGRAM

Our state machine has 2 states :

- EVEN (1)
- ODD (0)



TRUTH TABLE

3-bit message			Odd parity bit generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

EXCITATION TABLE

INPUT BIT (at time t)	PRESENT STATE(PS)	NEXT STATE (NS)	OUTPUT (O/P)
0	0 (ODD)	0 (ODD)	1
0	1 (EVEN)	1 (EVEN)	0
1	0 (ODD)	1 (EVEN)	0
1	1 (EVEN)	0 (ODD)	1

STATE TABLE

PRESENT STATE (P)	(NEXT STATE, OUTPUT)	
	INPUT BIT	
	0	1
0 (ODD)	(0 , 0)	(1 ,1)
1 (EVEN)	(1 , 1)	(0 , 0)

TRANSITION TABLE

PRESENT STATE	NEXT STATE	
	INPUT BIT	
	0	1
0 (ODD)	0	1
1 (EVEN)	1	0

OUTPUT TABLE

PRESENT STATE	OUTPUT	
	INPUT BIT	
	0	1
0 (ODD)	0	1
1 (EVEN)	1	0

K-MAP

- **FOR NEXT STATE (Y(t+1))**

INPUT BIT (X)	PRESENT STATE(Y(t))	
	0	1
0	0	1
1	1	0

$$Y(t+1) = (X \,.\, \overline{Y(t)}) + (\overline{X} \,.\, Y(t))$$

$$Y(t+1) = X \oplus Y(t)$$

- **FOR OUTPUT LOGIC (Z)**

INPUT BIT (X)	PRESENT STATE(Y(t))	
	0	1
0	0	1
1	1	0

$$Z = (X \,.\, \overline{Y(t)}) + (\overline{X} \,.\, Y(t))$$

$$Z = X \oplus Y(t)$$

LOGIC DIAGRAM