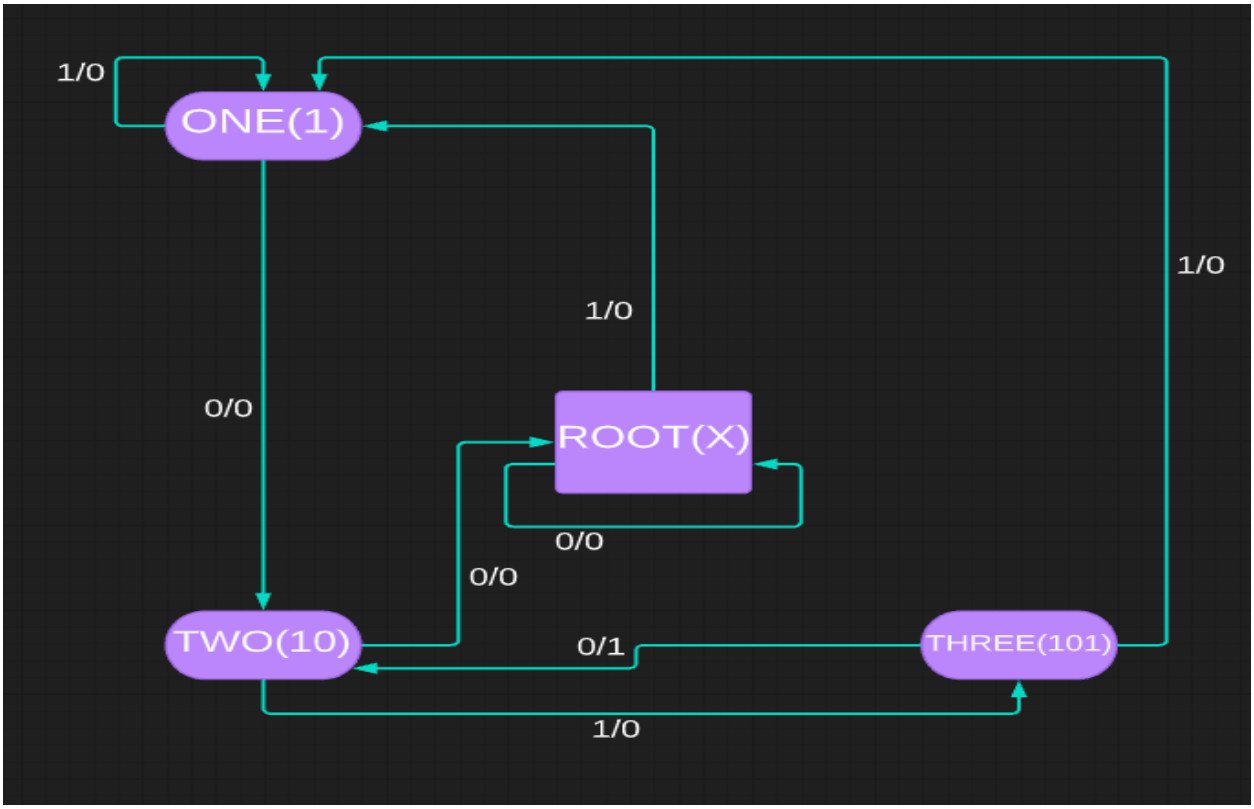
Sequence detector

State diagram:

The FSM for the sequence detector has 4 states.

The States are represented as :

- ROOT = 00
- ONE = 01
- TWO = 10
- THREE = 11



Excitation Table

INPUT BIT (X)	PRESENT STATE(PS)	NEXT STATE(NS)	OUTPUT(Z)
0	00 (ROOT)	00 (ROOT)	0
1	00 (ROOT)	01 (ONE)	0
0	01 (ONE)	10 (TWO)	0
1	01 (ONE)	01 (ONE)	0
0	10 (TWO)	00 (ROOT)	0
1	10 (TWO)	11 (THREE)	0
0	11 (THREE)	10(TWO)	1
1	11 (THREE)	01 (ONE)	0

STATE TABLE :

PRESENT STATE	(NEXT STATE , OUTPUT)	
	INPUT BIT	
	0	1
00(ROOT)	(00,0)	(01 ,0)
01(ONE)	(10,0)	(01,0)
10(TWO)	(00,0)	(11,0)
11(THREE)	(10,1)	(01,0)

Transition table

PRESENT STATE	NEXT STATE	
	INPUT BIT	
	0	1
00(ROOT)	00	01
01(ONE)	10	01
10(TWO)	00	11
11(THREE)	10	01

OUTPUT TABLE

PRESENT STATE	OUTPUT	
	INPUT BIT	
	0	1
00(ROOT)	0	0
01(ONE)	0	0
10(TWO)	0	0
11(THREE)	1	0

K-MAP

FOR NEXT STATE :

PRESENT STATE	NEXT STATE	
	INPUT BIT	
	0	1
00(ROOT)	00	01
01(ONE)	10	01
10(TWO)	00	11
11(THREE)	10	01

- **For bit 1 of next state :**

INPUT BIT(X)	**PRESENT STATE(S1,S2)**			
	00(ROOT)	**01(ONE)**	**11(THREE)**	**10(TWO)**
0	**0**	**0**	**0**	**0**
1	**1**	**1**	**1**	**1**

$$Y1 = X$$

- **For bit 2 of next state :**

INPUT BIT	**PRESENT STATE(S1,S2)**			
	00	**01**	**11**	**10**
0	**0**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**

$$Y2 = (\bar{X}.S2) + (X.S1.\bar{S2})$$

S1 , S2 denotes first and second bit of the states respectively.

FOR OUTPUT LOGIC :

INPUT BIT	PRESENT STATE(S1,S2)			
	00(ROOT)	01(ONE)	11(THREE)	10(TWO)
0	0	0	1	0
1	0	0	0	0

$$Z = (\bar{X}.S1.S2)$$

LOGIC DIAGRAM