# A 5-33 GHz 8-Channel Transmit Beamformer with Peak Power of 14 dBm for X/Ku/Ka-band SATCOM Applications


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***Abstract*— This paper presents a 5-33 GHz 8-channel transmit beamformer implemented in 90nm SiGe BiCMOS HBT technology. Each channel is composed of a wideband two-stage power-amplifier (PA), a phase-shifter (PS), a variable gain amplifier (VGA) and single-ended to differential converter (S2D). The input RF power is distributed to the 8-channels using a two-stage Wilkinson network and active dividers. The measured small-signal gain is 24-27 dB at 5-33 GHz with 5-bit phase-shifter operation and > 20 dB gain control. A peak OP1dB and OPsat of 13-14 dBm is achieved at Ku-band. To author's knowledge, this work achieves the widest bandwidth Tx beamforming chip. Application areas are ground terminals capable of communications with X, Ku and Ka-band satellite constellations.**



***Keywords*— phased-array, SATCOM, wideband, PA, SiGe HBT**


## I. Introduction

The demand for communications is increasing worldwide leading to the necessity for better telecommunication coverage and the availability of internet access across the globe. This also include terminals on planes and ships, where satellite systems, with their ubiquitous coverage over oceans, are used.

Current SATCOM systems enable high data rate and low latency communications with low Earth-orbit (LEO) and medium Earth-orbit (MEO) satellites. However, there are multiple frequencies used, from X-band (8 GHz), Ku-band (14 GHz) and Ka-band (29 GHz) (Fig.1a). A ground terminal which covers all satellite bands in a single system simplifies the hardware complexity, allows for worldwide operation over multiple providers, and reduces the overall terminal cost.

This paper presents an 8-channel transmit (Tx) beamformer designed in a 90nm SiGe BiCMOS technology. The design covers the X, Ku and Ka SATCOM bands in a single chip for next-generation phased-array systems. The 8-channel chip is compact (3.9×4.7 mm) with 0.4 mm chip-scale-package and fits well in a 31 GHz phased-array design based on the 2×2 (quad-antenna) approach [1].


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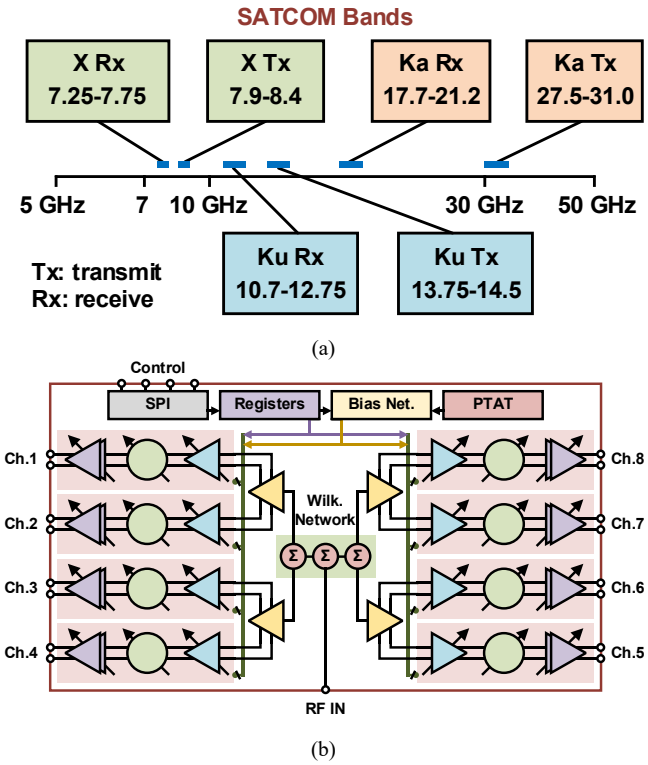


Fig. 1. (a) X, Ku and Ka-band SATCOM frequencies for commercial and defense systems. (b) Block diagram of the wideband 8-channel Tx beamformer chip.

## II. Eight-Channel Wideband Beamformer

Fig.1b presents a block diagram of the wideband 8-channel Tx beamformer. The input power is distributed to the channels using a wideband two-section Wilkinson network, followed by a single-ended to differential converter. The channels are all differential and contain a wideband VGA, a 5-bit phase shifter and a wideband power amplifier. The outputs are also differential which improves the stability over a wide frequency range. Also, wideband antennas are differential in nature, and

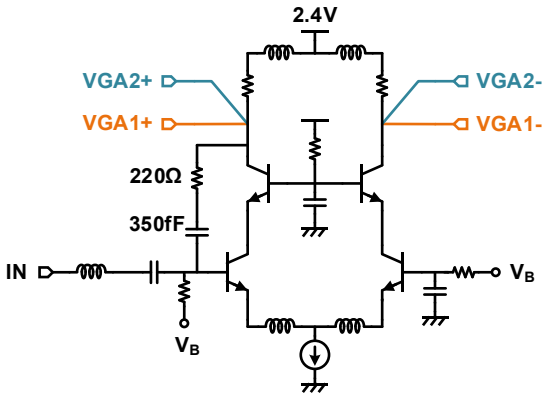


Fig. 2. Wideband single-ended to differential converter with input resistive feedback. The output node has a current split to two VGAs.

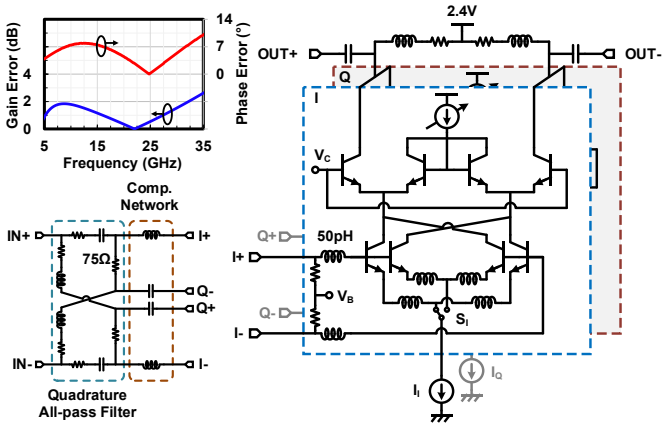


Fig. 3. Wideband vector-modulator phase shifter and the QAF network with the simulated I/Q magnitude and phase error.

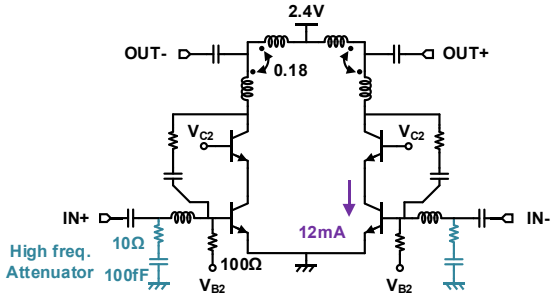


Fig. 4. Wideband differential output power amplifier with T-coil matching (second stage shown).

differential output ports eliminate the use of wideband baluns and result in a more efficient system.

### A. Technology

The chip is implemented in the Tower Semiconductor 90nm SiGe BiCMOS process (SBC18S5) with 7 aluminum metal layers. The top two metal layers are used for high Q inductors (Q ~16 at 25 GHz). MIM capacitors with density of 2.8 fF/μm$^2$ are also present in the process. All the inductors, capacitors and the transmission lines are modelled using Integrand Software EMX with the Cadence Suite. The simulated fT and fmax of a 3μm emitter length HBT is 245 GHz and 304 GHz, respectively, at 1.5-2.0 mA/μm current density.

### B. Wilkinson Network

The input power is distributed using a 1:4 Wilkinson network with two-section Wilkinson-dividers to increase the bandwidth (Fig.1b). The 1:4 divider network insertion loss (ohmic loss) is 1.8-3.8 dB at 5-33 GHz and does not include the 6 dB division loss. The increase in the insertion loss is compensated by increasing the channel gain at high frequencies, resulting in a nearly flat response.

### C. Single-ended to Differential Stage (S2D) and VGA

The S2D employs a fully differential cascode amplifier topology with one input being AC-grounded (Fig. 2). The single-ended to differential conversion is ensured by the common-mode rejection of the tail bias current source. The wide bandwidth is achieved by employing a shunt 220 Ω and 350 fF feedback. The simulated common-mode rejection is 16.2-18.6 dB at 5-33 GHz. This is followed by two VGAs based on a cascode design with current steering (not covered for brevity). The differential and common-mode gain of the S2D+VGA is 5-10.2 dB and -17 to -7.4 dB at 5-33 GHz, resulting in a common-mode rejection of 21-17.6 dB, and ensuring a reasonable purity for the differential signal.

### D. Active Phase Shifter

The active phase shifter employs a vector modulator architecture with a quadrature all-pass filter (QAF) (Fig. 3). The I/Q signals are fed to two variable gain amplifiers with current-steering, and the output signals are added in the current mode. For wideband operation, de-Q series resistors are used for the inductors and the capacitors in the QAF network [2]. This degrades the noise figure (NF) and gain by ~3 dB but is required for wideband operation with low I/Q errors. The QAF network is followed by an LC compensation network to introduce a nearly resistive interface to the VGAs. Note that the VGAs employ an emitter inductor to lower their noise figure and increase their input impedance (and make it resistive) [3].

The phase shifter has simulated small-signal gain of 1.6-4.5 dB and a NF of 8.4-11 dB at 5-33 GHz. An I/Q error of up to 2.2 dB and 8.3° is present over the entire bandwidth, which is relatively high. This is due to the use of a single-stage LC I/Q network for a 6.5:1 bandwidth design, and a better response can be achieved using a 2-stage LC I/Q network. Therefore, a 6$^{th}$ bit is employed in the VGA current steering to compensate for the I/Q error, and this results in true 5-bit operation at 5-33 GHz (different 32 phase shifter states chosen for different frequency bands).

### E. Power Amplifier

The wideband power amplifier is composed of two differential cascode amplifiers. The driver stage and output stages both employ resistive shunt feedback to increase the bandwidth of operation. A tail current source is not implemented in the PA design to improve the voltage headroom and increase

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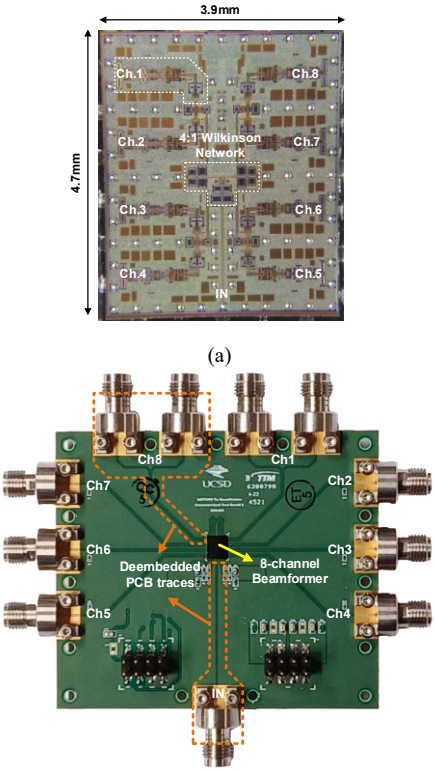


Fig. 5. (a) Die photo of the 8-channel Tx beamformer chip, (b) PCB for beamformer evaluation. Some ports are differential all the way to the connectors and some ports are (half) terminated by 50 Ω and taken as single ended to the connectors.

the output power, leading to pseudo-differential operation and a class AB design. At the output stages of both the driver amplifier and power amplifier, bridged T-coils are implemented to achieve a wideband power match.

The common-emitter HBT devices also include 100 Ω resistors at their base feeds. These are effectively shunted to ground in RF operation and intentionally reduce the small-signal gain to improve the wideband stability. Also, shunt RC networks are added at the input to degrade the small-signal gain at > 40 GHz, again for stability. Without this network, the PA would have gain up to 60 GHz resulting in potential instabilities when packaged. The RC and 100 Ω stability-improvement networks are implemented only at the input side in order not to degrade the output power but do reduce the amplifier efficiency a bit.

The two-stage power amplifier has a simulated small-signal gain of 27.3-24.7 dB at 5-33 GHz, and a OP1dB of 10-13.4 dBm. The PA consumes 76.8 mW from a 2.4 V supply, resulting in a PAE of 13-25% over the entire band.

### *F. Chip Performance*

The chip has a simulated electronic gain of 24.7-30.5 dB at 5-33 GHz, including the 6 dB division loss. The electronic gain (S21) is defined as the power at the differential output port divided by the input at the chip common port. Each channel has simulated power consumption of 294 mW at P1dB, resulting in a peak system PAE of 12.7% at 14 GHz. The chip is controlled

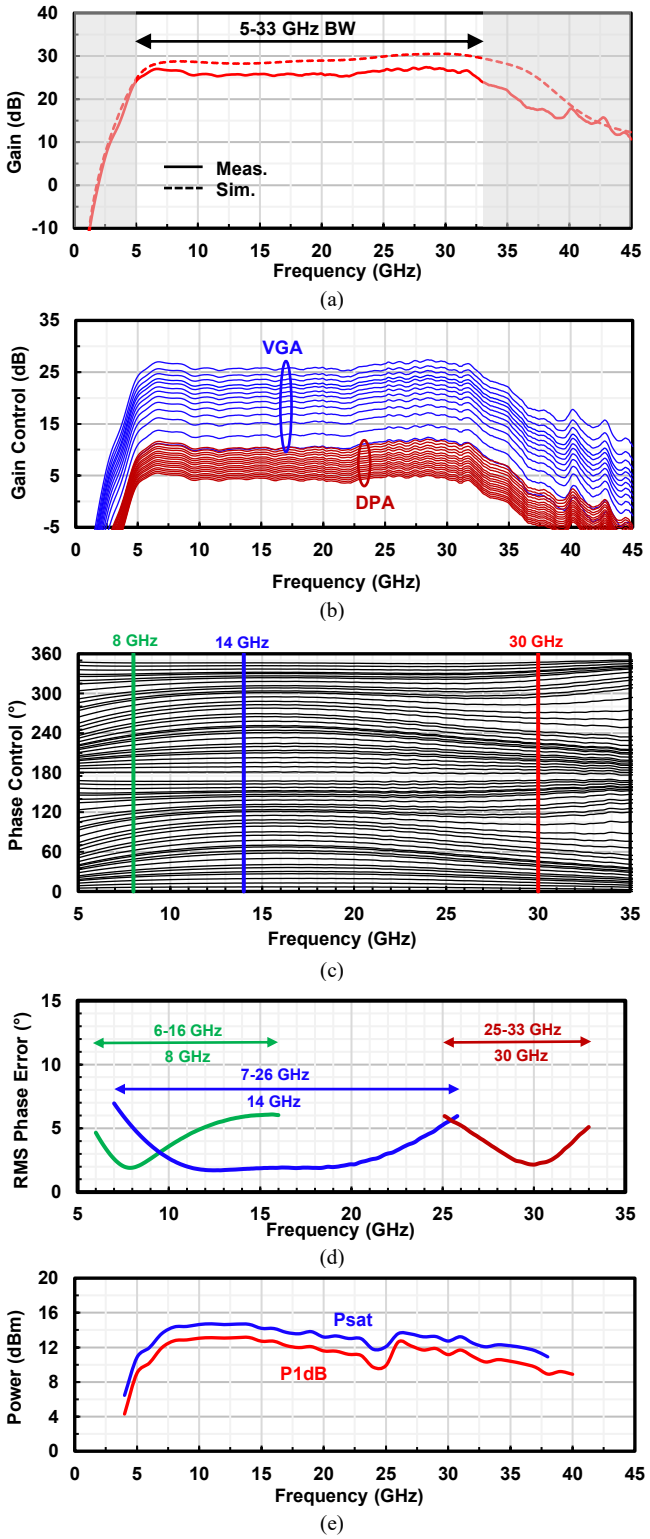


Fig. 6. (a) Electronic gain, (b) Gain control, (c) Phase control, (d) RMS phase error for 3 different phase-shifter settings, (e) Large-signal performance.

using a high-speed SPI and a PTAT reference current source is used for biasing and has 380 µm bump pitch with SAC305 balls.

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TABLE I. COMPARISON WITH STATE-OF-THE-ART BEAMFORMERS (IN TX MODE)

| Reference | This Work | JSSC'21 [4] | ISSCC'21[5] | RFIC'19[6] | RFIC'18 [7] | IMS'18[8] |
|---|---|---|---|---|---|---|
| **Technology** | **90nm SiGe BiCMOS** | 90nm SiGe BiCMOS | 45-nm SOI CMOS | 0.13um SiGe BiCMOS | 0.13um SiGe BiCMOS | SiGe BiCMOS |
| **Frequency (GHz)** | **5-33** | 15.25-50.5 | 24-30 | 24.2-30.5 | 24.5-30.5 | 23-29 |
| **Fractional BW (%)** | **147** | 107.2 | 22.2 | 23 | 21.8 | 23.1 |
| **Architecture/Polarization** | **4x2 Tx Single Pol.** | 4x1 Tx Single Pol. | 8x2 Tx/Rx Dual Pol. | 2x2 Tx/Rx Single Pol. | 2x2 Tx/Rx Single Pol. | 2x2 Tx/Rx Single Pol. |
| **Gain Control (dB)** | **21** | 16.2 | - | >30 | 26 | >35 |
| **Phase Resolution (bit)** | **5** | 5 | - | - | 6 | 6 |
| **OP1dB (dBm)** | **9-13.3** | 13.5-14.7 (20-50 GHz) | 20 | 18 | 16.2 | 13 |
| **OPsat (dBm)** | **10.8-14.7** | 14.4-15.3 | - | - | - | - |
| **$P_{DC}$/Channel (mW)** | **240 at P1dB** | 250 at P1dB | 300 at 11dBm | 450 at P1dB | 376 at P1dB | 248 at P1dB |

## III. MEASUREMENTS

Measurements are done on a packaged chip and not on-wafer. The beamformer die photo is shown in Fig. 5 together with the test module. The chip size is 3.9×4.7 $mm^2$ and is limited by the 380 μm chip-scale package pitch. The 8-channel transmit chip is first placed on an RF PCB using flip-chip assembly. The small-signal and large-signal performance are obtained using a 4-port PNA-X (Keysight N5245B to 50 GHz) with a single-ended input (port 1) and differential outputs (port 2). The PCB trace and connector losses are de-embedded, and the reference planes are at the chip input and output ports (on the PCB). The chip consumes 1.8 W with a 2.4 V supply at small signal. The power increases to 1.9 W at P1dB resulting in 240 mW per channel.

Fig. 6a presents the electronic gain of the 8-channel beamformer. The maximum electronic gain is 27.4 dB with the 3-dB bandwidth of 5-33 GHz, and all channels are within +/-1 dB of each other. The reverse isolation (S12) is -48 to -70 dB at 5-33 GHz, ensuring unconditionally stable operation. The gain control is shown in Fig. 6b. The VGA and DPA (driver for the PA) have 15 dB and 6 dB gain control, respectively, resulting in 21 dB of gain control.

Fig. 6c presents the measured phase performance. The native 6-bit performance is trimmed to 32 states at 8 GHz, 14 GHz and 30 GHz, and the RMS phase error is plotted. One can see that 5-bit operation is achieved with an RMS error of < 5.2° for each setting. The RMS amplitude error is ~1 dB for each case.

The beamformer chip delivers a peak P1dB of 13.1 dBm at 14 GHz. Saturated output power (OPsat) is defined when the beamformer is driven 3 dB higher power than the input 1dB compression point. The beamformer can deliver a maximum of 14.7 dBm OPsat at 14 GHz. The kink around 25 GHz happens at K-band and does not affect the intended SATCOM operating frequencies. We have traced this to the interstage matching network between the driver and the power amplifier.

Table 1 presents a comparison with other state of the art beamformers. This work has the widest bandwidth and covers the X, Ku and Ka SATCOM bands. Also, all presented results are packaged and not on-chip, and the chip is unconditionally stable for all port terminations (open, short and 50 Ω).

## IV. CONCLUSION

An ultra-wideband 8-channel Tx beamformer is presented. The channels employ a differential architecture with 5-bit of phase control and high OP1dB. This work is intended for phased array systems operating at multiple SATCOM bands.


## ACKNOWLEDGMENT

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