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A Wideband Ultra-Low Noise 15-55 GHz Dual-Beam Receive Phased-Array Beamformer with 2.9-4.2 dB NF

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***Abstract*— This paper presents an 8-channel 15-55 GHz dual-beam receive (Rx) phased-array beamformer in 90 nm SiGe BiCMOS process capable of synthesizing two simultaneous beams at any frequency. The design achieves ultra-low noise figure in the 15-55 GHz band together with high linearity per element. Each channel also has a 5-bit phase control and 22 dB gain control. The outputs of the 4 channels for the two beams are combined using two independent Wilkinson networks. The measured chip has an electronic gain of 25 dB with a NF of 2.9-4.2 dB at 15-50 GHz, and an IP1dB of -31±3 dBm. To the authors' knowledge, this work achieves the lowest NF for wideband Rx beamformers in the same frequency range. The chip also demonstrates an EVM of < 2.5% at 25-42 GHz for 5G 400 MHz OFMD waveforms with a PAPR of 11.6 dB. Application areas are phased-arrays covering multiple 5G bands and multi-standard systems.**

***Keywords*— wideband, beamformer, LNA, 5G, phased array, receiver, SiGe BiCMOS.**

I. Introduction

Millimeter-wave communication systems have enabled high data rates benefiting from the large available spectrum at higher frequencies. The key enablers for these systems are phased arrays based on multi-channel SiGe/CMOS beamformer ICs which offer higher lever of integration and lower cost. Multiple frequencies are suggested for the fifth-generation (5G) mobile networks from 20 to 60 GHz including the 28 GHz, 39 GHz, and 47 GHz bands which are already approved for use. Prior work on beamformers for 5G applications demonstrated excellent performance but the bandwidth is usually limited to only a single 5G band [1], [2], [3]. Other work presented dual-band [4] or wideband [5], [6], [7] operation but with a high noise figure at 20-100 GHz.

This paper presents an 8-channel dual-beam 15-55 GHz Rx beamformer chip implemented in a 90 nm SiGe BiCMOS process. Any beam can operate at any frequency in the 15-55 GHz range. The current work is not intended to be a wideband 5G Tx/Rx chip, but rather as an ultra-low-noise phased-array chip for monitoring 5G radiation in FCC base stations, and to ensure spectrum conformity. Two beams are used to search the space in half the time. The design can also be extended to 4 or 8 simultaneous beams.

II. RX Beamformer Design

The block diagram of the beamformer chip is shown in Fig. 1. The chip has 4 differential inputs which are intended to be connected to wideband differential antennas. Each channel pair share a low-noise amplifier (LNA) which also acts as a power splitter and generates dual differential outputs for the two channels. The LNA is followed by a phase shifter, a variable-gain amplifier (VGA), and a differential to single-ended (D2S) stage. The channel outputs are then combined using two independent 4:1 Wilkinson networks. All the active circuits are fully differential to improve stability and reduce coupling between the channels. This work is an extension of [5] with a much better noise figure, lower power consumption, and two simultaneous beams.

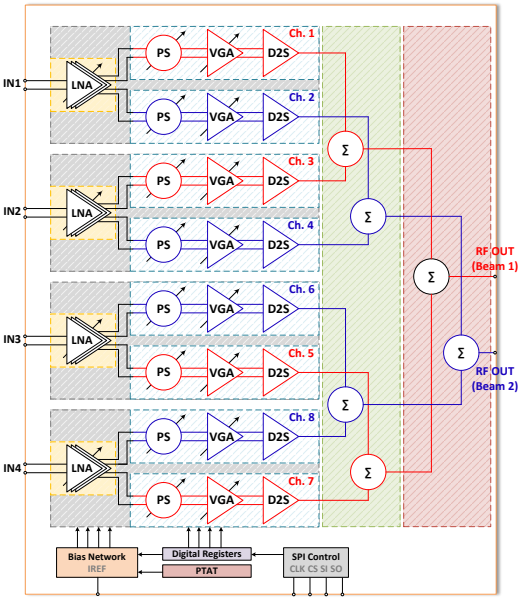

Fig. 1. Block diagram of the wideband 15-55 GHz 8-channel two simultaneous beam Rx beamformer.

A. Technology

The process used in this work is TowerJazz 90 nm SiGe BiCMOS (SBC18S5) process. The heterojunction bipolar transistor (HBT) in this technology has a maximum f_t/f_{max} of 270/300 GHz with parasitic extraction to the top metal layer. The NF_{min} at 35 GHz is 1.1 dB at a current density of 0.25 mA/μm. The process features 7 aluminum metal layers, with 2.8 μm thickness for the two upper metal layers allowing for a high-quality factor for the passives.

B. Low-Noise Amplifier

The LNA consists of three differential common-emitter stages (Fig. 2(a)). The first stage is a low-noise cascode design while the second and third stages use resistive feedback to extend the operation bandwidth. T-coils are used for

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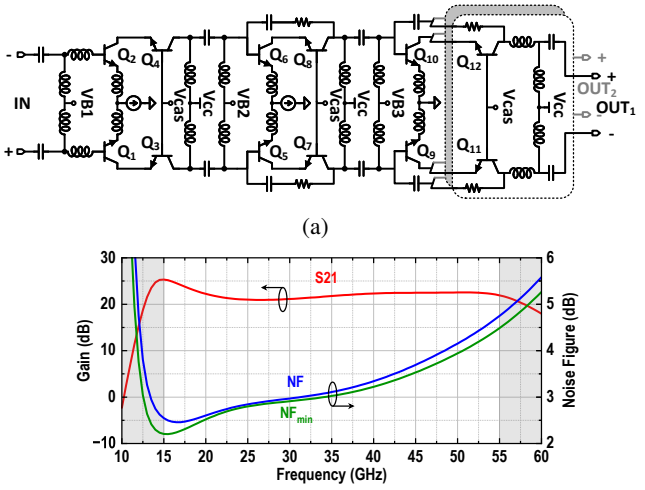

(a)

(b)

Fig. 2. (a) Wideband 3-stage LNA with active splitter, (b) simulated gain and noise figure of the 3-stage LNA.

matching at the input and the output to achieve wideband input and output matching. Interstage matching is done using capacitively coupled resonators to extend the bandwidth while the feedback resistors reduce the in-band gain ripples [8], [9]. The cascode devices and the load network in the third stage are split into two allowing for power splitting between the two beams.

The LNA (with two outputs) has a simulated gain of 21 dB with a 3-dB bandwidth of 18-57 GHz (Fig. 2(b)). A NF of 2.5-4.2 dB is achieved at 17-50 GHz with a midband NF of 3.1 dB at 35 GHz. Fig. 2(b) also shows wideband noise matching with less than 0.2 dB difference between the noise figure and NF_{min} at 17-50 GHz. The LNA IP1dB is high and is -19±3 dBm (OP1dB of 0 dBm). Its power consumption is 100 mW (50 mA/2 V) due to its linearity. Note that the last stage is duplicated for two channels and consumes 25 mW per stage. To our knowledge, this is the lowest noise LNA in the 15-55 GHz band.

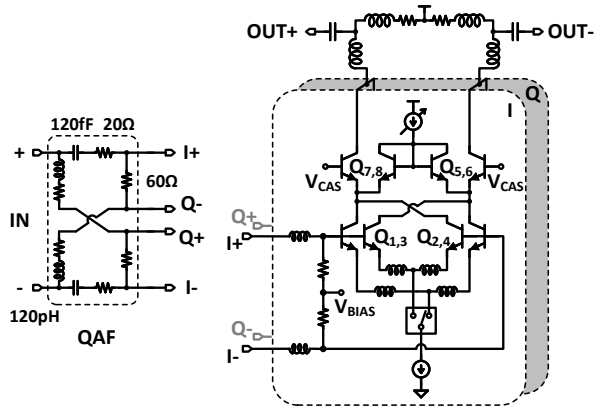

Fig. 3. Wideband 5-bit active phase shifter with inductive matching.

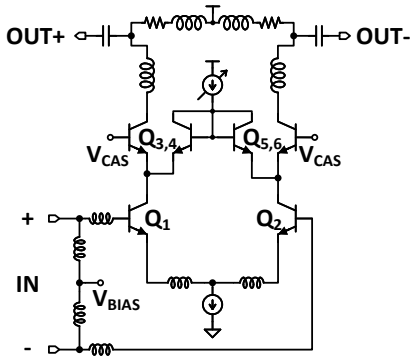

Fig. 4. 4-bit variable-gain amplifier.

C. Active Phase Shifter

The active phase shifter consists of a quadrature all-pass filter (QAF) followed by two current steering VGAs (Fig. 3). The QAF network generates differential quadrature signals which are then weighted and summed by the VGAs to achieve the required phase shift. The QAF network includes de-Q resistors to lower the quality factor of the network and reduce the effect of the loading capacitance on the network response [10]. This allows the network to generate accurate wideband IQ signals but reduces the gain and increases the NF. The IQ network has < 1.4 dB gain error and < 10° phase error at 15-50 GHz.

The VGAs are designed as wideband high-linearity low-noise amplifiers with emitter degeneration inductors (L = 50 pH) and series matching inductors (L = 40 pH) at their base nodes. Two current steering DACs are used to control the gain of the I/Q VGAs and a T-coil matching network with a series de-Q resistor is used at the output to achieve a wideband gain response.

The phase shifter has a simulated mean gain of -2.5 dB over the 32 phase states with an rms gain error of < 1.5 dB at 15-55 GHz. The simulated rms phase error is < 5.6° and the mean NF is 15.5 dB. The simulated IP1dB is -4 dBm for a power consumption of 48 mW (24 mA/2 V).

D. Variable-Gain Amplifier

The VGA is based on a Gilbert cell with the current steered away from the cascode devices using a 4-bit current steering DAC (Fig. 4). T-coil matching is used at the input and output to achieve a wideband gain response.

The maximum simulated gain is 8 dB and it has a 3-dB bandwidth at 15-58 GHz. The VGA has a 3 dB NF at the highest gain state and a -4.5 dBm IP1dB, all at 35 GHz. The VGA can achieve 19 dB gain control and consumes 24 mA from a 2 V supply.

E. Differential-to-Single-Ended Stage

The D2S is based on common emitter/emitter follower stages to combine the differential inputs into a single-ended output. The D2S provides 19 dB CMRR at 15-55 GHz and achieves 4 dBm IP1dB while consuming 10 mW (5 mA/2 V).

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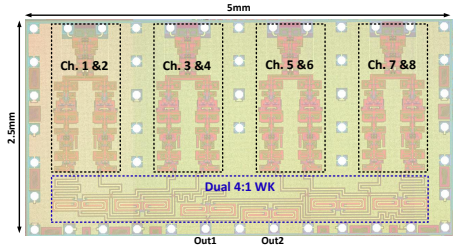
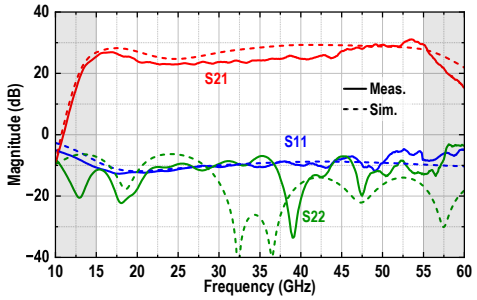
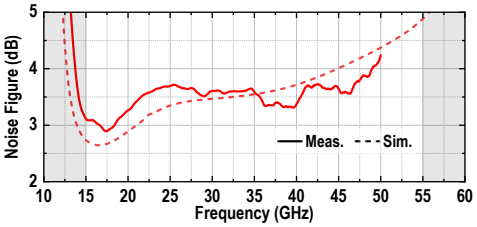


Fig. 5. 8-channel Rx wideband phased-array chip (5 mm × 2.5 mm).



(a)



(b)

Fig. 6. Measured (a) S-parameters at maximum gain state, (b) noise figure.

F. Wideband Rx Channel and Wilkinson Network

The entire channel has 28-30 dB simulated gain and IP1dB of -31±3 dBm at 15-55 GHz. The linearity is limited by the IP1dB of the phase shifter and the VGA. The simulated NF is 2.7-4.3 dB at 15-50 GHz. The channel power consumption is 180 mW from a 2 V supply.

The dual 4:1 combining networks are constructed using single-section Wilkinson power combiners with > 10 dB isolation with < 0.9 dB insertion loss at 17-55 GHz. The transmission lines from the outputs of the channels to the Wilkinson combiners are meandered to ensure equal line length. The simulated ohmic loss for the entire Wilkinson network including the routing loss is 2-3.5 dB at 15-55 GHz resulting in a channel electronic gain of 25-28 dB.

III. Measurements

The beamformer chip is measured using a probe station, GSSG/GSG probes for the RF input/output ports, and a Keysight N5247A PNA-X network analyzer (Fig. 5). The chip consumes 1.48 W from a 2 V supply (185 mW per channel). The chip employs SAC305 bumps with 0.4 mm pitch and can be directly flipped on a PCB for a chip-scale package.

The measured channel S-parameters are shown in Fig. 6(a). A 6 dB is added to S21 to account for the excess loss in the combining network due to the fact that only one channel is energized. The electronic gain is 23-30 dB at 15-55 GHz and is 2-4 dB lower than the simulated gain at 15-45 GHz. Fig. 6(a) also shows wideband input and output matching at 15-55 GHz. The reverse isolation is > 40 dB.

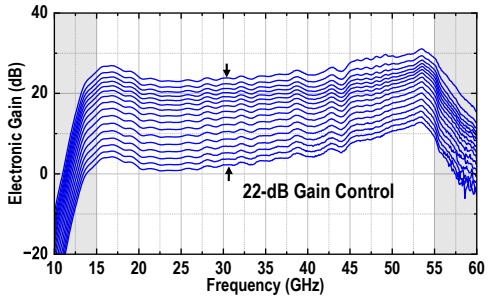


Fig. 7. Measured gain response across the VGA states.

For NF measurements, a wideband balun is added before the chip and its loss is then de-embedded from the measurement. The noise figure is < 4 dB up to 48 GHz with a minimum noise figure of 2.9 dB at 17.5 GHz (Fig. 6(b)). The measured beamformer IP1dB is -31±3 dBm /channel at 15-55 GHz.

The VGA provides 22 dB gain control as shown in Fig. 7. The normalized 6-bit phase response is shown in Fig. 8. The rms phase error is < 11° at 15-55 GHz for 64 phase-states. When trimmed to 32 phase states at 35 GHz (32 out of 64 states are chosen), an rms phase error < 5.6° can be achieved at 20-44 GHz resulting in a true 5-bit operation. Similar trimming can be done at 20 GHz and 50 GHz to achieve 5-bit operation at different frequencies (Fig. 8). The rms gain error across the 64 phase states is < 1.6 dB at 15-55 GHz. All 8 channels were measured and show the same response with < ±1.5 dB gain variation.

The measured constellations and EVMs at different frequencies with 400 MHz 5G NR signals with a PAPR (peak to average power ratio) of 11.6 dB are shown in Fig. 9. A Keysight M9384B VXG signal generator is used to generate the complex modulated signals and a Keysight N9040B UXA signal analyzer is used to extract the constellations and EVMs. The measured EVMs are < 2.32% at 25 GHz, < 1.98% at 28

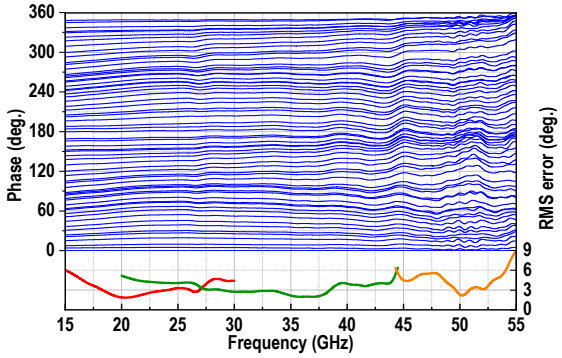


Fig. 8. Measured normalized phase response across the 64 phase shifter states.

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Table 1. Performance Comparison with State-of-The-Art Wideband Beamformers

Design	This work	[5] TMTT'22	[4] JSSC'19	[11] TMTT'16	[6] JSSC'21
Technology	**90nm SiGe BiCMOS**	90nm SiGe BiCMOS	65nm CMOS	130nm SiGe BiCMOS	22nm FD-SOI
Frequency (GHz)	**15-55**	15-57	27-29.75 /35-38.75	2-16	43-97
Function	**Rx**	Rx	Rx	Rx	Rx
# of channels	**8**	4	4	8	1
# of beams	**2**	1	2	up to 4	1
Gain (dB)	**25**	25	33/26.5	11	14
NF (dB)	**2.9-4.2**	4.7-6.2	5.7/8.5	11.5-12.3	12.5-16.5
Phase step (°)	**11.25**	11.25	-	11.25	-
Gain control (dB)	**22**	18	-	8	-
IP1dB (dBm)	**-31±3**	-30 to -23	-30/-23	-17 to -14	-8 to -5.6
Modulation	**QPSK, 16-QAM, 64-QAM, 256-QAM (400 MHz 5G NR)**	QPSK, 16-QAM, 64-QAM, 256-QAM (400 MHz 5G NR)	CW	CW	64-QAM (0.2-1 GHz single carrier)
EVM (%)	**1.7-2.5**	1.5-2.76	-	-	1.6-3.6
P_{DC}/Ch. (mW)	**185**	242	52.5	250	36

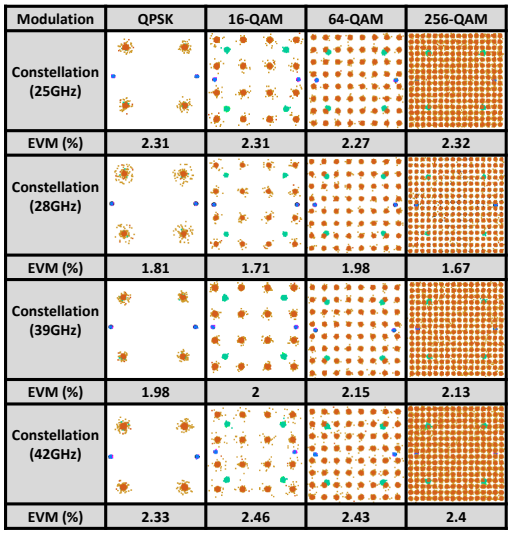

Fig. 9. Measured constellation and EVM performance with 400 MHz 5G NR signals.

GHz, < 2.15% at 39 GHz, and < 2.46% at 42 GHz.

The 8-channel receive beamformer is compared with previous work on wideband beamformer in Table 1. It achieves the lowest noise figure with high gain across a wide bandwidth covering multiple 5G bands, provides two simultaneous beam operation, and with lowest EVM.

IV. Conclusion

An 8-channel dual-beam receive beamformer IC is presented in this paper. The design employs multiple bandwidth extension techniques in the active circuitry to achieve ultra-wideband performance with low noise figure. This chip is suitable for large phased arrays for 5G FR2 bands and multi-standard applications.

Acknowledgment

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