A 25-50 GHz Phase Change Material (PCM) 5-Bit True Time Delay Phase Shifter in a Production SiGe BiCMOS Process

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***Abstract*— This paper presents the implementation and measurement results of a wideband (DC-67 GHz) phase change material (PCM) switch and a miniature 5-bit true time delay (TTD) phase shifter. A series-shunt single pole double throw (SPDT) switch is implemented based on the 4-terminal PCM switch integrated in the back-end-of-line (BEOL) of Tower Semiconductor SBC18H3 0.18 μm SiGe BiCMOS process. The PCM Switch core has a nominal R_{ON} of 3 Ω and a C_{OFF} of 4 fF leading to a FoM of 12 fs. This core performance leads to a wideband SPDT IL of 0.9 dB at 30 GHz and to 45 dB of isolation. Using the SPDT switch, a 5-bit 0-124 ps TTD unit with a transmission line based implementation is presented. It exhibits an RMS group delay error of less than 2 ps from 25-50 GHz and less than 3 ps from 6-55 GHz.**

***Keywords*— phase change material (PCM), PCM switch, delay lines, true time delay (TTD), insertion loss (IL), isolation, phase shifter**

I. Introduction

Phase change material switches present tremendous advantages for RF and microwave applications as they offer an increase in the $R_{ON}C_{OFF}$ FoM by an order of magnitude, in comparison to a standard CMOS SOI process. They are also naturally non-volatile, meaning that they can retain their state indefinitely [1]-[7]. The PCM switch used in this work is developed by Tower Semiconductor and is integrated in the BEOL of a 0.18 μm SiGe BiCMOS node (Fig. 1). The switch is fundamentally a chalcogenide based crystal that possesses a high resistivity amorphous state and a low resistivity crystallic state [6]-[7]. The transition from one state to the other is accomplished by applying voltage pulses with specific characteristics onto a heater resistor that accompanies the crystal. These pulses offer the appropriate thermal excitation for the crystal to change states between ON ($R_{ON} = 3$ Ω) and OFF ($C_{OFF} = 4$ fF) [7].

Besides the conventional applications of 1:N switch networks, low loss and high isolation switches have long been a prerequisite for the design of true time delay circuits. TTD units provide a variable time delay within a frequency bandwidth and can be used in wideband phased arrays, radars and imaging or tracking sensors [8], [13]. Several attempts for TTD designs have been presented in literature including varactor-loaded transmission lines (TLs) that provide continuous group delay variation [9]-[10] by tuning the TL's distributed capacitive loading. In a second approach, TTD is implemented using variable length switched TLs. Depending on the selected route, the signal will be propagated through a variable group delay path [11], [12], [15]. Finally, all-pass networks have also been utilized in TTD units, as in [13]-[14].

The low IL and high isolation of the PCM switch have been validated in previous work [6]-[7]. However, higher complexity PCM-based switches have yet to be reported. In this work, we will present a high-isolation SPDT switch based on the PCM switch core. In addition, a transmission line based 5-bit TTD unit that utilizes the SPDT is also presented. The phase shifter exhibits the best reported group delay flatness over frequency and the largest absolute group delay (on a chip).

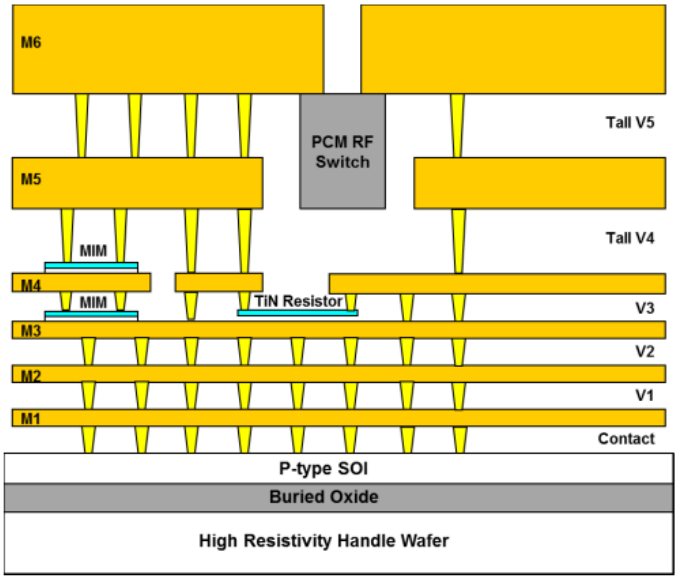

Fig. 1. A schematic cross-section of the SiGe BiCMOS SBC18H3 process where the PCM RF switch is monolithically integrated between M5 and M6.

II. PCM Pulsing and Nominal Specifications

The PCM switch requires specifically shaped voltage pulses to be applied onto its heater resistor to transition from the OFF-state ($C_{OFF} = 4$ fF) to the ON-State ($R_{ON} = 3$ Ω) and vice versa. The switch comes naturally in the low-resistivity, crystallic state. For the switch to transition to the OFF-state, a voltage pulse needs to be applied on the heater resistor for the crystal to amorphize. In order for it to get back at its ON state, another pulse with different characteristics needs to be re-applied.

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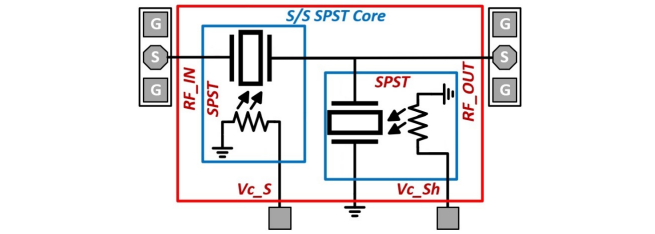
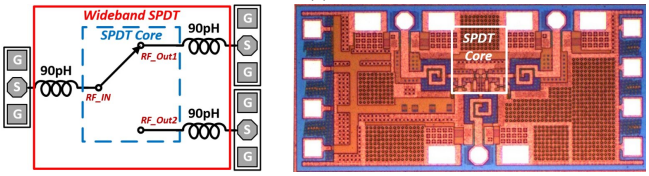
III. SPDT DESIGN AND MEASUREMENTS

As a building block for the SPDT switch, a high-isolation series-shunt switch design is utilized (Fig. 2a). The SPDT switch (Fig. 2b) incorporates two SPST switches and two 90 pH series inductors with a Q of 12 at 30 GHz at the input and output port to tune out the SPST capacitance.

The measured SPDT exhibits excellent impedance matching (S_{11}, S_{22} < -15 dB from 0-67 GHz) and an isolation of 45 dB at 30 GHz as shown in Fig. 2c. For the ON state, the IL from the input to the output GSG pads (reference planes) is 0.9 dB at 30 GHz. This includes the GSG pad loss, the inductor loss due to the finite Q, the matching loss and the PCM switch core loss (Fig. 2d). The SPDT switch insertion loss, when referenced to the inductors (switch ports) is estimated to be 0.7 dB at 30 GHz when the GSG pad loss (0.05 dB each) and transmission-line loss (0.05 dB total) are subtracted.



(a)



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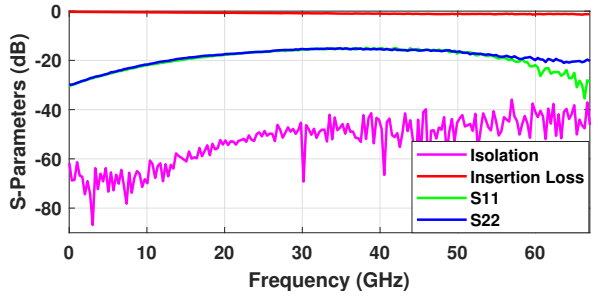
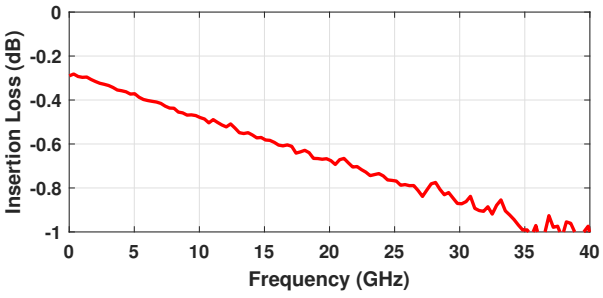


(c)

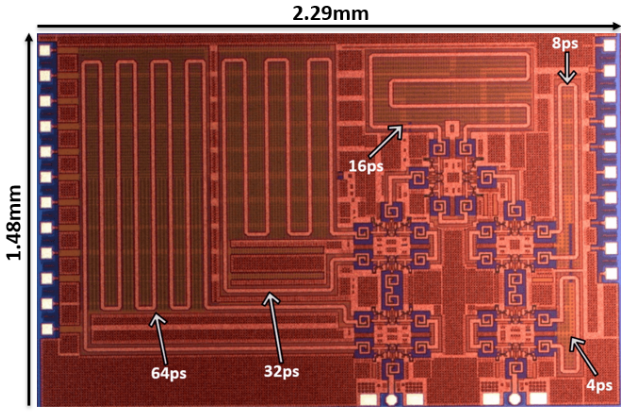


(d)

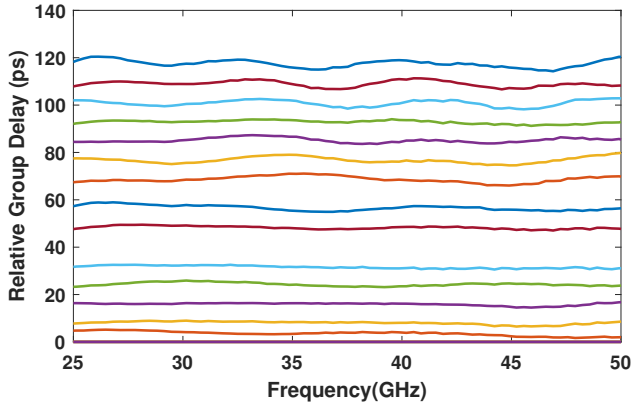
Fig. 2. (a) Schematic representation of the series-shunt SPST that is used as the building block of the SPDT. (b) Layout and schematic representation of the SPDT. (c) Measured S-parameters of the SPDT switch. (d) Measured insertion loss of the SPDT switch.

IV. TTD PHASE SHIFTER DESIGN AND MEASUREMENTS

The design of the TTD phase shifter employs cascaded switches and 50 Ω transmission lines of binary weighted group delay lengths (Figs. 3a-4). The binary step is 4 ps, meaning that bit-0 corresponds to 4 ps of delay, bit-1 to 8 ps of delay and all the way to bit-4 with a 64 ps delay, leading to a maximum 124 ps of relative group delay, with regard to the reference path.



(a)



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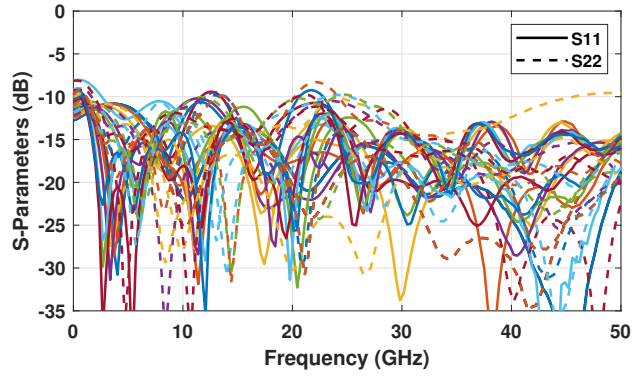

(c)

Fig. 3. (a) Layout of the 5-bit TTD phase shifter. (b) Measured group delay states. (c) Measured S-parameters of the TTD PS over all group delay states.

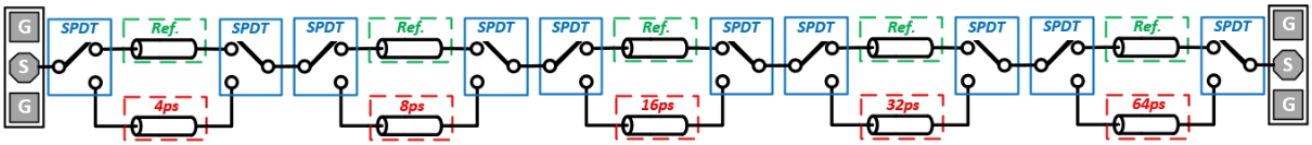

Fig. 4. Schematic Representation of the 5-bit TTD phase shifter

Table 1. Performance comparison of published TTD circuits

	This Work	[11]	[12]	[14]	[15]
IC Process	**PCM 0.18um SiGe BiCMOS**	0.25um CMOS	0.13um CMOS	28nm CMOS	RF MEMS
Frequency (GHz)	**25-50**	10-50	15-40	3-30	8-12
Max. Relative Group Delay (ps)	**124**	32.8	42	68.5	100.8
Nominal Insertion Loss (dB)	**10.4 at 30 GHz**	15.5 at 30 GHz	14 at 28 GHz	13.5 at 28 GHz	1.6 at 12 GHz
Resolution (ps)	**4**	Cont.	3	4.9	6.3
RMS Group Delay Error (ps)	**<2**	N.A	N.A	<2	N/A
Pdc (mW)	**Passive**	Passive	8.6-24.6	Passive	Passive
Area (mm^2)	**3.39**	0.22	0.99	0.34	21.32

The PCM SPDTs allow for excellent isolation between the activated and de-activated RF paths, thereby eliminating S_{21} resonances which can appear in TTD units. Also, the excellent matching between the cascaded SPDT switches allows for the reflected waves to minimally impact the group delay flatness, meaning that the ripples in the group delay are almost non-observable (Figs. 3b-c). As a result the measured group delay flatness is < 2 ps or half an LSB from 25-50 GHz and < 3 ps from 6-55 GHz. The 5-bit TTD insertion loss at 30 GHz varies between 6.1 dB (minimum group delay state) to 14.9 dB (maximum group delay state) and is given mostly by the transmission-line loss of the large group-delay states. A comparison with different TTD units is presented in Table 1.

V. Conclusion

This paper presented a miniature 5-bit transmission line-based TTD phase shifter. The SPDT exhibits excellent impedance matching and isolation up to 67 GHz while the TTD unit exhibits the widest TTD performance and the highest absolute/relative group delay achieved. The TTD unit size of 2.29x1.48 mm makes it ideal for wideband 2-D phased-arrays with 0.5λ spacing at 55 GHz.

Acknowledgment

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