A 20–42-GHz IQ Receiver in 22-nm CMOS FD-SOI With 2.7–4.2-dB NF and −25-dBm IP1dB for Wideband 5G Systems

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***Abstract*— This article presents a 20–42-GHz in-phase and quadrature (IQ) receiver in 22-nm CMOS fully depleted silicon on insulator (FD-SOI). The receiver includes a wideband low noise variable-gain amplifier (LN-VGA), double-balanced IQ mixers, wideband I/Q generation network and wideband local oscillator (LO) driver, low-pass filters, and wideband intermediate frequency (IF) amplifiers. The measured receiver has a peak conversion gain of 25.3 dB with a 3-dB bandwidth of 19.8–42 GHz and an I and Q bandwidth of 5.7 GHz and covers the 5G millimeter-wave (mm-wave) band. The measured single-sideband noise figure (NF) is 2.7–4.2 dB at 24–42 GHz with an IP1dB of −26 to −23 dBm. The I/Q downconverter consumes a total of 102 mW from 0.8- and 1.6-V supplies. The IP1dB can be improved by 5 dB with an NF degradation by only 1.2 dB using RF VGA gain control. At peak gain and −8-dB VGA setting, the receiver dynamic range is 64–68 dB for a 100-MHz bandwidth, which is very high for low power consumption. The gain and phase mismatch between the I and Q channels is <0.6 dB and <6°, respectively. To the best of the authors' knowledge, this is the first wideband I/Q receiver that covers the entire mm-wave 5G band based on GF 22-nm CMOS FD-SOI. The application area is multistandard multigigabit per second communication systems.**

***Index Terms*— 5G, millimeter wave, 6G, 22-nm CMOS fully depleted silicon on insulator (FD-SOI), wideband receiver.**

I. Introduction

THERE is a growing interest for utilizing millimeter-wave (mm-wave) bands for 5G communication systems in recent years. Compared with current sub-6-GHz system, the mm-wave bands can provide larger bandwidth and gigabit-per-second data rate and enables different applications, such as virtual reality terminals.

The mm-wave links suffer from a large space loss factor and from atmospheric attenuation for long ranges [1]–[10]. Phased arrays and multiple-input–multiple-output (MIMO) have been proposed and are widely used to solve these issues by using spatial signal combining to enhance the desired signal and improve the interference rejection using MIMO and orthogonal frequency-division multiplexing (OFDM) standards. However, current work focuses on relatively narrowband applications, such as 24–29 and 37–42 GHz, and in the future, it is desirable to have a system that covers both bands. Wideband phased-array beamformers and LNA/power amplifier (PA) T/R modules have been recently investigated with good success [11]–[15]. Also, wideband quadrature downconverters have also been explored [16]–[23]. The goal is to build, in the future, phased arrays capable of 24–44 GHz operation for carrier aggregation in the 24-/28-/39-/41-GHz bands or for lowering the cost of phased arrays by using a single unit that covers multiple bands (see Fig. 1).

Wideband downconverters can be used either at the common port of analog beamforming phased array for single-beam or MIMO operation, or on each antenna element for digital beamforming. Also, if a large baseband bandwidth is available, the I/Q downconverter can be used as a single-sideband (SSB) intermediate frequency (IF) downconverter with an external 0°/90° coupler.

Fig. 2 presents several topologies for wideband receivers. A switched narrowband LNA design (with narrowband amplifiers or passive filters) can be used for highest linearity but is not suitable for placement at the antenna element due to its large area requirement and additional switch loss. It is suitable for use at the sum point in analog beamforming arrays. A tuned LNA can also be used as in Fig. 2(b), but this is hard to build due to the low-Q varactors or relatively low figure of merit (FoM) for SOI switches, which makes them nonideal for mm-wave tuning. Another solution is to build a wideband high-performance LNA with low noise figure (NF) and relatively high linearity, which can be used at both the sum point and at the antenna element [see Fig. 2(c)]. Their pros and cons are summarized in Fig. 2.

The bottleneck in wideband design is the generation of a wideband I/Q local oscillator (LO), which can be used for either SSB mixing to an IF or to baseband in an I/Q receiver. There are several popular methods to achieve a high-fidelity I/Q LO network: The first is to use a divide-by-two architecture and a voltage-controlled oscillator (VCO) running at twice the LO frequency [24]. This is hard to realize at 20–45 GHz as the LO needs to operate at 40–90 GHz. The second method is to employ a multistage polyphase filter (PPF), and for a 66% fractional bandwidth application, at least two stages are required. This results in high loss and sensitivity to loading capacitance [27], [28]. Therefore, it is a challenge to design wideband I/Q LO networks with low loss and with

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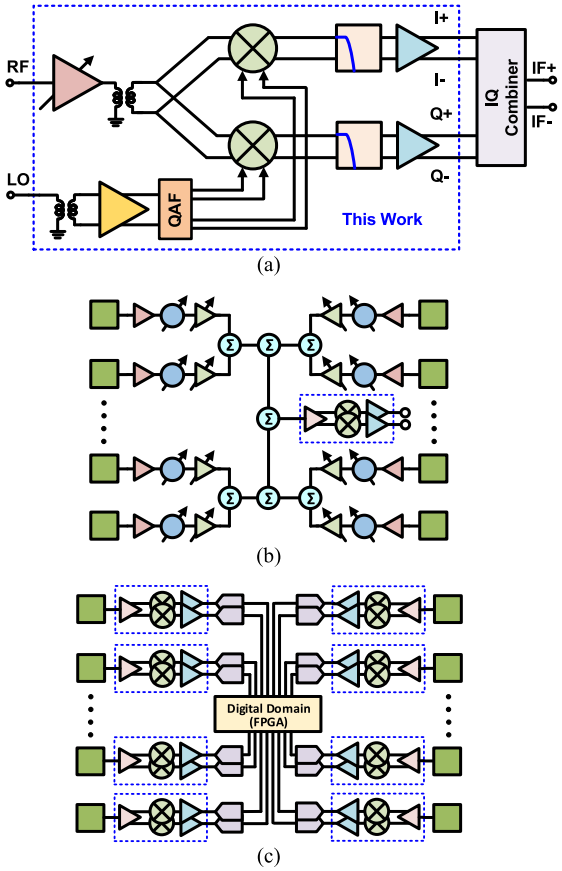
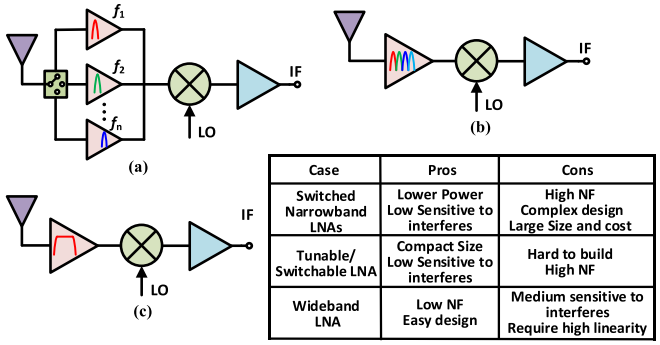


Fig. 1. (a) Wideband 20–44 GHz I/Q downconverter/receiver with large baseband bandwidth and an external in-phase and quadrature (IQ) combiner. The chip I and Q outputs can also be connected to ADCs for digital processing (direct conversion receiver or SSB receiver). (b) Analog beamforming architecture with I/Q downconverter at some point. (c) Digital beamforming architecture with I/Q downconverter on each antenna.



Case	Pros	Cons
Switched Narrowband LNAs	Lower Power Low Sensitive to interferes	High NF Complex design Large Size and cost
Tunable/ Switchable LNA	Compact Size Low Sensitive to interferes	Hard to build High NF
Wideband LNA	Low NF Easy design	Medium sensitive to interferes Require high linearity

Fig. 2. Three solutions for wideband receivers. (a) Switched narrowband LNAs. (b) Tunable/switchable LNA. (c) Wideband LNA.

low amplitude and phase mismatch. This is addressed in this work.

This article presents a low-IF or baseband wideband I/Q receiver, which covers the 24-, 28-, and 39-GHz 5G bands (see Fig. 1). The wideband I/Q network is generated by a quadrature all-pass filter (QAF) network with low amplitude and phase mismatch. The design details of each block are presented in Section II, and Section III presents the measured results. The receiver can be used for multistandard multigigabit-per-second communication systems at the sum

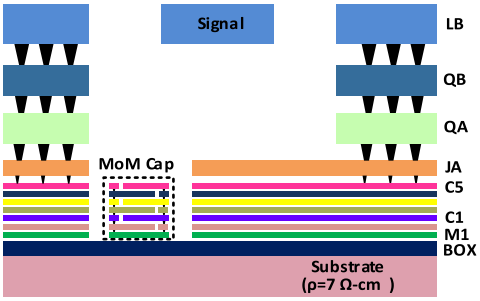


Fig. 3. Cross section of GF 22-nm CMOS FDSOI.

point of a wideband phased array or for the new generation of element-level digital beamforming arrays at 24–42 GHz (such as 6G systems).

II. Receiver Design

Fig. 1(a) shows the wideband I/Q receiver and is based on a standard I/Q mixer topology. A 20–45 GHz low noise variable-gain amplifier (LN-VGA) is first used with low NF. Next, a wideband double-balanced mixer is employed and downconverts the signal into baseband. The IF section includes low-pass filters (LPFs) and dc–6-GHz baseband amplifiers. The LO chain includes a wideband balun, which converts the single-end external LO into differential signal, a wideband all-pass I/Q network, and LO drivers. The output is a differential I/Q signal, which can be fed to a 90° combiner to suppress the image for IF SSB operation.

The I/Q receiver is implemented in the Global Foundries 22-nm fully depleted silicon on insulator (FD-SOI) process, which provides ten layers of copper and one aluminum top-layer, as shown in Fig. 3 [29], [30]. Because of the three thick metal (QA, QB, and LB) layers, transformers and baluns build in this stack-up can have high coupling coefficient and low loss. Due to the fully depleted characteristic, the BOX layer is quite thin (~20 nm), which enables the back gate control to save power for a low V_{dd} operation. Super-low threshold voltage transistors are used in this design due to their low $\mathrm{NF}_{\min}$ and high $f_t/f_{\max}$. The transistor provides 1×, 2×, and 3× gate pitch and 1× pitch size is chosen because 2× and 3× need a long narrow (0.1 μm) M1 trace to connect each finger, which results in a higher gate resistor and deteriorates the NF. The final transistor layout employs multiple vertical-gate finger connections to reduce the gate resistor to improve the transistor performance.

A. LN-VGA Design

The LN-VGA is a three-stage amplifier with current steering for gain control (see Fig. 4). The first stage is common-source (CS) stage with source degeneration for the lowest NF operation and the second stage is a cascode amplifier, which is used to implement the gain tuning. The third stage is a CS amplifier due to its lower output impedance. This makes it easier to realize wideband output matching. The effect of gain tuning on the LNA NF is reduced since the NF is dominated by the first stage. The cascade input third-order intercept point (IIP_3) can be written as

$$\frac{1}{\mathrm{IIP}_{3,\mathrm{LNA}}} = \frac{1}{\mathrm{IIP}_{3,1}} + \frac{G_1}{\mathrm{IIP}_{3,2}} + \frac{G_1 G_2}{\mathrm{IIP}_{3,3}} \quad (1)$$

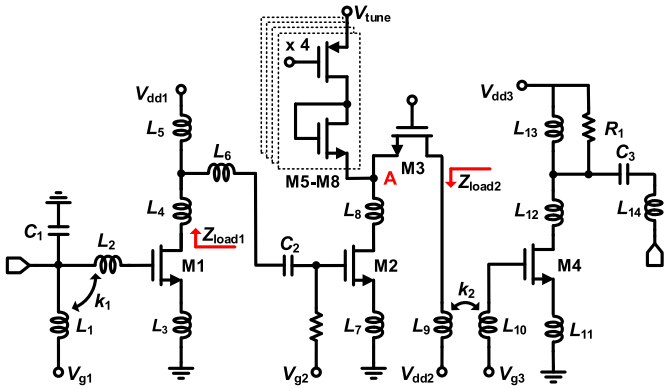


Fig. 4. Schematic of the three-stage LN-VGA.

TABLE I
LN-VGA COMPONENT VALUES

L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8	L_9	L_{10}
400 p	350 p	70 p	300 p	250 p	200 p	20 p	200 p	350 p	300 p
L_{11}	L_{12}	L_{13}	L_{14}	C_1	C_2	C_3	k_1	k_2	R_1
50 p	100 p	300 p	400 p	75 f	250 f	188 f	-0.2	0.55	100 Ω

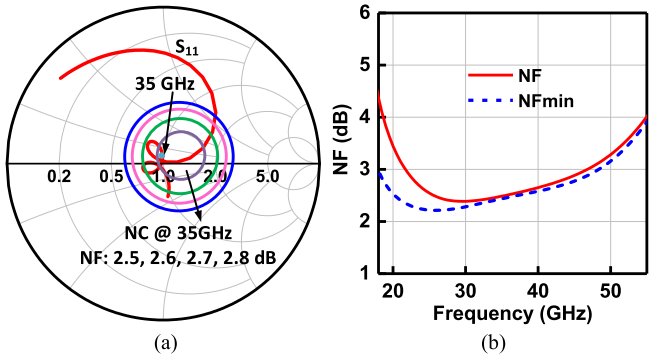


Fig. 5. (a) Simulated S_{11} and noise circle (35 GHz). (b) Simulated NF and NFmin.

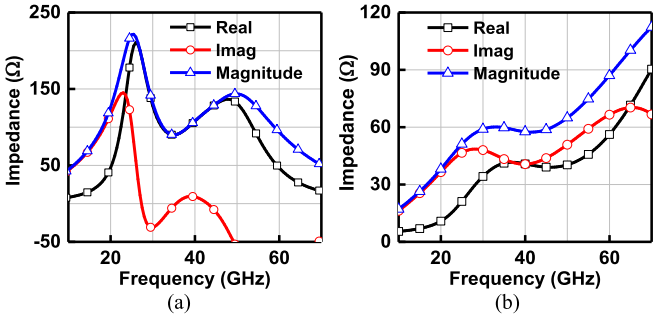


Fig. 6. Simulated (a) stage 1 load impedance (marked as Z_{load1}) and (b) stage 2 load impedance (marked as Z_{load2}).

where $IIP_{3,n}$ is the nth stage IIP_3. When G_2 is reduced, $IIP_{3,LNA}$ is improved if the LNA linearity is dominated by the third stage, which is typical in low-power designs. Also, since the gain tuning is realized at the second stage, the input and output matching are not affected by the gain variation and the wideband design can be maintained over a wide gain response.

The transistor width of M1–M3 is 48 μm and the width of M4 is 60 μm. The transistors are biased with a dc current of 5.4/7.7/6.7 mA, which has a current density of 0.1–0.15 mA/μm, and is around the NF_{min} bias point. In order to realize wideband input matching, a two-stage transformer-based matching network is used, which can generate two matching poles. The output matching is realized by a low Q inductor and a two-stage matching network. Since the previous two stages provide enough gain, the effect of low-Q load on the LNA NF is reduced. Also, in order to cover the whole 5G band, each stage is designed to peak at different frequencies. In order to maintain a wideband low-NF design, the noise matching is realized at high frequencies since the intrinsic transistor NF is very low at the lower band. This is done by sizing the first-stage CS transistor and adding the source degeneration inductor (L_3) for best performance at 35 GHz. Fig. 5(a) shows the simulated S_{11} and noise circle at 35 GHz with excellent impedance and noise matching simultaneously realized. The penalty of this approach is only 0.5 dB at 22 GHz, as shown in Fig. 5(b).

To maintain a low NF during gain tuning, the first stage needs provide a wideband gain response, and a network of three inductors is used at the M1 drain. This network is equivalent to a T-coil network, or a dual-pole transformer, exhibits a two-peak impedance profile, and provides high gain over a wide bandwidth. Fig. 6(a) shows the simulated first stage load impedance with peaks at 27 and 50 GHz. Also, two impedance peaks are desired for stage 2 to maintain the same transfer function shape as the gain is changed. This is done using a double-tuned transformer, which again results in a dual-impedance peak with separation controlled by the transformer coupling coefficient (k).

Fig. 6(b) shows the simulated second-stage load impedance with one peak at 30 GHz and the other one is at high frequency. Since the peaks of stages 1 and 2 compensate each other and stage 3 exhibit a wideband flat response due to the low Q load, the three-stage LNA realizes a flat gain response. V_{dd} of each stage is 0.8 V, which presents a problem for the cascode stage. Therefore, back gate control is applied to reduce V_{th} by ∼0.15 V and allow for 0.8-V operation. The final parameter values are listed in Table I.

Fig. 7 shows the simulated LN-VGA performance, where the load is 50 Ω. The peak gain is 24.2 dB with 3-dB bandwidth of 20.8–44.5 GHz at a dc power of 16 mW. The gain tuning range is ∼8 dB with 4-bit control. The simulated S_{11} and S_{22} are less than −10 dB at 22–48 GHz. At the high gain state, the NF is 2.4–3 dB at 22–44 GHz, and at the low-gain state, the NF becomes 3–3.7 dB. The IP1dB improves from −25 to −19 dBm between the high- and low-gain states, with a corresponding NF increase of only ∼0.8 dB. Since the OP1dB is limited by the last stage, the IP1dB improves with gain control and results in a higher dynamic range.

B. LO Driver and Mixer

After the LNA, a wideband passive balun converts the single-ended signal into a differential signal and feeds the I/Q mixer. The balun is implemented using QA and QB layers

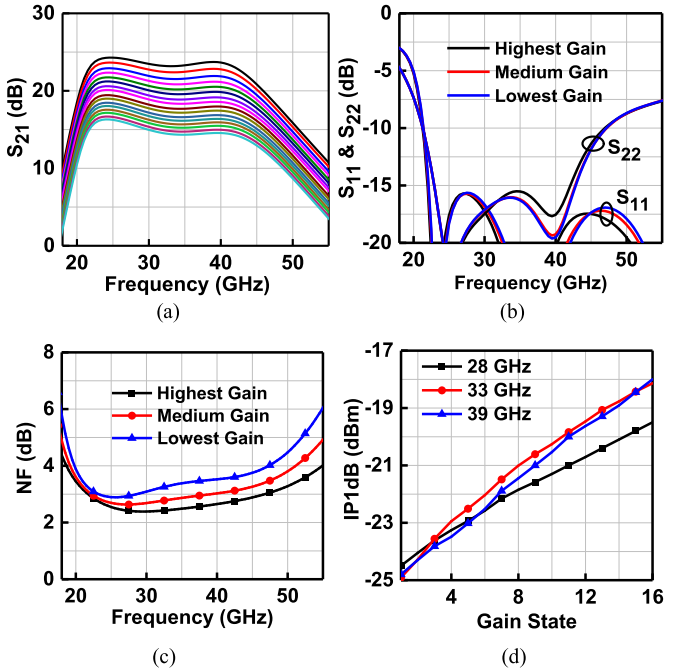


Fig. 7. Simulated LNA-VGA. (a) S_{21}. (b) S_{11} and S_{22}. (c) NF versus gain tuning. (d) IP1dB versus gain tuning.

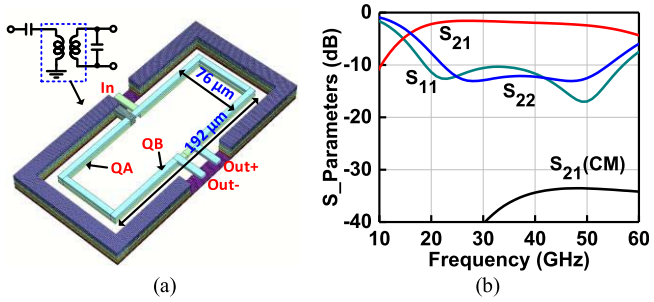


Fig. 8. Passive RF balun. (a) 3-D layout. (b) Simulation results.

as its primary and secondary coils with widths of 4 μm, as shown in Fig. 8(a). The core balun size is 76 μm $\times$ 192 μm. Then, capacitors are added to the primary and secondary stages to balance the amplitude and phase. The simulated balun insertion loss is <2.4 dB at 20–50 GHz and the common-mode rejection is >30 dB, as shown in Fig. 8(b).

The single-ended LO is provided externally and is fed to a passive balun first. The wideband passive balun is similar to the RF balun described above. The differential LO is then amplified, and in order to cover 20–50 GHz, an LO inverter-based amplifier is adopted due to its wideband characteristics, as shown in Fig. 9(a) [31]. However, due to the transistor gate and drain capacitors, the gain decreases at high frequencies. Also, the dominant pole is at the input node due to the Miller effect, which increases the input shunt capacitance by $\sim A_v C_{gd}$. In order to extend the LO driver bandwidth, a series inductor is added at the input node, which resonates out the input node capacitance [see Fig. 9(b)]. The LO driver gain is [32]

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{1}{1+s^2 L_1(C_{gsn}+C_{gsp})} \times \frac{1-R_f(g_{mn}+g_{mp})}{1+sR_f(C_{gdn}+C_{gdp})} \quad (2)$$

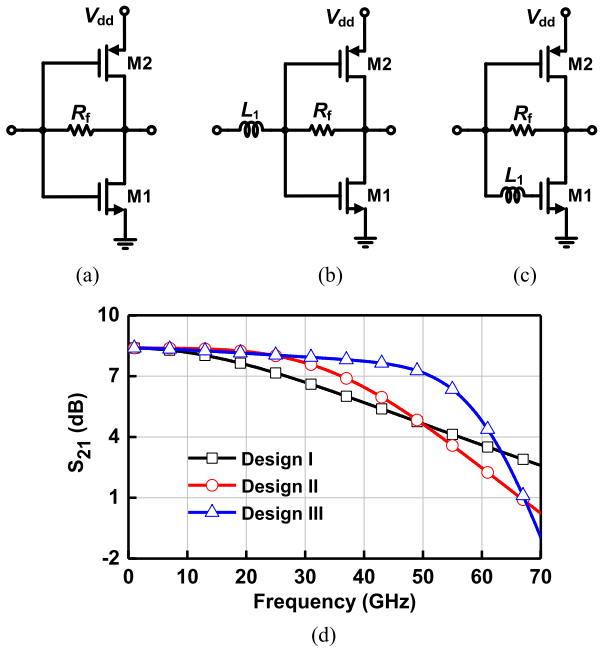


Fig. 9. (a)–(c) Designs I–III for the inverter amplifier structure. (d) Simulated gain with $R_f = 300\ \Omega$ and $L_1 = 300$ pH.

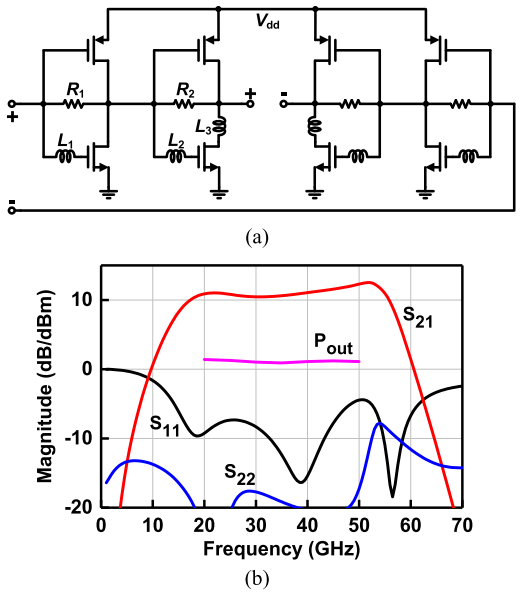


Fig. 10. (a) Schematic of the LO driver amplifier. (b) Simulated results of LO balun and driver amplifier together.

where g_m, C_{gs}, and C_{gd} are the transconductance, gate–source, and gate–drain capacitance of NMOS/PMOS, respectively. Another method to extend the bandwidth is to add an inductor at the NMOS or PMOS gate, as shown in Fig. 9(c), which also resonates out the parasitic capacitance.

Fig. 9(d) shows the simulated results of the three different inverter amplifiers. The original design shows a 1-dB bandwidth of 24 GHz. This is extended to 35 GHz with Design II and 48 GHz with Design III. The LO driver amplifier is built using Design III and is composed of two stages for added gain (see Fig. 10). The PMOS transistor size is chosen to be 1.4 times larger than the NMOS to balance g_m and result

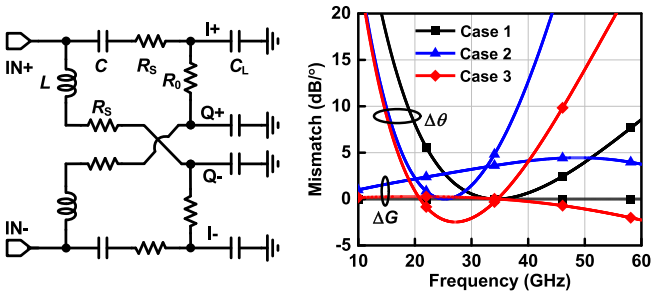


Fig. 11. (a) Schematic of traditional QAF. (b) Simulated amplitude and phase mismatch of the QAF for different cases.

in a voltage switch centered at $V_{dd}/2$. The simulated gain is 11.5 ±1 dB at 20–50 GHz with gain peaking at 52 GHz due to L_3 [see Fig. 10(b)]. Note that L_3 also improves the impedance match between the LO driver and QAF. With an input power of −9 dBm, the output power is ∼1 dBm at a dc power consumption of 22.6 mW.

The LO signal is then fed into a wideband differential I/Q generation network based on a QAF design [see Fig. 11(a)]. L and C resonate at ω_0 and the characteristic filter impedance is $Z_0 = (L/C)^{1/2} = R_0$, which results in a network Q of 1. The transfer function is

$$\begin{bmatrix} V_{I\pm} \\ V_{Q\pm} \end{bmatrix} = V_{\text{in}} \begin{bmatrix} \mp\dfrac{\omega^2+\omega_0^2-\frac{2\omega_0}{Q}j\omega}{-\omega^2+\omega_0^2+\frac{2\omega_0}{Q}j\omega} \\ \pm\dfrac{\omega^2+\omega_0^2+\frac{2\omega_0}{Q}j\omega}{-\omega^2+\omega_0^2+\frac{2\omega_0}{Q}j\omega} \end{bmatrix}. \tag{3}$$

Based on (4), $|V_{I\pm}| = |V_{Q\pm}|$ is realized at any ω with orthogonal phase splitting at $\omega = \omega_0$ and $Q = 1$. The two network poles can also be split by using a lower network Q. An issue of this QAF is that I/Q errors are sensitive to the load capacitance (C_L), arising from the mixer gate capacitance [33]. In order to mitigate the effect of C_L, a low-Q network with a series R_s is employed at the expense of higher loss [34]. Fig. 11(b) shows the simulated phase and gain mismatch for three cases: $C_L = 0$ and $R_s = 0$, $C_L = 40$ fF and $R_s = 0$, and $C_L = 40$ fF and $R_s = 50\ \Omega$. It is seen that when $C_L = 0$ and $R_s = 0$ (case 1) and $\omega_0 = 35$ GHz, there is no amplitude mismatch and the phase mismatch is <5° at 22.6–52.7 GHz. When $C_L = 40$ fF and $R_s = 0$ (case 2), ω_0 shifts to 25.3 GHz, and the gain mismatch becomes 2–4.4 dB at 20–50 GHz with a phase mismatch of <5° at 17.7–34.2 GHz. Therefore, C_L decreases the bandwidth and also increases the gain/phase mismatch. By adding R_s, the gain mismatch is reduced to 1 dB and the phase mismatch is <5° at 17–41.3 GHz. However, the voltage gain is reduced by ∼3 dB due to R_s.

In order to improve the QAF loss, a series inductive compensation network (L_1 and L_2) is used instead of R_s [see Fig. 12(a)]. By adding an inductor before the vector modulator loading capacitor, voltage peaking occurs at the load. Also, the added LC network provides the freedom to adjust the impedance seen by the core QAF, thus reducing its load sensitivity. For comparison, a two-stage Type-I constant-phase PPF is simulated with the first stage pole at 25 GHz

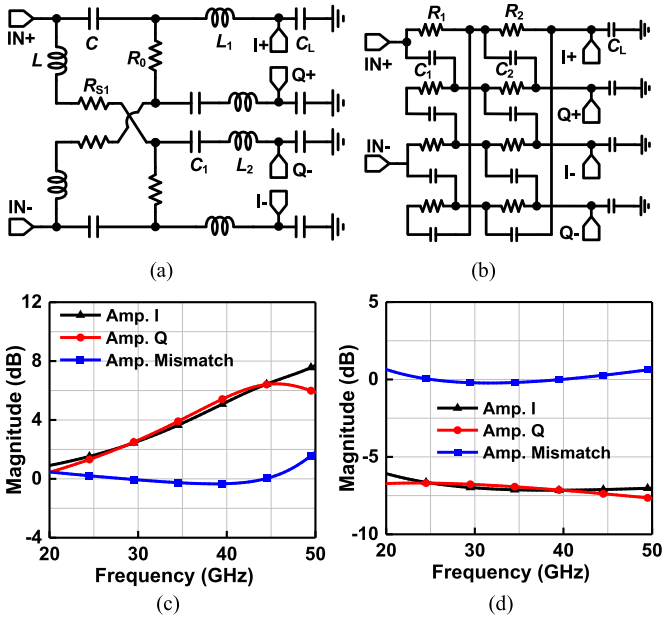


Fig. 12. Schematic of (a) modified QAF and (b) two-stage Type-I PPF. Simulated I/Q amplitude and mismatch of (c) modified QAF and (d) polyphaser filter.

($R_1 = 50\ \Omega$ and $C_1 = 127$ fF) and the second stage pole at 40 GHz ($R_2 = 50\ \Omega$ and $C_2 = 80$ fF) (see Fig. 12). The load C_L is 40 fF. The QAF and the two-stage polyphase networks are simulated in schematic mode and both realize a low amplitude mismatch (<0.5 dB). However, the PPF has a voltage gain of −7 dB, while the improved QAF has an average gain of 3 dB and results in a 10-dB voltage gain difference [see Fig. 12(c) and (d)].

Fig. 13(a) shows the QAF layout after full EM effects are taken into account with a size of 240 μm × 410 μm. The QAF gain is simulated together with the LO balun and driver with the mixer as the load since the balun also introduces a bit of mismatch versus frequency [see Fig. 13(b)]. The simulated LO network composed of the LO balun, driver, and I/Q network shows a voltage gain (differential to differential) of 10–15 dB at 20–55 GHz, with an amplitude mismatch <0.6 dB and a phase mismatch <5°. The differential-mode-to-common-mode voltage swing ratio at QAF output is larger than 26 dB.

Low-IF or direct conversion receivers employ passive mixers due to their low $1/f$ noise. However, passive mixers require rail-to-rail swings at the transistor gates, which greatly increases the power consumption. Also, 25% duty cycle LO is required to avoid LO overlap for the I/Q mixer, which also increases the design complexity. Therefore, an active mixer is used in this design and can be used as follows: 1) at an IF of 1–7 GHz, the I/Q mixer can be configured to become an SSB mixer using an external hybrid and the $1/f$ noise is therefore of no issue and 2) the mixer can also be used as a direct I/Q mixer provided that the $1/f$ noise at the cyclic prefix of 50 kHz in 5G OFDM waveforms does not cause system-level degradations.

Fig. 14(a) shows the double-balanced I/Q downconversion mixer. A resistor load (R_2) is used due to a relatively low IF of dc–6 GHz. Degeneration resistors (R_1) are added in the g_m

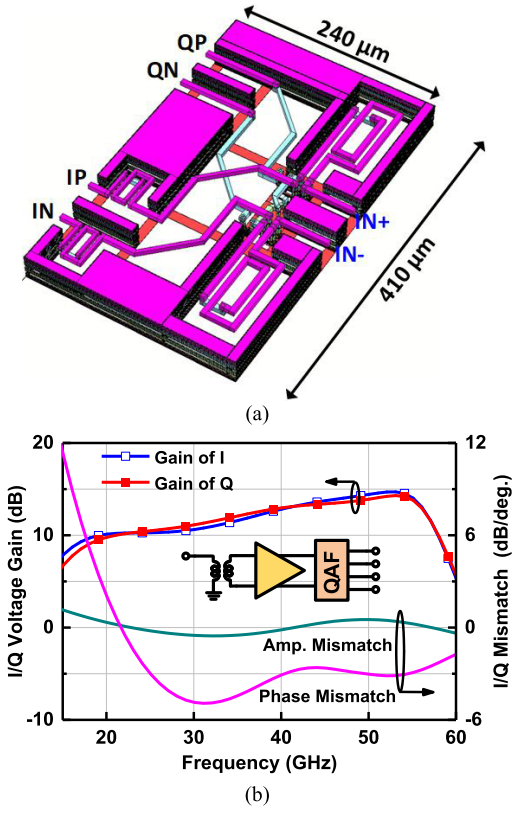


Fig. 13. (a) 3-D layout of the revised QAF. (b) Simulated I/Q voltage gain and amplitude and phase mismatch for the entire LO chain.

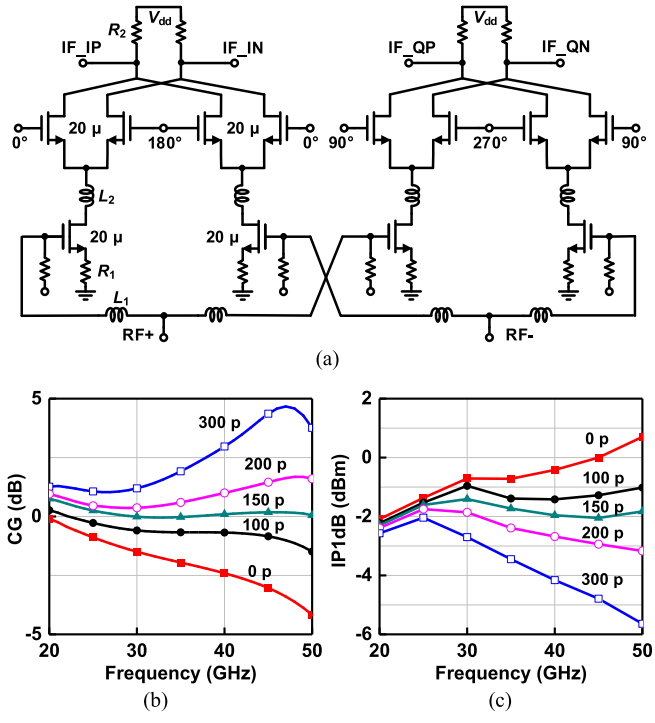


Fig. 14. (a) Schematic of the double-balanced I/Q downconversion mixer. (b) Simulated CG versus L_2. (c) Simulated IP1dB versus L_2.

stage to improve the linearity and improve the input matching. Also, series inductors L_2 are inserted between the g_m stage and the switching quad. The inductors resonate out the parasitic

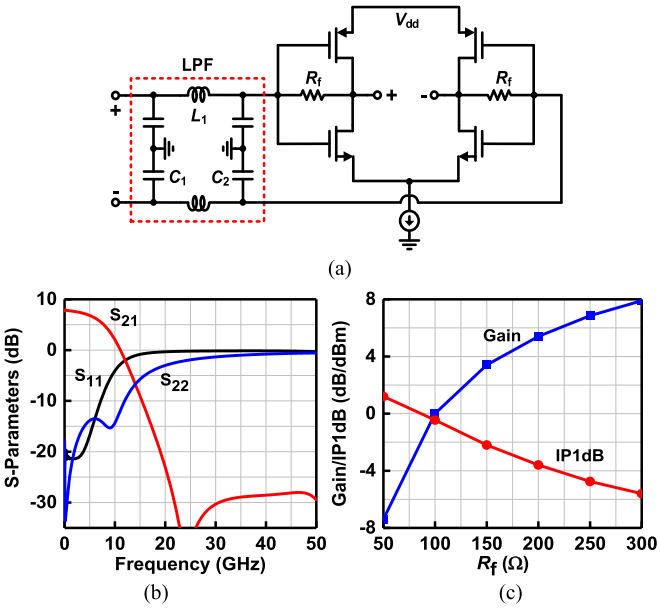


Fig. 15. (a) Schematic of LPF and IF amplifier. (b) Simulated S-parameters using full-EM modeling of the LPF. (c) Simulated gain and IP1dB versus R_f.

capacitance of the gm-stage and improve the mixer conversion gain (CG) and noise performance [35]. In this design, 20-μm width is used for the switching quad transistors for best compromise between LO drive power and load capacitance.

Fig. 14(b) and (c) shows the simulated CG and IP1dB versus L_2, with an IF fixed at 2 GHz. This simulation includes the LO chain (LO balun, LO driver, and IQ generation) with $P_{\mathrm{LO}} = -9$ dBm and RF balun. It is observed that without L_2, the CG drops versus frequency. However, with a large L_2, the IP1dB decreases especially at high frequencies. Taking CG and IP1dB into consideration, $L_2 = 150$ pH is chosen for best performance. The IQ double-balanced mixer consumes 27 mW of dc power.

C. LPF and IF Amplifier

A differential LPF is employed after the mixer to suppress the unwanted high-frequency tones and to create a band-limited signal response. A third-order Chebyshev design is used with a corner frequency of 6 GHz [see Fig. 15(a)]. This is followed by an IF amplifier based on a single-stage inverter with its gain determined by the tail current and feedback resistor (R_f). Since the LPF and the IF amplifier are directly connected to the mixer, the IF amplifier input impedance affects the mixer CG. A large R_f results in a higher gain, narrower bandwidth, and larger input impedance, which will be beneficial to the mixer. However, a large R_f also decreases the IP1dB and limits the mixer linearity. Taking all of these into consideration, $R_f = 300\ \Omega$ is chosen, and the amplifier input impedance is calculated as

$$Z_{\mathrm{in}} = \frac{R_f + R_L}{1 + (g_{mp} + g_{mn})R_L}. \tag{4}$$

With a total g_m of 0.04 S, the input impedance is to be 116 Ω. Thus, a mixer load resistor of 120 Ω is chosen to result in an LPF design with ~120-Ω load at both of its ports.

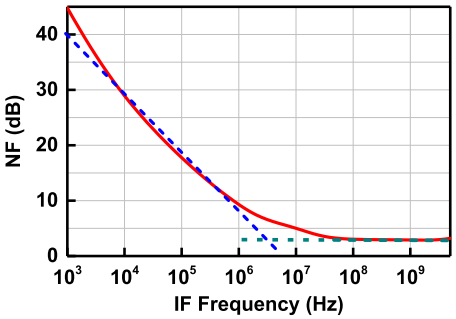


Fig. 16. Simulated output noise profile with a $1/f$ corner frequency of 5 MHz.

Note that the ac coupling capacitor between the IF amp and mixer has been removed to allow for dc–6-GHz operation. Thus, the dc level at the mixer output and the dc level of IF amplifier input must be the same, and this is realized by sizing the IF amplifier PMOS and NMOS transistors to provide the required bias voltage at the input node (attached to the mixer).

The LPF lumped element values are calculated as

$$C_1 = \frac{g_1}{R_0\omega_c} \quad C_2 = \frac{g_3}{R_0\omega_c} \tag{5}$$

$$L_1 = \frac{R_0 g_2}{\omega_c} \tag{6}$$

where g_1, g_2, and g_3 are the low-pass prototype elements, R_0 is the system impedance (120 Ω), and ω_c is the cutoff frequency of 6 GHz. C_1 and C_2 and L_1 are then determined to be 120 fF and 3 nH, respectively. Finally, the 3-nH inductor is realized by routing at LB/QB/QA layer with a compact size of 60 × 60 μm^2. The LPF insertion loss is <0.9 dB.

Fig. 15(b) shows the simulated LPF and IF amplifier combined response. The peak power gain is 7.9 dB with 1-/3-dB bandwidth of 5.1/8.1 GHz and a dc power consumption of 13.6 mW from a 0.8-V supply. The high power consumption is due to the required linearity of the output stage, and the simulated IP1dB and OP1dB are −5.5 and 1.4 dBm, respectively [see Fig. 11(c)]. S_{21} is less than −25 dB at >21 GHz, which means that the LO leakage at the IF port is suppressed by at least 25 dB. The 22FDX process results in very low NF in the dc–6-GHz range and the simulated NF for the LPF + IF amplifier is 3.8 dB, including the LPF loss.

The simulated receiver peak differential gain is 26 dB with 3-dB bandwidth of 21–44 GHz. The IP1dB is approximately −28 dBm for a power consumption of 102 mW from a 0.8- and 1.6-V supply. The linearity is mainly limited by the LN-VGA and the double-balanced mixer. This means that the receiver linearity can be improved with additional RF-VGA control. The simulated flicker noise corner frequency is ∼5 MHz, which is expected in this technology (see Fig. 16). The LO leakage at 21–44 GHz is very low at the IF ports due to the symmetric double-balanced mixer layout and the IF LPF/amplifier with an additional rejection of >25 dB at 20–44 GHz.

III. Measurements

Fig. 17 shows the micro-photograph of the 22FDX I/Q receiver chip. The chip core area is 1.8 mm × 0.5 mm.

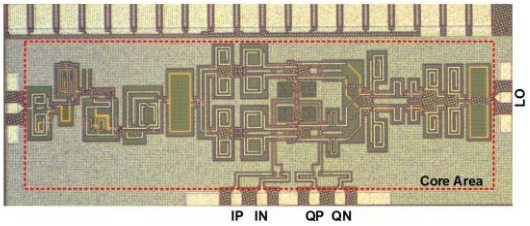


Fig. 17. Microphotograph of the fabricated IQ receiver chip with core size of 1.8 × 0.5 mm^2.

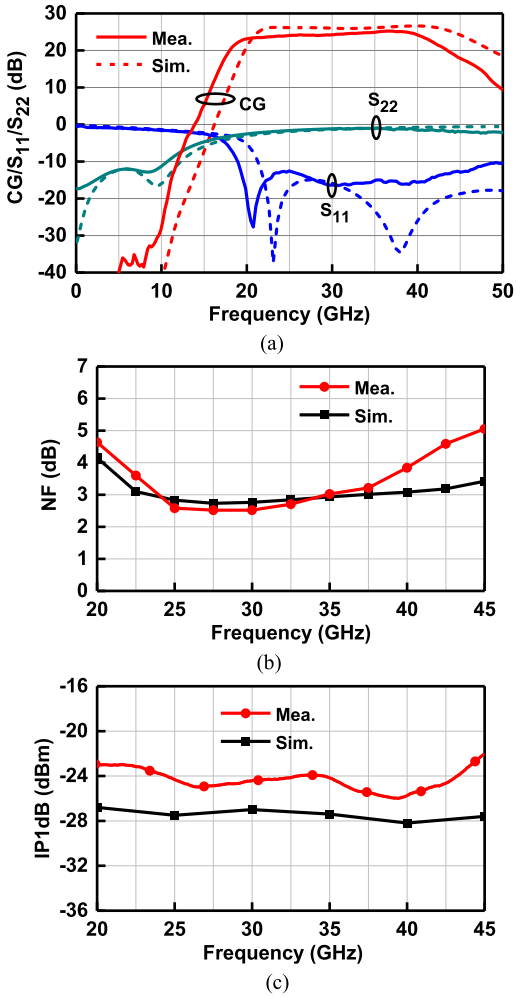


Fig. 18. Measured and simulated (a) CG and input–output matching, (b) NF, and (c) IP1dB.

All measurements, including NF and linearity, were performed using on-chip probing, a Keysight N5247B network analyzer (PNA-X), and a Keysight E8267D signal generator. When biased, the power consumption is 102 mW as predicted.

Fig. 18(a) shows the measured CG and input–output matching. The RF and LO are sliding together to result in a fixed IF of 2 GHz. The measured channel peak CG is 25.3 dB with 3-dB bandwidth of 19.5–42 GHz, which covers the whole mm-wave 5G band. S_{11} is less than −10 dB at 19–50 GHz and S_{22} is less than −10 dB at dc–10 GHz.

The measured NF is 2.7–5 dB at 20–44 GHz and 2.7–4.2 dB at 22–42 GHz [see Fig. 18(b)]. The NF degradation at

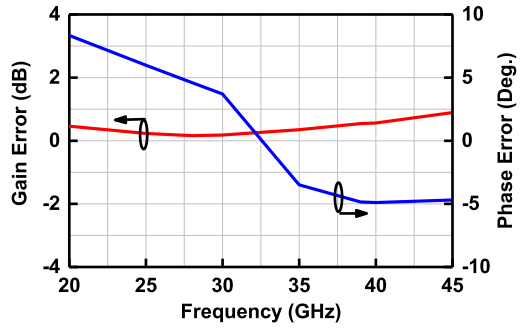


Fig. 19. Measured gain and phase error between I and Q.

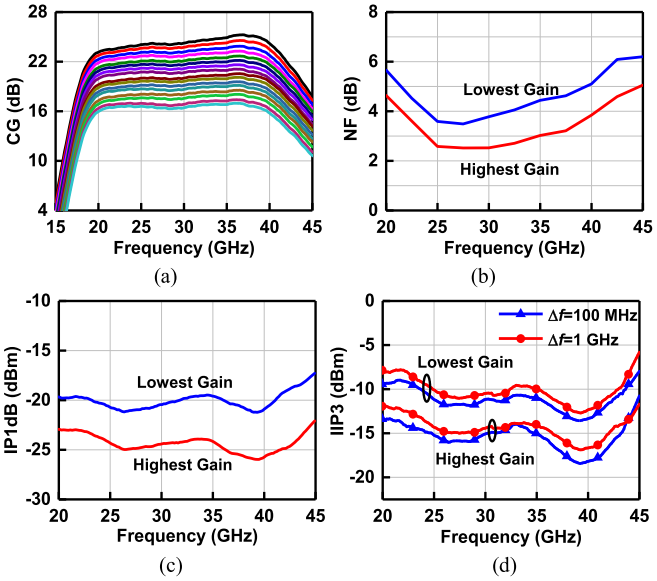


Fig. 20. Measured (a) CG, (b) NF, (c) IP1dB, and (d) IIP_3 versus gain tuning.

40–45 GHz can be observed and is due to the LNA gain shift to lower frequencies, which results in gain drop at 40–45 GHz. The measured IP1dB is −26 to −23 dBm at 20–45 GHz with an IIP_3 of −15 dBm, both measured with $\Delta f = 0.1-1$ GHz [see Fig. 18(c)].

Fig. 19 shows the measured CG error and phase error between the I and Q channels (IF = 2 GHz). The gain error is <1 dB at 20–45 GHz and specifically <0.3 dB at 26–30 GHz and <0.6 dB at 37–41 GHz. The measured phase error is <5° at 25–42 GHz. If the I and Q outputs are fed directly to analog-to-digital converters (ADCs), then this can be easily corrected using digital signal processing. If this is fed to an IF hybrid, then ±1-dB gain control is easily achieved in the IF amplifiers (DAC current control). In this case, the image rejection ratio will have a worst case value of 27 dB at 25–45 GHz if no phase shift correction is done at the IF. The phase mismatch can be corrected at the IF or baseband using digital processing.

Fig. 20 shows the measured CG, NF, IP1dB, and IIP_3 versus gain control. By using current steering in the LN-VGA, the receiver CG can be controlled by 7–9 dB at 20–42 GHz. The tuning gain step is within ±0.15 dB of the simulated LN-VGA steps and is due to process variation between M3 and M5–M8 [see Fig. 4(a)]. At the lowest gain state, the NF

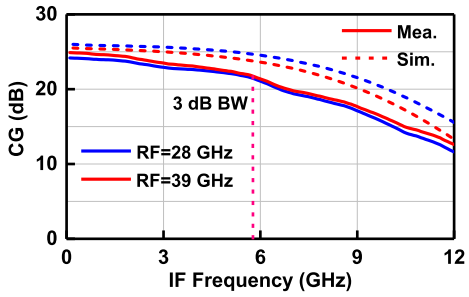


Fig. 21. Measured and simulated CG versus IF frequency.

TABLE II
COMPARISON WITH WIDEBAND IQ RECEIVERS

Ref.	**This Work**	EuMIC 2016 [17]	IMS 2018 [19]	JSSC 2020 [21]	TMTT 2020 [23]
Tech.	**22-nm SOI**	0.13-μm SiGe	0.12-μm SiGe	45-nm SOI	65-nm CMOS
f_0 (GHz)	**31**	35	25	34	28
RF BW(GHz)	**19.5-42**	25-45	10-40	24-44	26.5-32.5
Peak CG (dB)	**25.3**	21	36	35.2	29.5
NF (dB)	**2.7-4.2**	5-7	6.8-9.5	3.2-6.1	5.3
IP1dB (dBm)	**-26 to -23**	-26 to -20	-27	-27 to -25	-28
LO	**Ex. SE**	Ex. SE	Ex. SE	Ex. Diff	Ex. SE
Pdc (mW)	**102**	N.A.	273	60**	33*
Size (mm^2)	**0.9**	2.5	N.A	0.76	0.65

*LO driver power is not given and is not included.

** DC power is not correct with gain of 35 dB, IP1dB of -25 dBm resulting in an OP1dB of 9 dBm at 1-6 GHz.

increases by 1.2 dB as expected, and the IP1dB increases by 5.2 dB. As expected, the dynamic range increases with lower receiver gain.

Fig. 21 shows the measured results when the LO is fixed, while RF is changed. The measured IF 3-dB bandwidth is 5.7 GHz for the I and Q channels.

Table II compares the wideband IQ receiver with start-of-the-art I/Q receivers. The 22FDX design realizes a wide bandwidth, very low NF, and excellent linearity. Of importance is the achieved spurious-free dynamic range (SFDR) of 50 dB at 24–42 GHz for a 100-MHz waveform and for 100 mW of dc power consumption. The SFDR is calculated based on the following equation and $SNR_{o,min} = 0$ dB is assumed

$$\text{SFDR(dB)} = \frac{2}{3}(\text{IIP}_3 - N_{\text{RX}}) - \text{SNR}_{o,\text{min}} \quad (7)$$

$$= \frac{2}{3}(\text{IIP}_3 - \text{KTBNF}) - \text{SNR}_{o,\text{min}}. \quad (8)$$

This is excellent for element-level digital beamforming systems requiring downconverters on every antenna in the large mm-wave array.

IV. CONCLUSION

This article presented a 24–42-GHz IQ receiver for the mm-wave 5G band. A three-stage wideband LN-VGA is used

to ensure a low NF, and a modified LO QAF network is used to generate a wideband low-mismatch IQ signal for the double-balanced mixers. Efforts are done to result in a low-power wideband mm-wave receiver, including the use of LO and IF amplifiers based on inverters. Future work will include much more programmability in the chip, such as additional gain control in the I/Q baseband amplifiers and a programmable LPF. Also, the LO quadrature generation section can be made better by using two different quadrature networks and a switch, followed by a wideband driver, and without additional power consumption. The current results indicate that a low noise, high linearity I/Q receiver can be built at only 102 mW of dc power consumption and is suitable as either a single receiver at the common RF point or for element-level digital beamforming systems in 5G and 6G communication systems.

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