ANKIT**JAIN**

Micro- and Nanosystems MSc. Programme, ETH Zurich

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interests

Microfluidics
MEMS Design & Fabrication
FPGA Design & Verification

education

ETH Zurich, CH
M.Sc. (Ongoing)
Micro- and Nanosystems

IIIT-Allahabad, INDIA
B. TECH. (Jun, 2013)
Electronics and Communication Eng.
CGPA: 9.35/10

K V No.2 GCF Jabalpur, INDIA
12th Grade (May, 2009)
Percentage: 95%

K V No.2 GCF Jabalpur, INDIA
10th Grade (May, 2007)
Percentage: 92.4%

skills

Programming
Matlab
C/C++
Verilog HDL

Platforms
Windows
Linux

Software
Comsol Multiphysics
AutoCAD
Cadence Allegro
Debussy
Xilinx ISE Design Suite
NI LabVIEW

industrial**experience**

Hardware Engineer, Juniper Networks (Aug, 2013 – Aug, 2015)

- Undertook ownership of high quality hardware from concept to production.
- Designed and verified the control path FPGA.
- Designed and tested high speed PCBs.
- Worked with PCB layout, Mechanical, Software, Testing and Manufacturing teams.

Application Engineer Intern, National Instruments (Jun – Jul, 2012)

- Undertook a project on PXI systems.
- Learned LabVIEW and signal processing on FPGA.

pro**jects**

Microfluidics

Microfluidic platform for the large-scale screening of C. elegans
Prof. Andrew deMello, ETH Zurich (April – July, 2016)
Developed an automated platform for the screening of *C. elegans*. The platform, consisting of the microfluidic chip and custom control software, was able to process on average 8 worms per minute and a total of 400 worms in an experiment. Worms were loaded using a pressure based delivery system and an on-chip trap system consisting of two hydraulic valves positioned next to or on top of the microfluidic channel. Both the worm loading and trapping was controlled by an image based LabVIEW algorithm.

MEMS design/fabrication

Fabrication and Characterization of MEMS acoustic sensors
Prof. Christofer Hierold, ETH Zurich (Feb – Aug, 2016)
Aided in the development of coupled mass based MEMS acoustic sensors. The tasks included design of test structures, etching (RIE) of devices, imaging using SEM, and characterization via Laser Doppler Vibrometer.

Fabrication and Characterization of a MEMS Accelerometer
Embedded MEMS Lab (Practical Course), ETH Zurich (Oct – Nov, 2015)

Design of a 2-D Micromirror Structure
Prof. B. R. Singh, IIITA (July – Nov, 2012)
Designed and simulated a micromirror structure in Comsol Multiphysics. The mirror was based on electrothermal actuation and designed to provide a smooth, large and stable angular movement in a 2-D plane for optical coherence tomography(OCT). The layout was designed in L-Edit and after defining a process definition, a 3-D model was generated.

Board design/verification

Design of 4X100GE CXP Optics based Physical Interface Card
Juniper Networks, Bangalore (Sep, 2013- Feb, 2015)
Designed and tested a high-speed PCB that housed four 100GE optical interface, Regenerative repeaters, a control path FPGA and associated clocking, power and miscellaneous control devices.

relevant**courses**

Biomicrofluidics
Embedded MEMS Lab
Microsystem Technology
Nanosystems
Nano-Optics
Nanorobotics
Devices and Systems
Biosensors and Bioelectronics
Embedded System Design
VLSI Design
Semiconductor Devices
Digital Electronics
Computer Organization
Microprocessor Programming
Digital Signal Processing
Signals and Systems
Digital and Analog Communication
Antenna and Wave Propagation
Radio Frequency and Microwave
Electromagnetic Fields and Waves

Qualification of 48 Port 10 GE Interface test module

Juniper Networks, Bangalore (Apr- Jun, 2013)

Tested PCB which was used for validating various types of interfaces like 10GE, I2C, SGMII, PCIe and MDIO. The board housed regenerative repeaters for looping back 10GE traffic, control path CPLD and various power loads.

FPGA design/verification

Implementation of a JPEG encoder

Dr. Neteesh Purohit, IIITA (Jan-May, 2012)

Developed a fast and efficient architecture for JPEG and implemented it on a Vertex 5 FPGA. It consists of 2-D discrete cosine transform (DCT), quantization and entropy encoding blocks. It has a 2-Stage pipeline. The DCT and quantization block has been implemented without using any hardware multiplier. The Run-length and Huffman encoding block has been combined for delay reduction and are triggered at positive and negative clock cycles respectively.

Simultaneous Generation of arbitrary waveforms across 32 Analog Channels in a PXI system

National Instrument, Bangalore (Jun-Jul, 2012)

The PXI system had four 7831R reconfigurable PXI modules each having 8 analog output channels and a Vertex 5 FPGA. The data was read simultaneously by four FPGAs using Direct Memory Access(DMA) lines and outputted synchronously at a rate of 1Msamples/s using hardware and software triggers. The FPGAs were programmed using LabVIEW FPGA tool.

notable**achievements**

- Awarded, Academic Excellence award for securing 2nd rank in ECE Department in 1st Semester, 2010.
- Awarded, “President Award” by President of India in ‘Scouting’, 2007.
- Successfully organized a photography event and an Electronics Quiz (EC Marathon) during the cultural festival at IIITA, 2012.
- Successfully lead groups of upto 10 people for trekking around Bangalore while working as a Trek Leader with Bangalore Hikers, 2014.