

AnkitJain

contact

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interests

Microfluidics
MEMS Design & Fabrication
FPGA Design & Verification

education

ETH Zurich, CH

M.Sc.

Sept, 2015 - ongoing

Micro- and Nanosystems

IIIT Allahabad, INDIA

Bachelor of technology

Aug, 2009 - Jun, 2013

Electronics and Communication

9.35/10

Kendriya Vidyalaya No.2 GCF

Grade 12th

July, 2008 - May, 2009

95%

skills

Programming

Matlab
LabVIEW
C/C++
Verilog HDL

Software

Comsol Multiphysics
AutoCAD
Cadence Allegro
Debussy

industrial experience

Juniper Networks

Hardware Engineer

Aug, 2013 – Aug, 2015

- Ownership of high quality hardware from concept to production.
- Design and verification of control path FPGA.
- Design and testing of high speed PCBs.
- Collaboration with PCB layout, Mechanical, Software, Testing and Manufacturing teams.

National Instruments

Application Engineer Intern

Jun, 2009 – Jul, 2009

- Design and verification of FPGA on PXI systems.
- Real-time signal processing using LabVIEW.

projects

Microfluidics

On-demand digital barcodes in droplets

Prof. Andrew deMello, ETH Zurich

Mar, 2017 – Ongoing

Design and characterization of a novel digital barcoding system that uses combination of differently colored beads (fluorescent dyes) to create unique codes. The system consists of on-demand generation of 8µm sized droplets of polymer solution, their photo-polymerization and subsequent encapsulation inside a mother droplet via electric field in a microfluidic chip.

Microfluidic platform for the large-scale screening of *C. elegans*

Prof. Andrew deMello, ETH Zurich

Apr, 2016 – Jul, 2016

Developed an automated platform for the screening of *C. elegans*. The platform, consisting of the microfluidic chip and custom control software, was able to process on average 8 worms per minute and a total of 400 worms in an experiment. Worms were loaded using a pressure based delivery system and an on-chip trap system consisting of two hydraulic valves positioned next to or on top of the microfluidic channel. Both the worm loading and trapping was controlled by an image based LabVIEW algorithm.

MEMS design & fabrication

Fabrication and characterization of MEMS acoustic sensors

Prof. Christofer Hierold, ETH Zurich

Feb, 2016 – Aug, 2016

Aided in the development of coupled mass based MEMS acoustic sensors. The tasks included design of test structures, etching (RIE) of devices, imaging using SEM, and characterization via Laser Doppler Vibrometer.

Design of a 2-D micromirror structure

Prof. B. R. Singh, IIT A

July, 2012 – Nov, 2012

Designed and simulated a micromirror structure in Comsol Multiphysics. The mirror was based on electrothermal actuation and designed to provide a smooth, large and stable angular movement in a 2-D plane for optical coherence tomography (OCT). The layout was designed in L-Edit and after defining a process definition, a 3-D model was generated.

Fabrication and characterization of a MEMS accelerometer

Embedded MEMS Lab (Practical Course), ETH Zurich

Oct, 2015 – Nov, 2015

Board design & verification

Design of 4X100GE CXP optics based physical interface card

Juniper Networks, Bangalore

Sep, 2013 – Jul, 2015

Designed and tested a high-speed PCB that housed four 100GE optical interface, Regenerative repeaters, a control path FPGA and associated clocking, power and miscellaneous control devices.

relevant courses

Biomicrofluidics
Embedded MEMS Lab
Microsystem Technology
Nanosystems
Nano-Optics
Nanorobotics
Devices and Systems
Biosensors and Bioelectronics
Embedded System Design
VLSI Design
Semiconductor Devices
Digital Electronics
Computer Organization
Microprocessor Programming
Digital Signal Processing
Signals and Systems
Digital and Analog
Communication
Antenna and Wave Propagation
Radio Frequency and Microwave
EM Fields and Waves

Qualification of 48 port 10 GE interface test module

Juniper Networks, Bangalore

Apr, 2013 – Jun, 2013

Tested PCB which was used for validating various types of interfaces like 10GE, I2C, SGMII, PCIe and MDIO. The board housed regenerative repeaters for looping back 10GE traffic, control path CPLD and various power loads.

FPGA design & verification

Implementation of a JPEG encoder

Dr. Neteesh Purohit, IIITA

Jan, 2012 – May, 2012

Developed a fast and efficient architecture for JPEG and implemented it on a Vertex 5 FPGA. It consists of 2-D discrete cosine transform (DCT), quantization and entropy encoding blocks. It has a 2-Stage pipeline. The DCT and quantization block has been implemented without using any hardware multiplier. The Run-length and Huffman encoding block has been combined for delay reduction and are triggered at positive and negative clock cycles respectively.

Simultaneous generation of arbitrary waveforms across 32 analog channels in a PXI system

National Instrument, Bangalore

Jun, 2012 – Jul, 2012

The PXI system had four 7831R reconfigurable PXI modules each having 8 analog output channels and a Vertex 5 FPGA. The data was read simultaneously by four FPGAs using Direct Memory Access(DMA) lines and outputted synchronously at a rate of 1Msamples/s using hardware and software triggers. The FPGAs were programmed using LabVIEW FPGA tool.

notable achievements

- Awarded, Academic Excellence award for securing 2nd rank in ECE Department in 1st Semester, 2010.
- Awarded, "President Award" by the President of India in 'Boy Scouting', 2007.
- Successfully organized a photography event and an Electronics Quiz (EC Marathon) during the cultural festival at IIITA, 2012.
- Successfully led groups of upto 10 people for trekking around Bangalore while working as a Trek Leader with Bangalore Hikers, 2014.

references

Prof. Dr. Andrew deMello

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Umar K Badusha

Hardware Engineering Sr. Manager, Juniper Networks, Bangalore, IN
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