**1. A memory and cache subsystem uses byte-addressing。。。**

【答案:】

32-bit **0x**22339abmemory address of following table contains 3 parts:

Tag，Index, Byte-Offset 0x22339ab= 0000 0010 0010 0011 0011 1001 1010 1011

16 13 3 0000 0010 0010 0011-0,011 1,001 1,010 1-011

13 13 6 0000 0010 0010 0-0,11 00,11 10,01 10-10 1011

14 15 3 0000 0010 0010 00-11 0,011 1,001 1,010 1-011

15 12 5 0000 0010 0010 001-1 001,1 100,1 101-0 1011

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Cache feature** | **Index value(Hex)** | **Index size, bits** | **TAG size, bits** | **Tatal Size,KB** |
| 64KB cache data,Direct-mapped,  8 bytes/block | 0x0735 | 13 | 16 | 8k\*(1+16)/8+64KB=81KB |
| 512KB cache data, Direct-mapped,  64 bytes/block | 0xce6 | 13 | 13 | 8K\*(1+13)/8+512KB=526KB |
| 512KB cache data, 2-Way set associative  8 bytes/block | 0x6735 | 15 | 14 | 64K\*(1+14)/8+512KB=632KB |
| 1024KB cache data, 8-Way set associative  32 bytes/block | 0x9cd | 12 | 15 | 32k\*(1+15)/8+1024KB=1088KB |

**2． A computer with multi-cycle CPU runs at 5 GHz 。。。。**

【答案:】

(1).Total Clock cycles of 1200 accesses in Part-A is (A) **1200**  ;

(2).Total Clock cycles of 40 accesses in Part-B is (B) **40\*(1+25)=1040** , these 40 accesses need more Clock cycles than 40 accesses in perfect cache mode, the increased cycle number is noted as J, value of J is (C) **40\*25=1000** .

(3).Total Clock cycles of 10 accesses in Part-C is (D) **10\*(1+25+400) =4260**  , these 10 accesses need more Clock cycles than 10 accesses in perfect cache mode, the increased cycle number is noted as K, value of K is (E) **10\*(25+400) =4250** .

(4).Average CPI of TP run in not perfect cache mode is noted as L, L may be written as an arithmetic expression about I,J and K, please fill following blank with such an arithmetic expression:

L= (F) **(4.2\*I+J+K)/I**