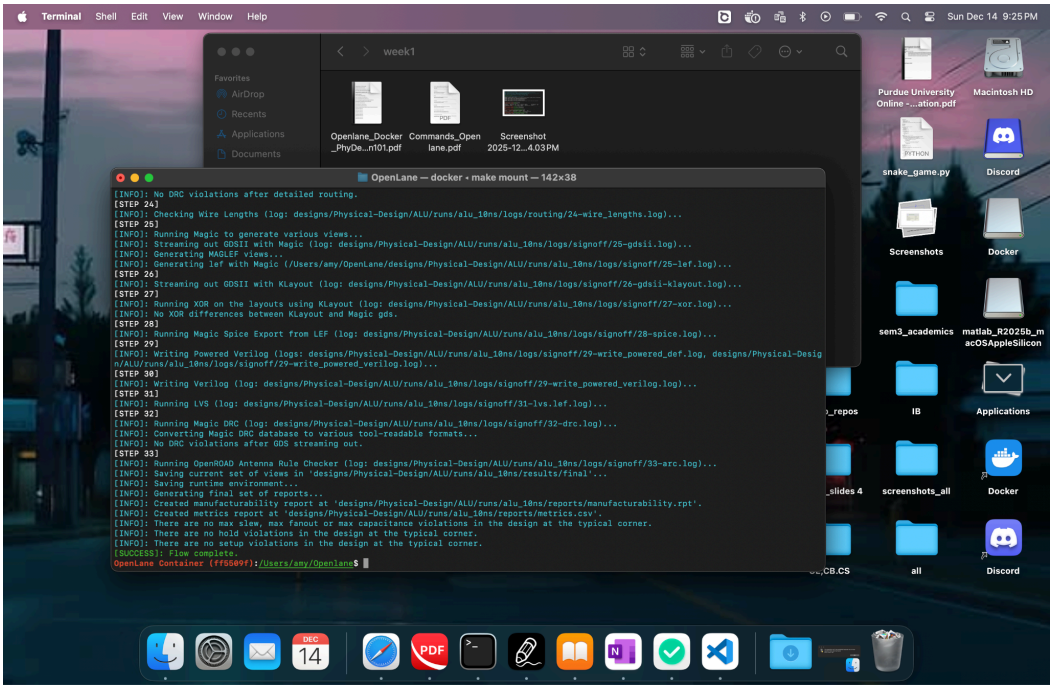
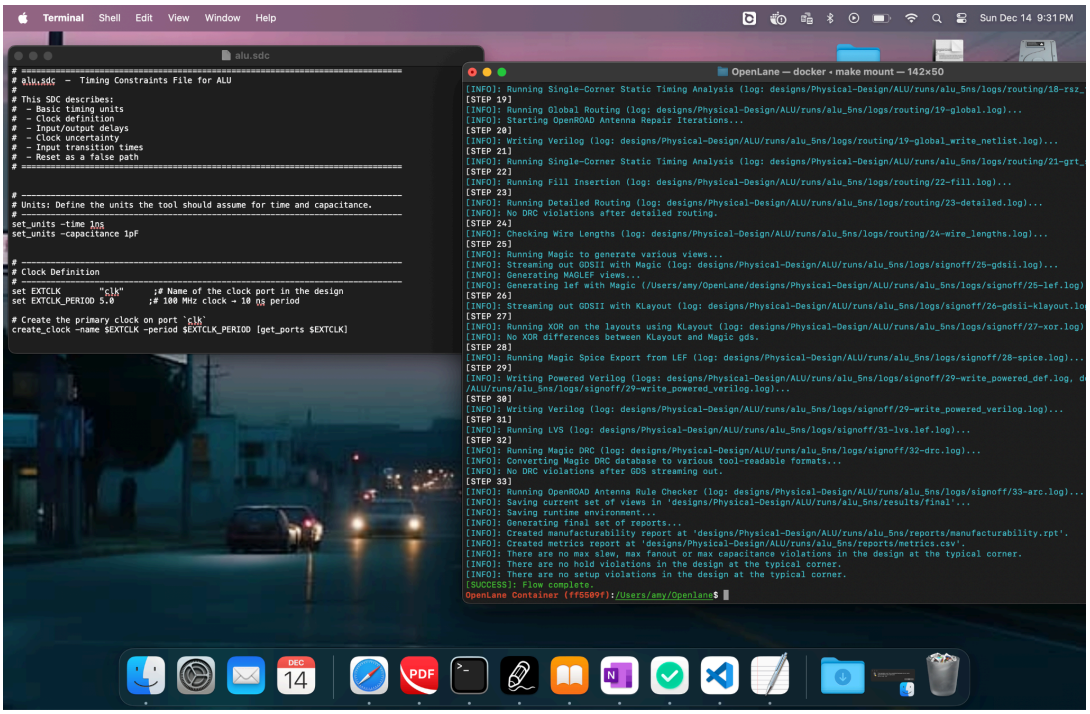
24b1312_Report_SSA_PhysicalDesign101_Assignment1_Openlane_Full&KS_Adder
Supriya Anand Mishra_ElectricalBtech

The full physical design flow

(below) alu_5ns



(below) alu_5ns



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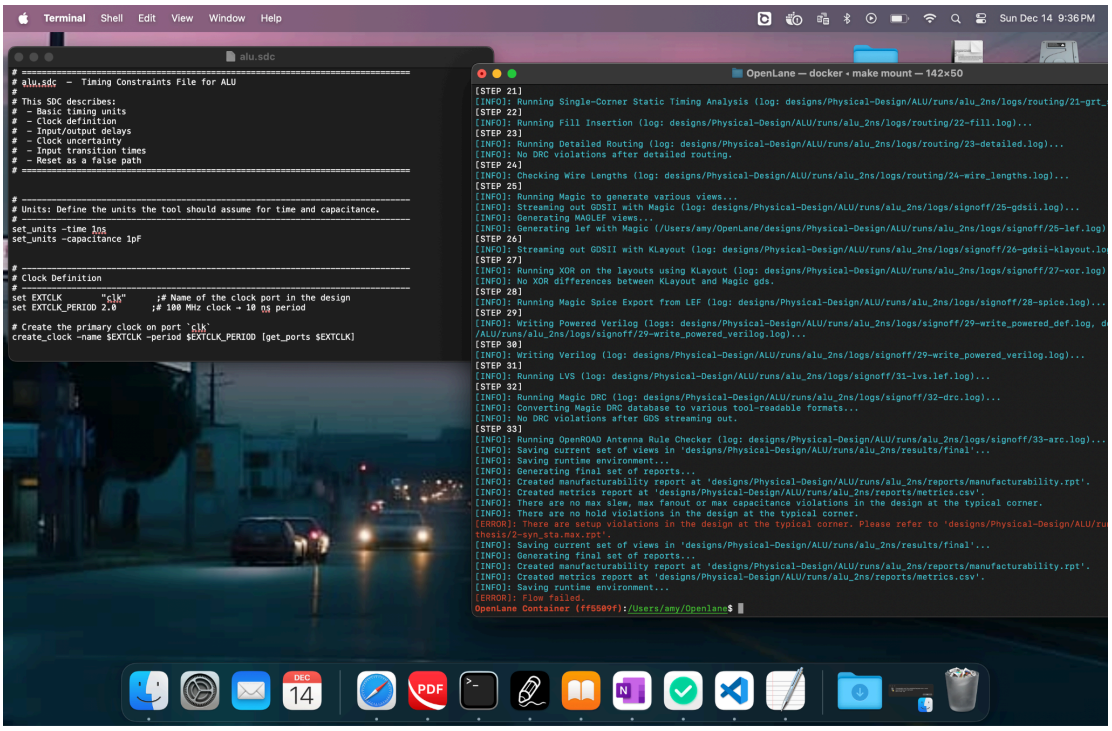
(below) alu_2ns



The ALU design successfully meets timing constraints at 10 ns and 5 ns clock periods with no setup or hold violations. However, when the clock period is tightened to 2 ns, post-route static timing analysis reports setup violations, indicating that the critical combinational paths cannot meet the aggressive timing constraint. This demonstrates the physical and logical limits of the design when targeting very high frequencies.

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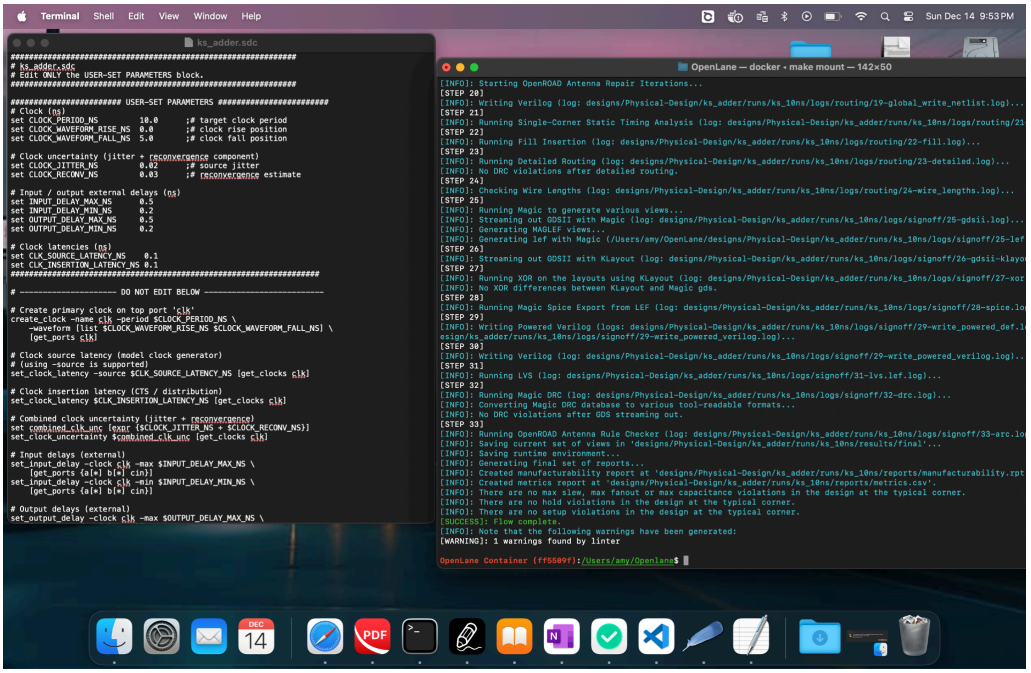
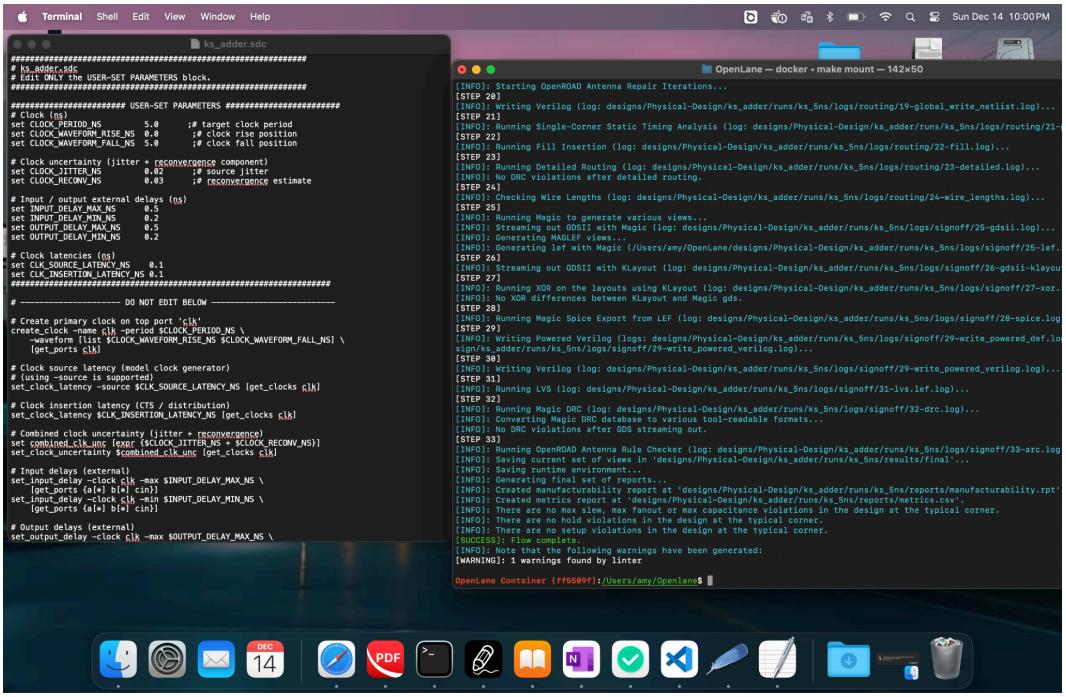
(below) ks_adder_10ns



(below) ks_adder_5ns



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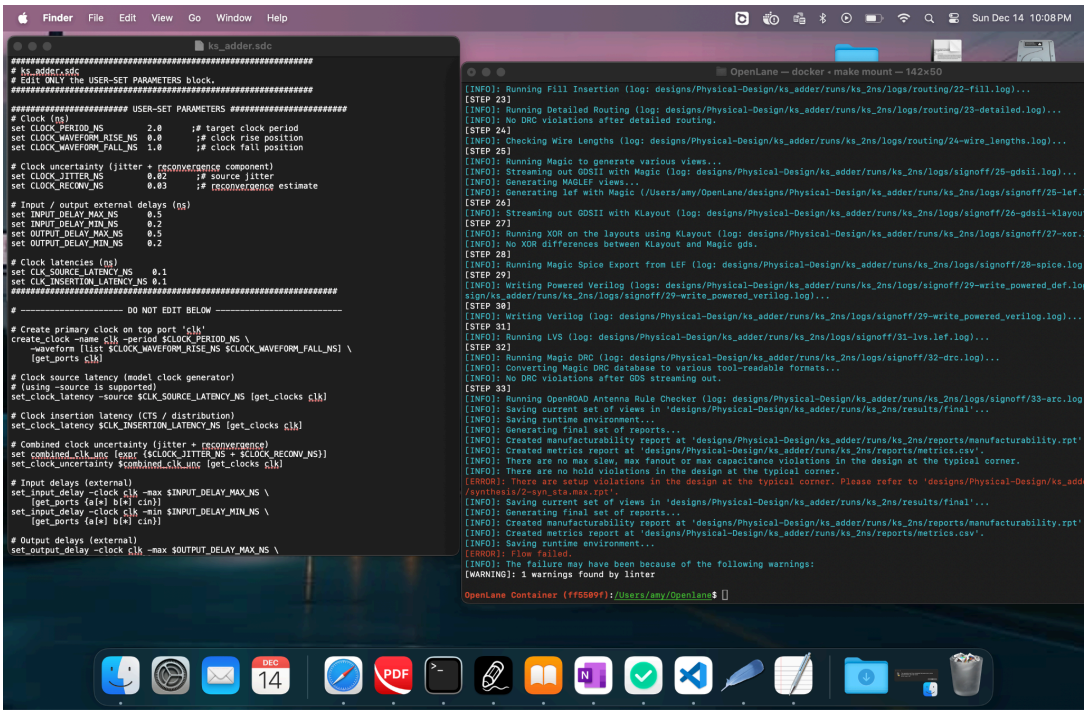
(below) ks_adder_2ns



Both the ALU and Kogge–Stone adder meet timing constraints at 10 ns and 5 ns clock periods, indicating that the backend flow can successfully optimize these designs for moderate operating frequencies. However, when the clock period is tightened to 2 ns, both designs exhibit setup violations despite full place-and-route optimization. This demonstrates the physical limitations imposed by combinational depth, routing parasitics, and clock distribution at aggressive frequencies. The Kogge–Stone adder shows higher routing complexity and area overhead compared to the ALU, highlighting the trade-off between theoretical speedup and backend implementability.

1)Physical_design_codes
https://drive.google.com/file/d/1qnoIeaRLtucXvi532X_pMXiwPUx13F7i/view?usp=sharing
2)Post_Simulation_Files(placement, routing ,synthesis)
https://drive.google.com/file/d/1qnoIeaRLtucXvi532X_pMXiwPUx13F7i/view?usp=sharing
3)Timing Analysis at Three Stages
https://docs.google.com/spreadsheets/d/1BFKDhbF69wjqO7UrwiDIvz7HG_2Vp1Bkdh3HA-lLh8Q/edit?usp=sharing
Post analysis synthesis, placement , routing for alu and ks_adder(sheet1 & 2)
4)metrics.csv
https://docs.google.com/spreadsheets/d/17iHOQjeyMFXhPCNQX0d0OlCPeU5DQ6JGY8ZBjiDhN1k/edit?usp=sharing

Conclusion

By running the complete OpenLane physical design flow on both the ALU and Kogge–Stone (KS) Adder, we observed how backend implementation strongly impacts timing and layout quality beyond logical design. As the clock period was reduced from 10 ns to 5 ns and further to 2 ns, setup timing became increasingly critical, with both designs meeting timing at relaxed clocks but exhibiting setup violations at aggressive constraints due to longer critical paths and interconnect delays. Hold timing remained largely unaffected across all runs, indicating stable short-path behavior.

In terms of physical characteristics, the ALU showed lower routing complexity and more predictable timing closure, benefiting from simpler logic and localized interconnects. The KS Adder, while theoretically faster at the logic level, introduced higher routing congestion and longer wire lengths due to its parallel-prefix structure, making timing closure more challenging under tight clock constraints. Area utilization was comparable, but the KS Adder required more careful routing and buffering. Power metrics were not evaluated due to the absence of switching activity; however, the increased routing and buffering in the KS Adder suggests higher dynamic power in a realistic scenario.

Overall, the ALU architecture behaved more robustly in the backend flow, while the KS Adder highlighted the trade-off between logical speed and physical implementability, emphasizing the importance of considering physical design effects early in architecture selection.