Winter Semicondutor School (WSS)
Semiconductor Fabrication 101

Assignment 1

Student Name: _____

Roll Number: _____

December 6, 2025

Instructions

- Write your answers clearly and concisely.
- Include relevant diagrams for fabrication process flows.
- Submit as a PDF before the deadline which is 14 Dec
- Tentative weightage of this assignment is 20 per cent.

Problem 1 (2)

Question: The single-crystal silicon has a diamond cubic unit cell with a lattice constant a = 0.543 nm at room temperature. Show that:
(a) Find the distance between nearest neighbours in terms of a, where a is the dimension of the unit cell. Also, make a sketch for visualisation.
(b) Find the density of silicon. . The mass of a silicon atom is approximately 4.664x10e-26 kg.

Problem 2 (4)

Design a process flow for electroplated Ni thin films (5 μm thick) on a silicon substrate using SiO2 as a bottom dielectric. Show this sequentially in terms of process cross-sections starting with a blank silicon substrate with photoresist deposition and patterning steps included.

Problem 3 (3)

A (100) n-type silicon substrate 525 μm thick is to be etched with KOH which has an etch rate of 1.1 μm/min for the [100] direction. The etch rate in the [111] direction is assumed to be negligible. Silicon Nitride is used as an etch mask for this process.
(a) What is the minimum opening at the top of the wafer to etch all the way through and leave a gap of 10 μm at the bottom? You may assume that the bottom of the wafer is fully masked (protected) during the KOH etch and any masking silicon nitride is removed at the end of the process.
(b) How long does it take for the wafer to be etched all the way through?
(c) One of the features to be created is a self-limiting V-groove that is 50 μm deep. What is the opening required at the top of the wafer to achieve this?

Problem 4 (1)

An IC manufacturing plant produces 100 wafers per week. Assume that each wafer contains 100 die, each of which can be sold for $ 50 if it works. The yield on these chips is currently running at 50%. If the yield can be increased, the incremental income is almost pure profit because all 100 chips on each wafer are manufactured whether they work or not. How much would the yield have to be increased to produce an annual profit increase of $10M?

Problem 5: Simulation exercise (10)

This is a simulation exercise in Magic VLSI tool for the better understanding of processes in fabrication CMOS. You will design a basic inverter for ease.

Check out **this** video to quickly understand how this layering is actually done while manufacturing in fabs to implement the design which you will make in Magic.

Refer to **this** for better understanding of each step in CMOS Fabrication with explanantion.

Follow **this** video to install the magic tool.

Follow any of these videos to understand how to use Magic and design the inverter.

1

2.1

2.2

Along with the PDF of other questions, attach a screenshot of the Magic layout and zero DRC-error proof.

NOTE - Take SS of the complete magic screen window. Then only we will consider it. Zip it with the inverter.mag file for final submission.

References

- Plummer, Deal, Griffin, *Silicon VLSI Technology.*
- Slides from FAB101 (WSS).