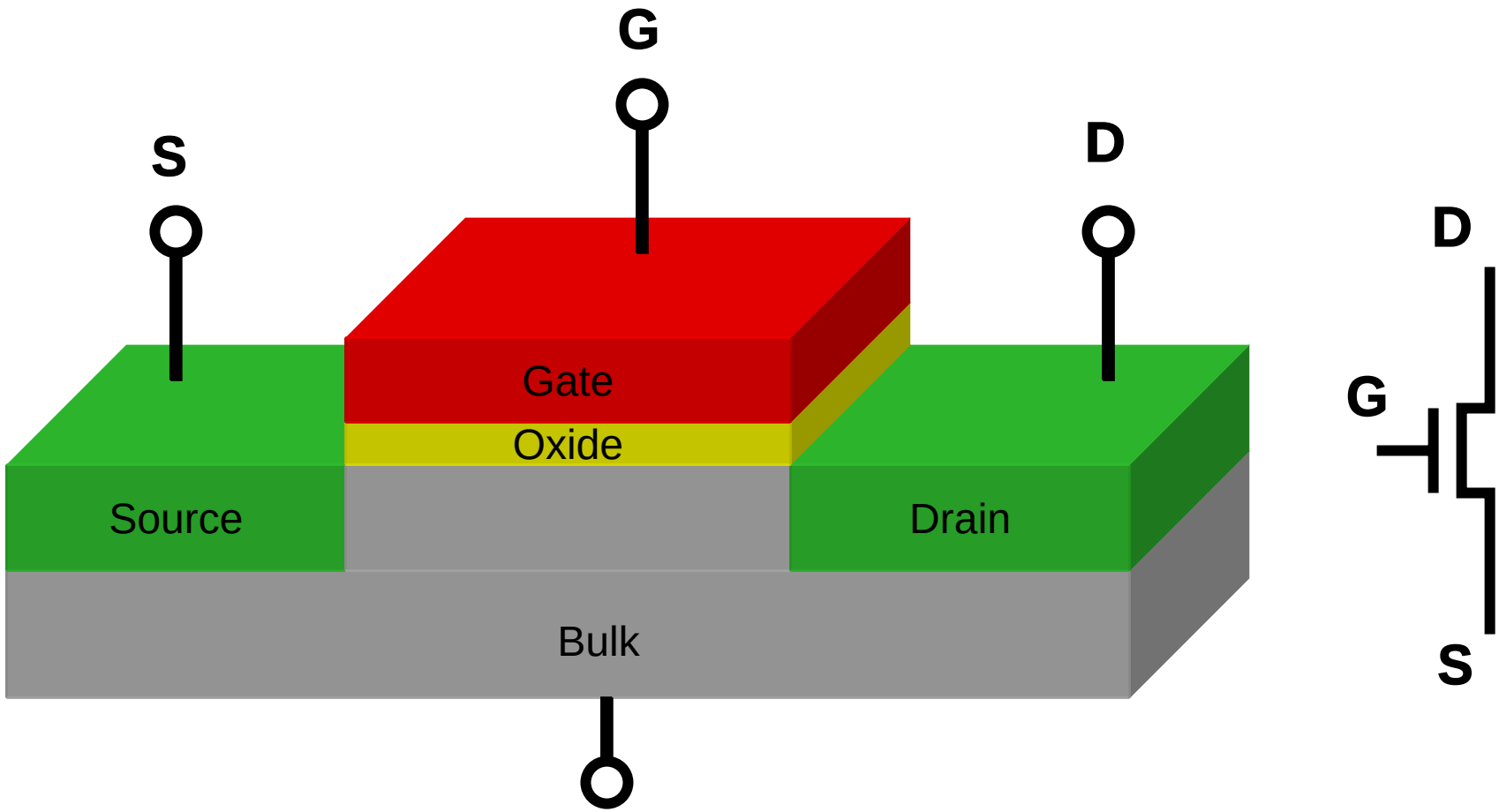
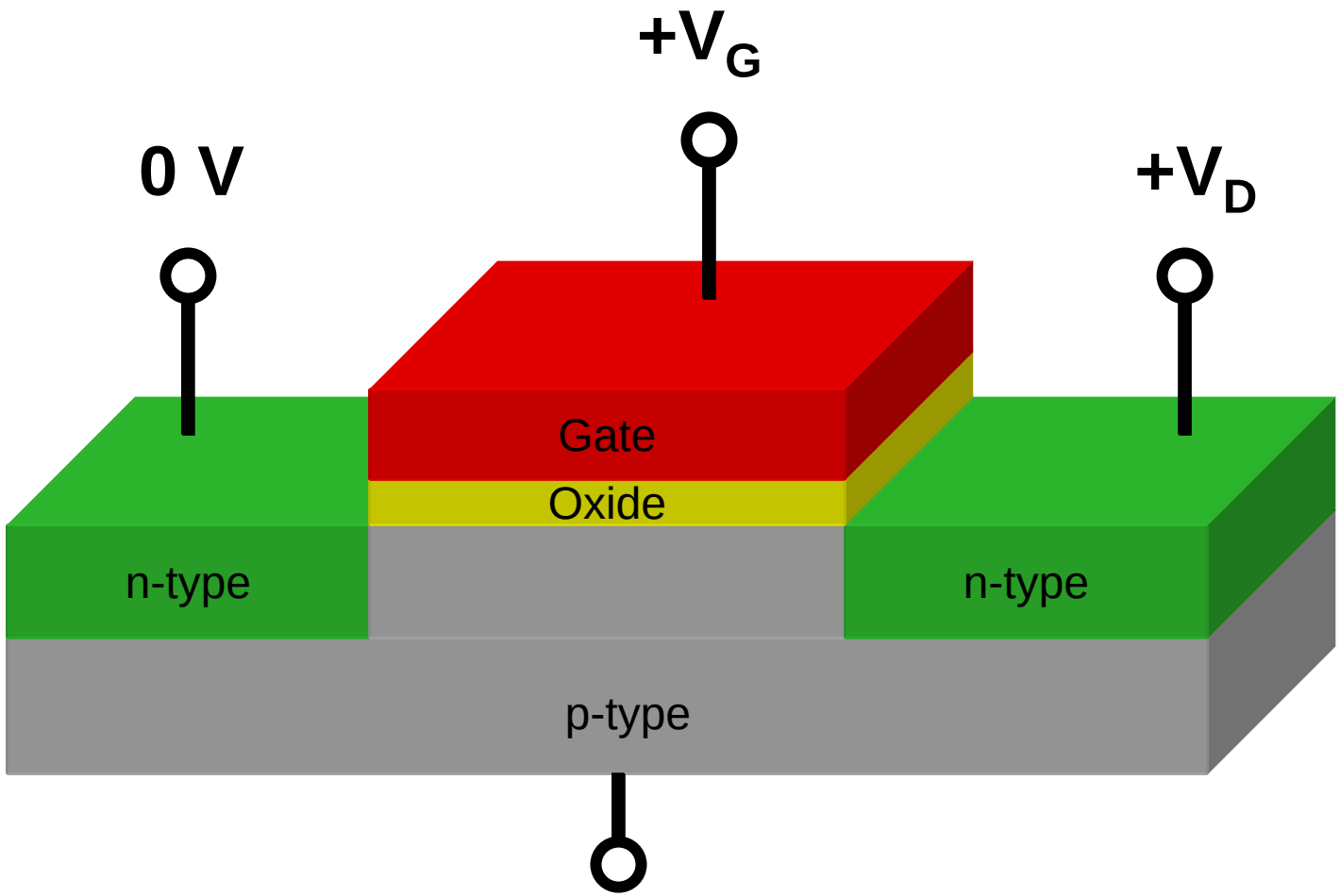
Outline

- The MOSFET Structure
- Semiconductor Doping
- The MOSFET as a Switch
- A MOSFET Process
- The MOS Capacitor Process
- Recommended reading
  - Plummer, Chapters 1 and 2

MOSFET



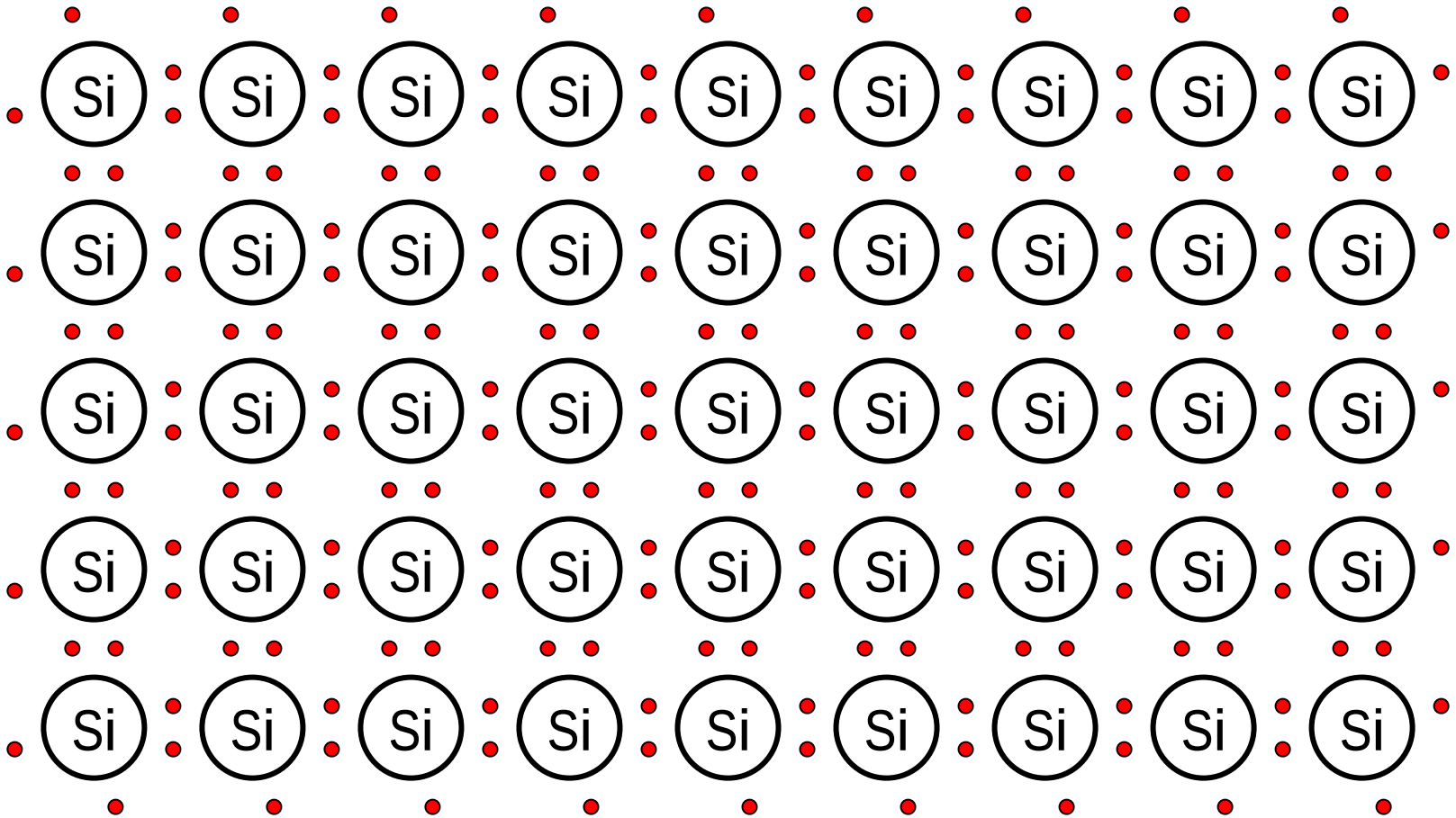
N-Channel MOSFET



A Word About Doping....

Silicon has four valence electrons

It covalently bonds with 4 adjacent atoms in the crystal lattice

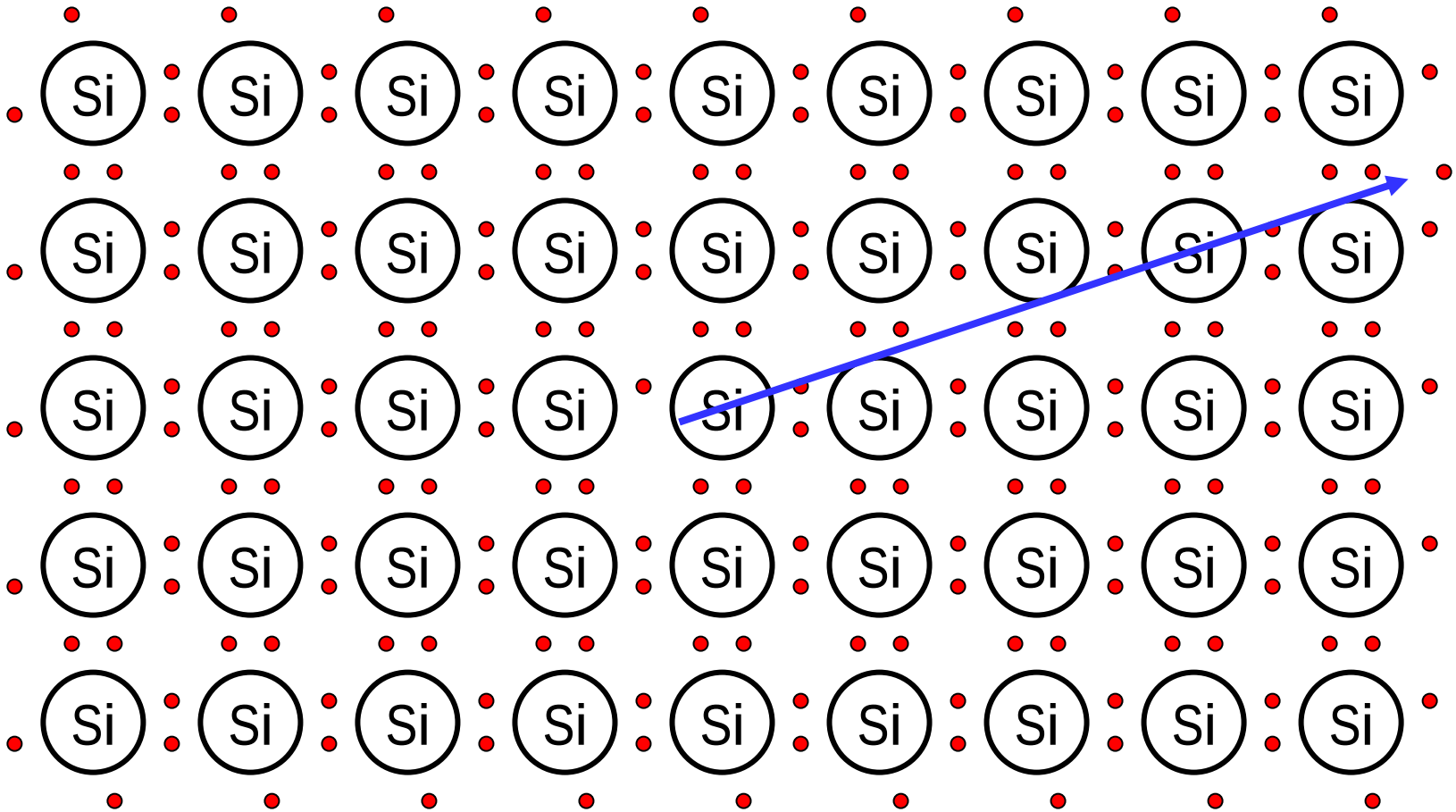


Intrinsic Semiconductor

Increasing Temperature Causes Creation of Free Carriers

10^{10} cm^{-3} free carriers at 23C (out of $2x10^{23}$ cm^{-3})

➡ Intrinsic Conductivity

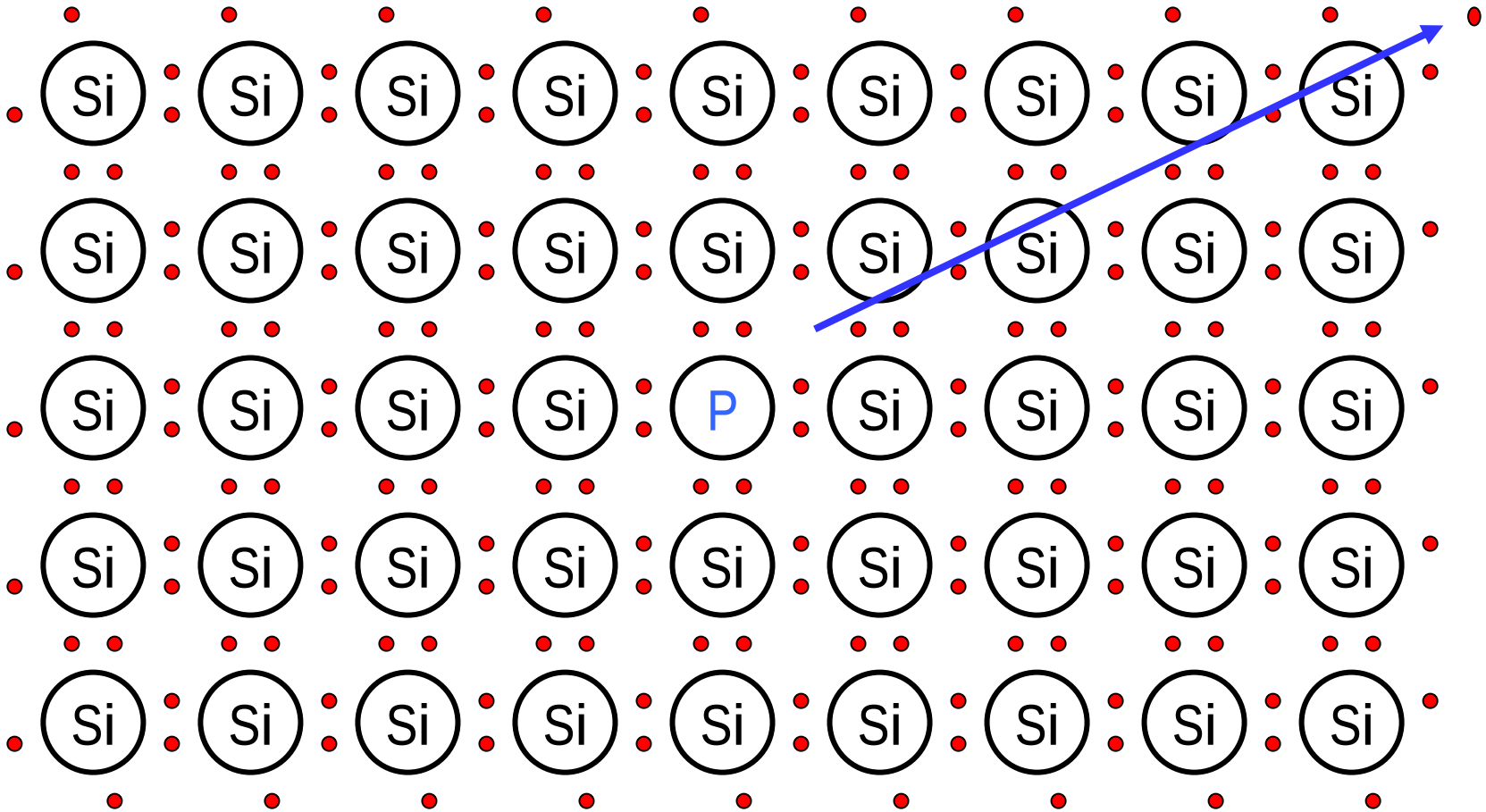


N-type Doping

Phosphorus has 5 valence electrons

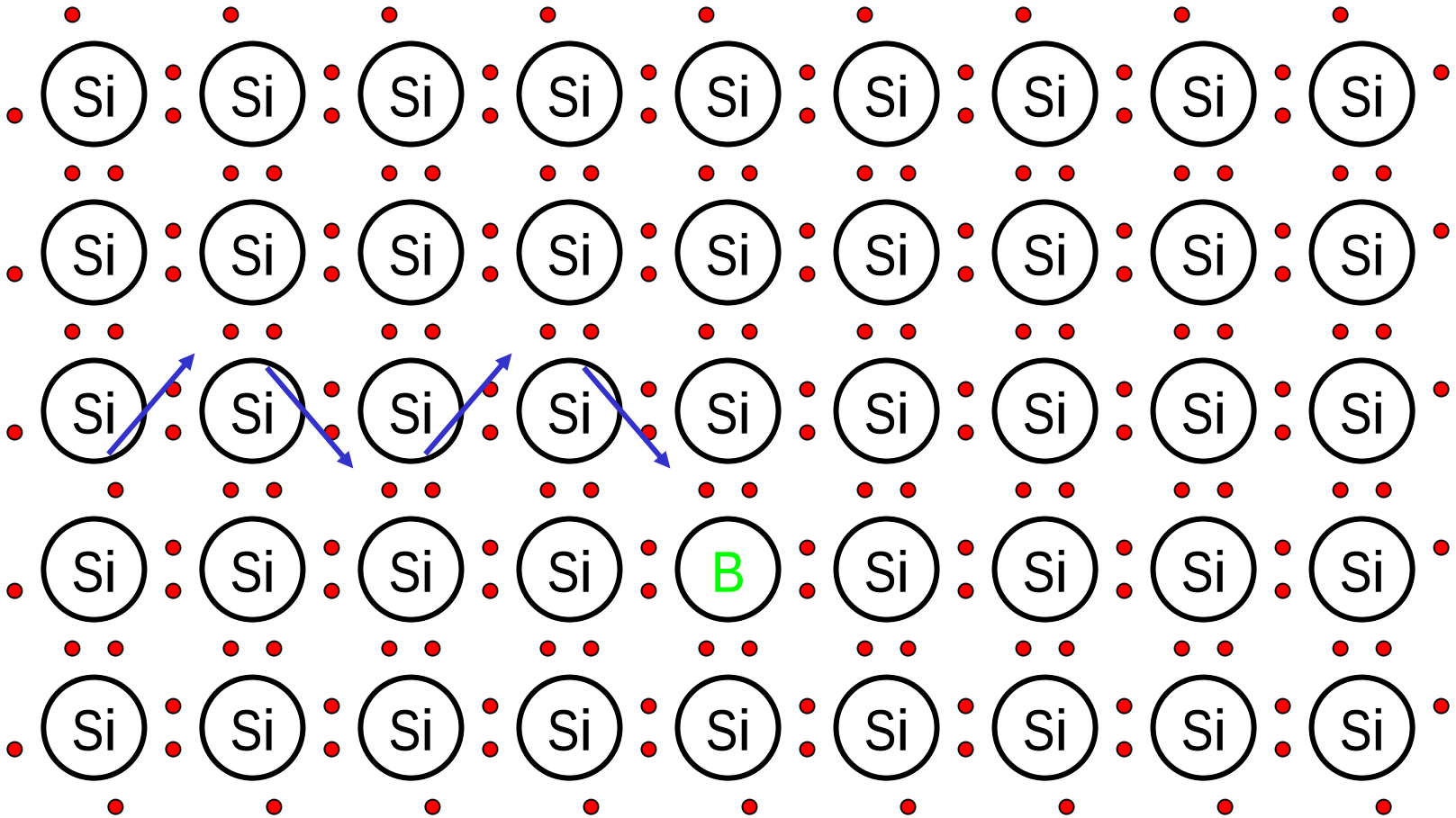
'Donates' one conduction electron – *n-type*

Our substrate has 10^{15} cm^{-3} phosphorus (1 in 10^8)



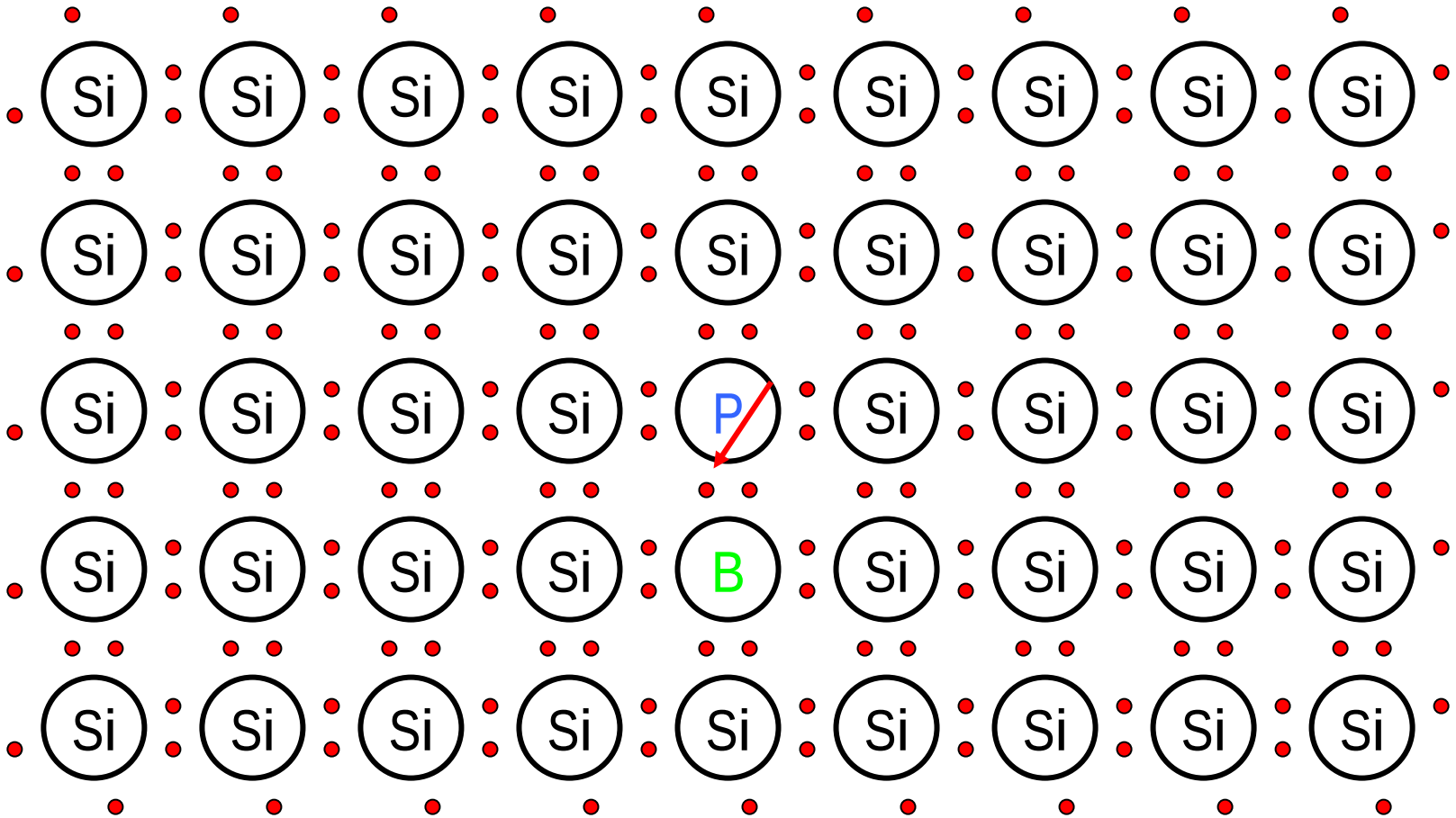
P-type Doping

Boron has 3 valence electrons
'Accepts' one electron from lattice
Creates a 'hole' – *p-type*



Counter Doping

The addition of one more B than P causes the doping type to change from n-type to p-type



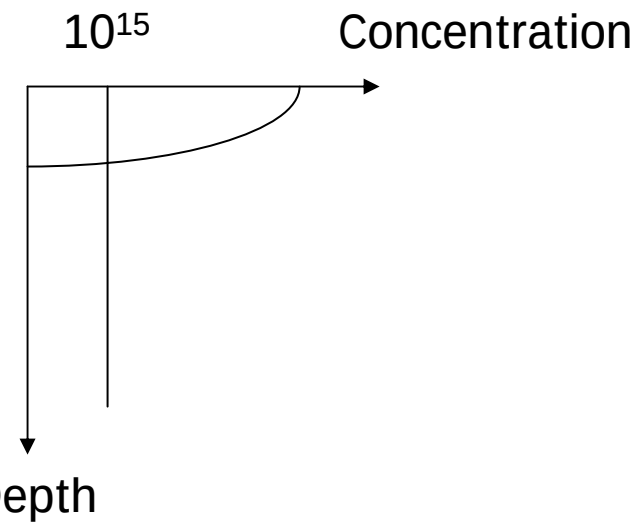
Counter Doping Process

n-type (10^{15} cm^{-3})

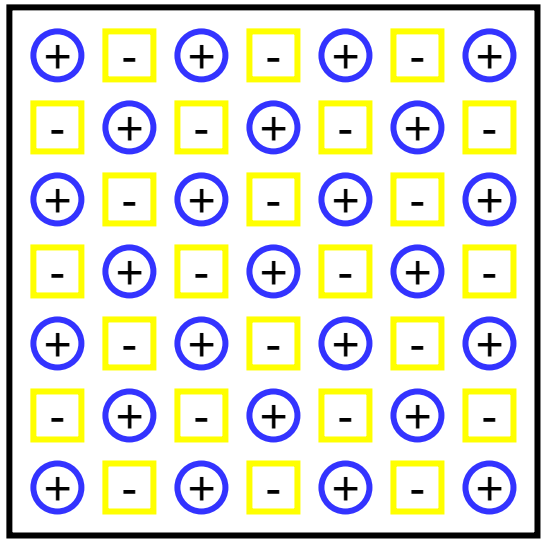
Implant Boron and Anneal

p-type (>10^{15} cm^{-3})

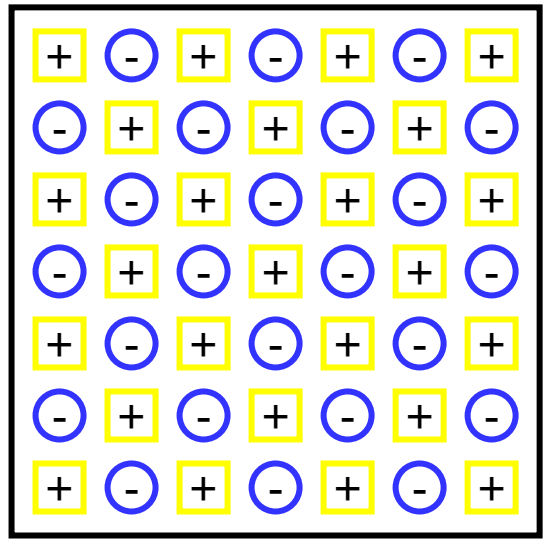
n-type (10^{15} cm^{-3})



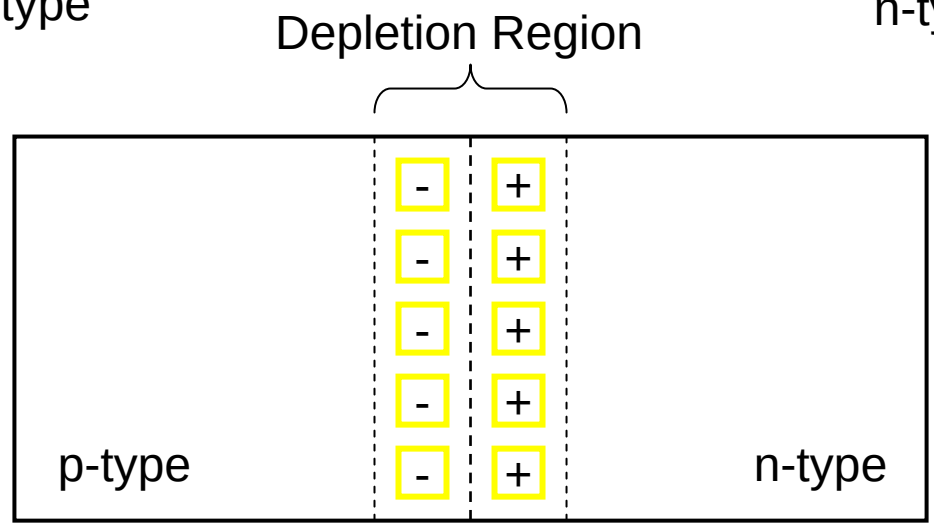
P/N Junction



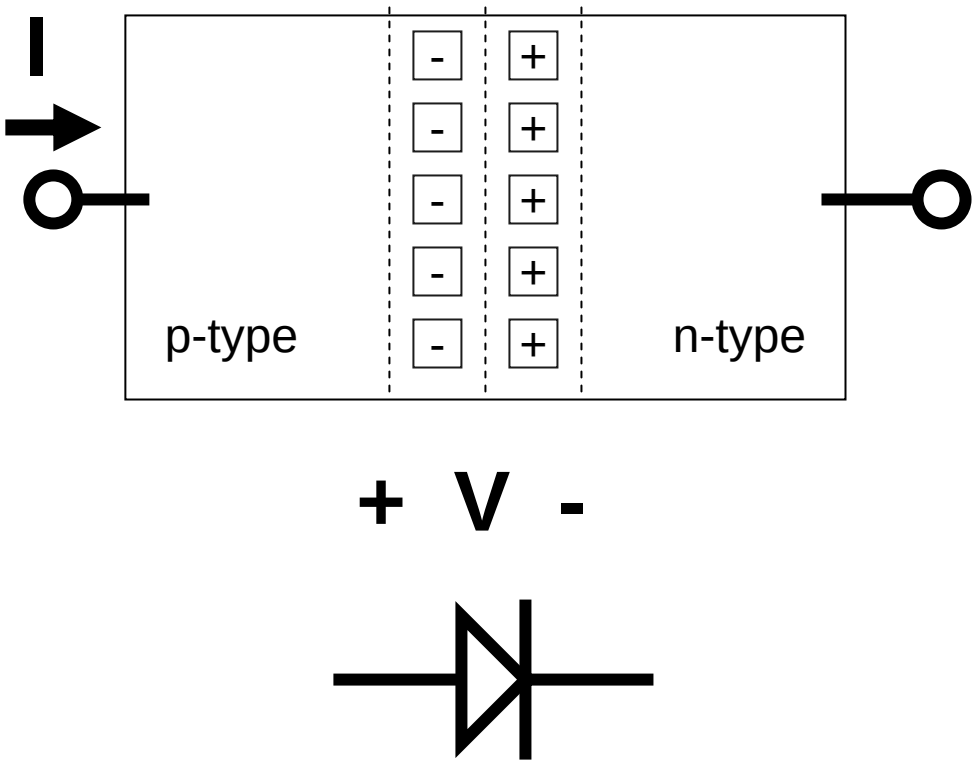
p-type

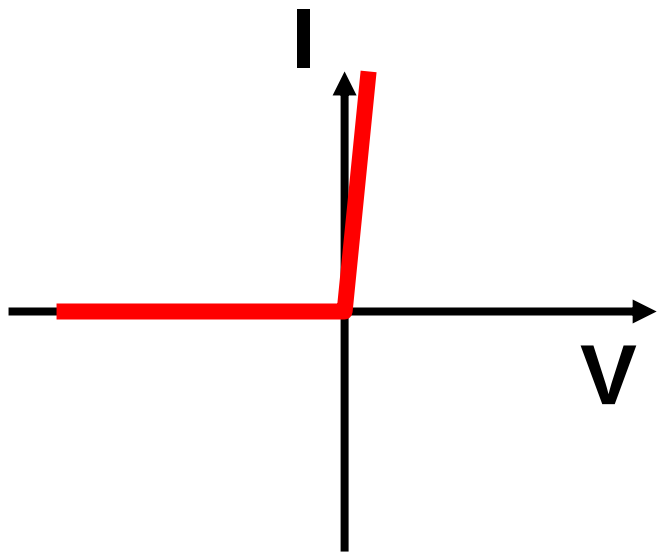


n-type

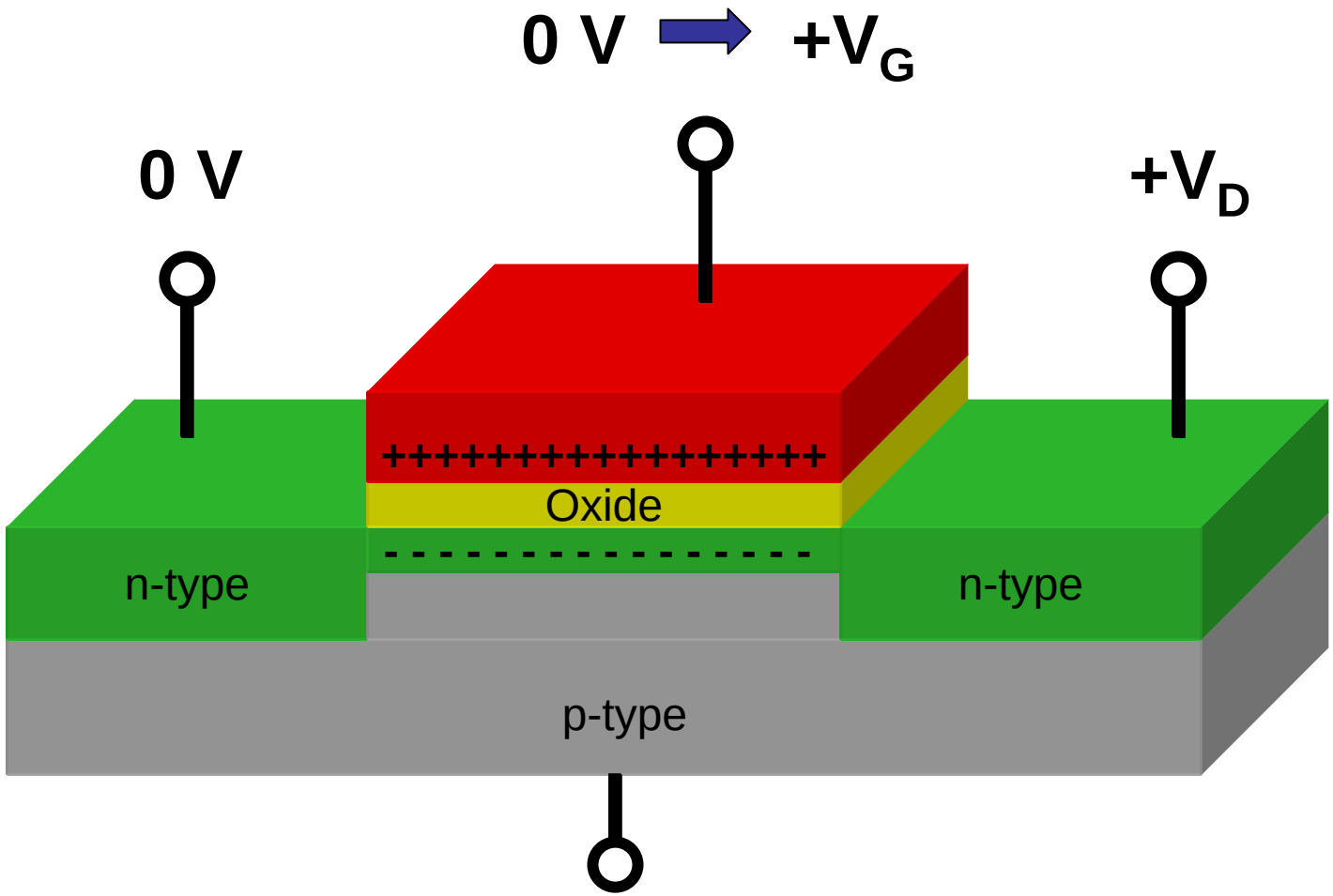


P/N Junction - Diode

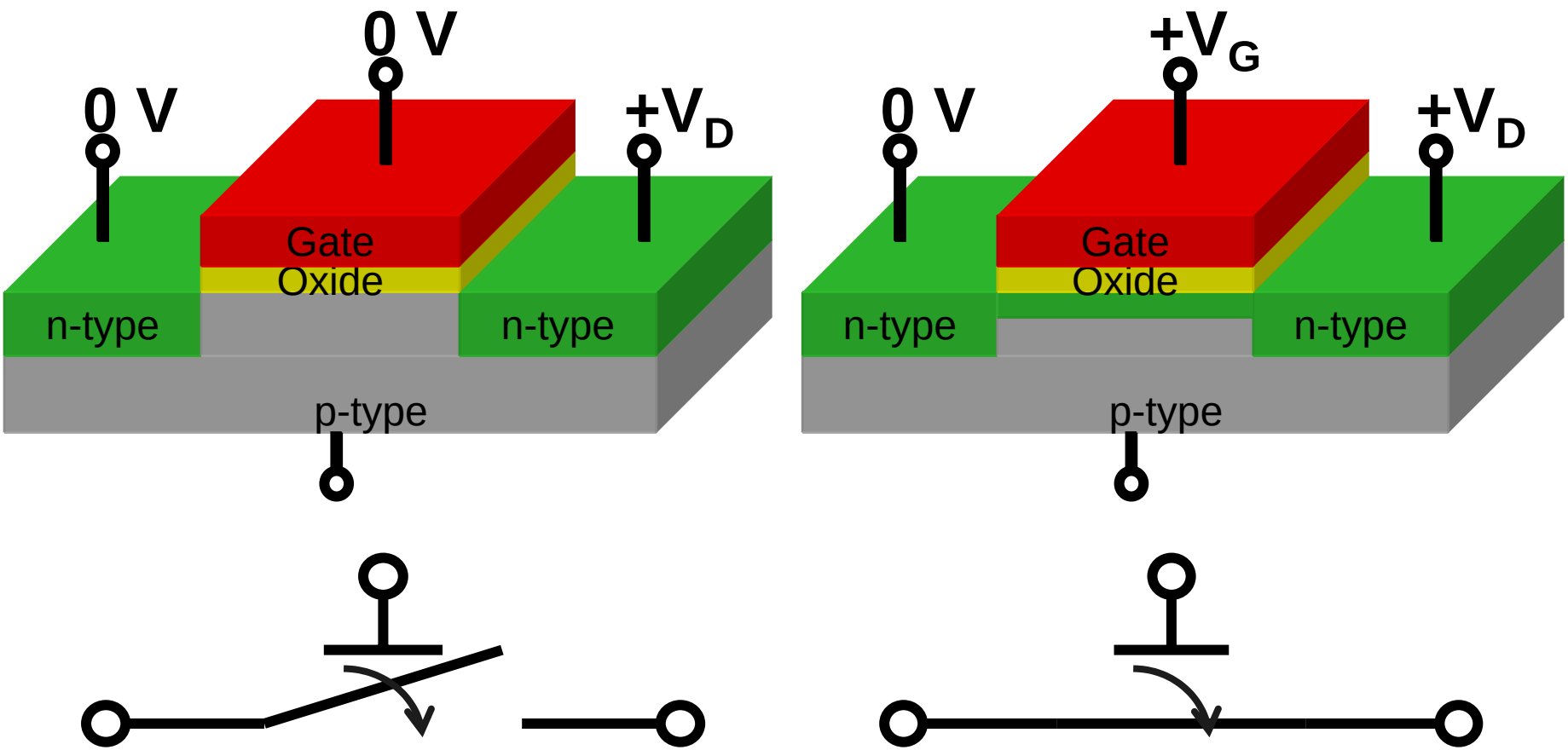




N-Channel MOSFET Operation



MOSFET as a Switch

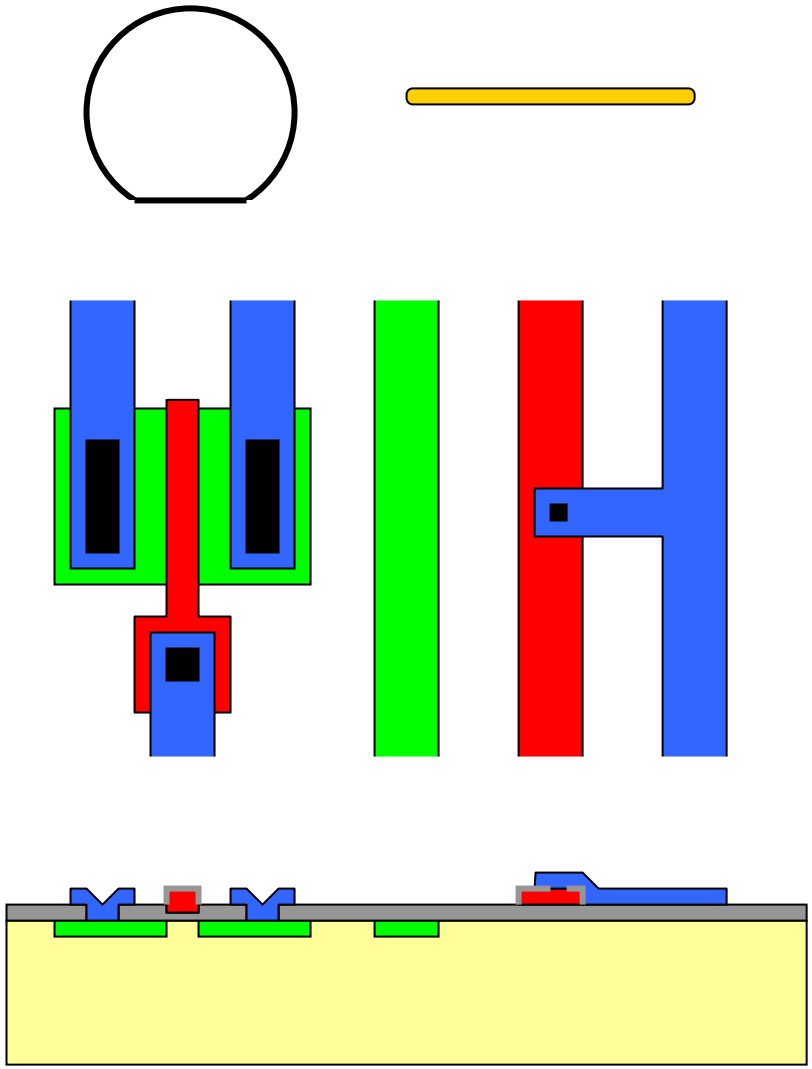


Microfabricated Devices

- Starting Material
  - Single crystal silicon
- Mask Set
  - Contains x,y info

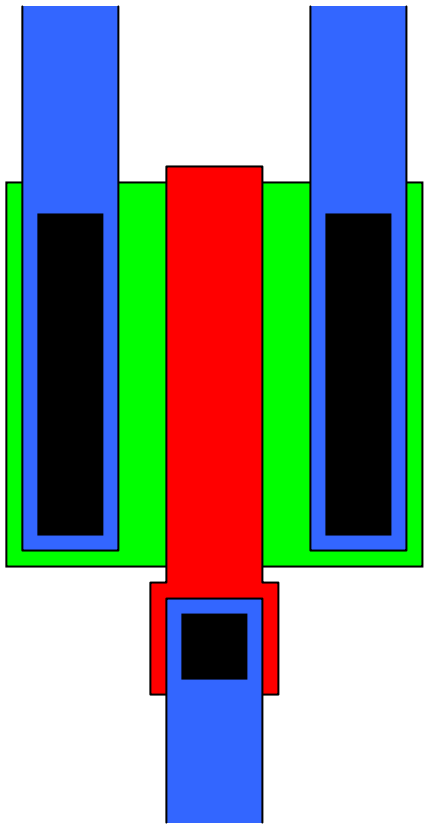
    (Top View)
- Process Sequence
  - Contains z info

    (Cross Section)

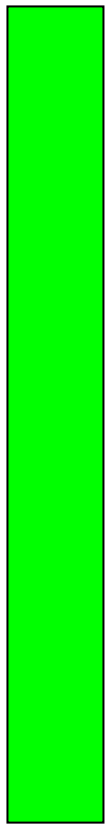


Sample Mask Set

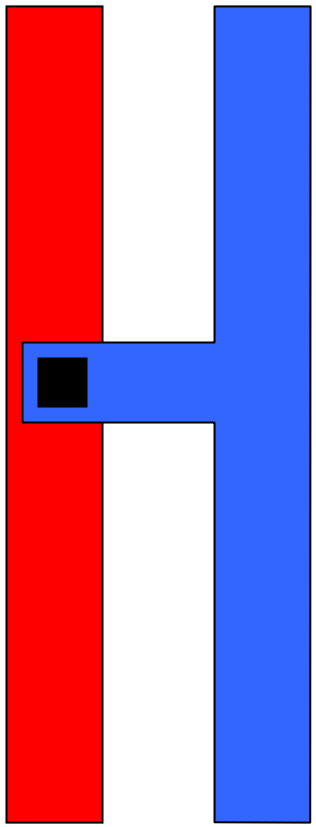
- Four Levels (Masks)



Transistor (MOSFET)



Diffusion Resistor (Diode)



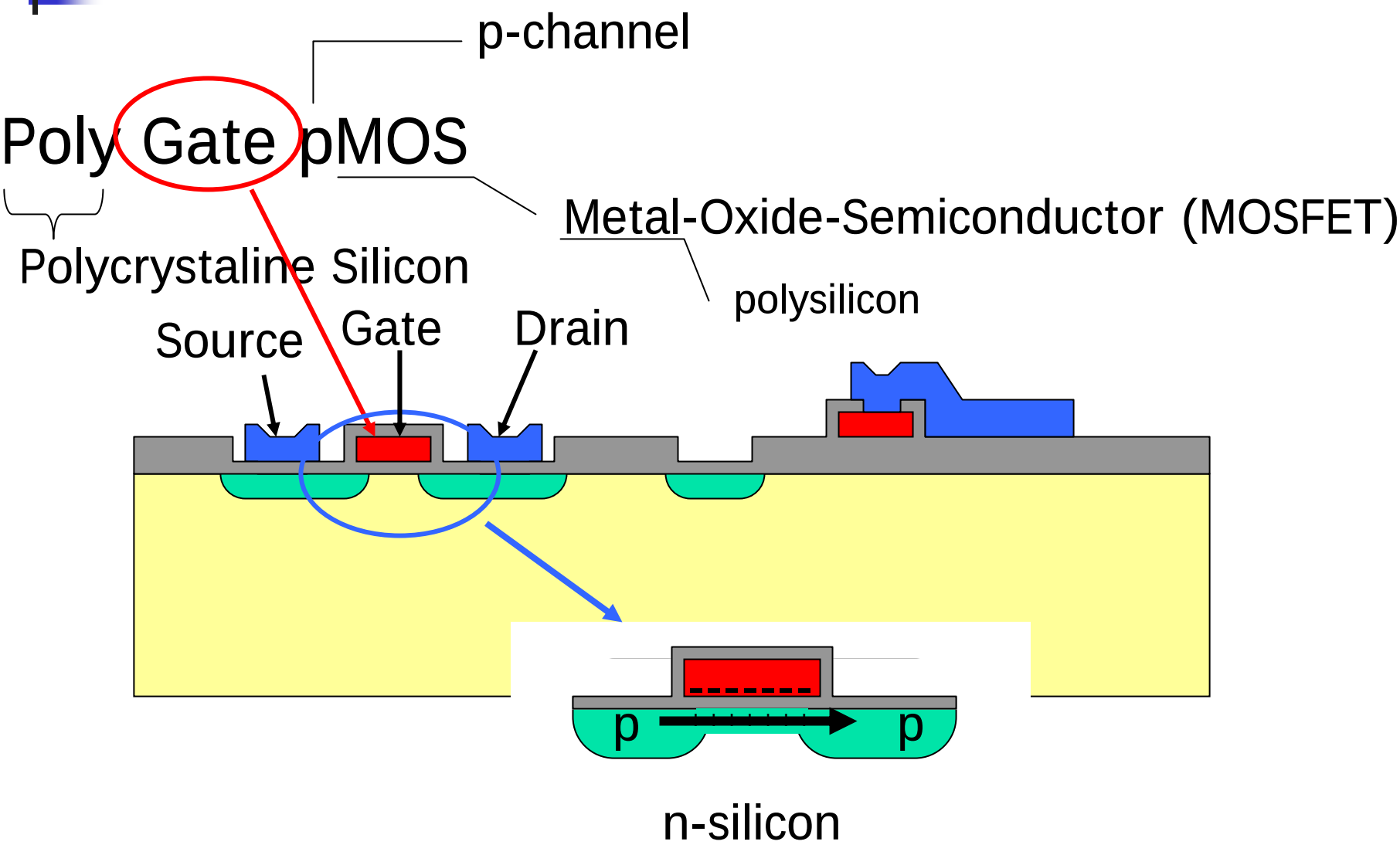
Polysilicon Resistor

Metal Resistor

Mask	Definition
1	Active Area
2	Polysilicon
3	Contact Cuts
4	Aluminum

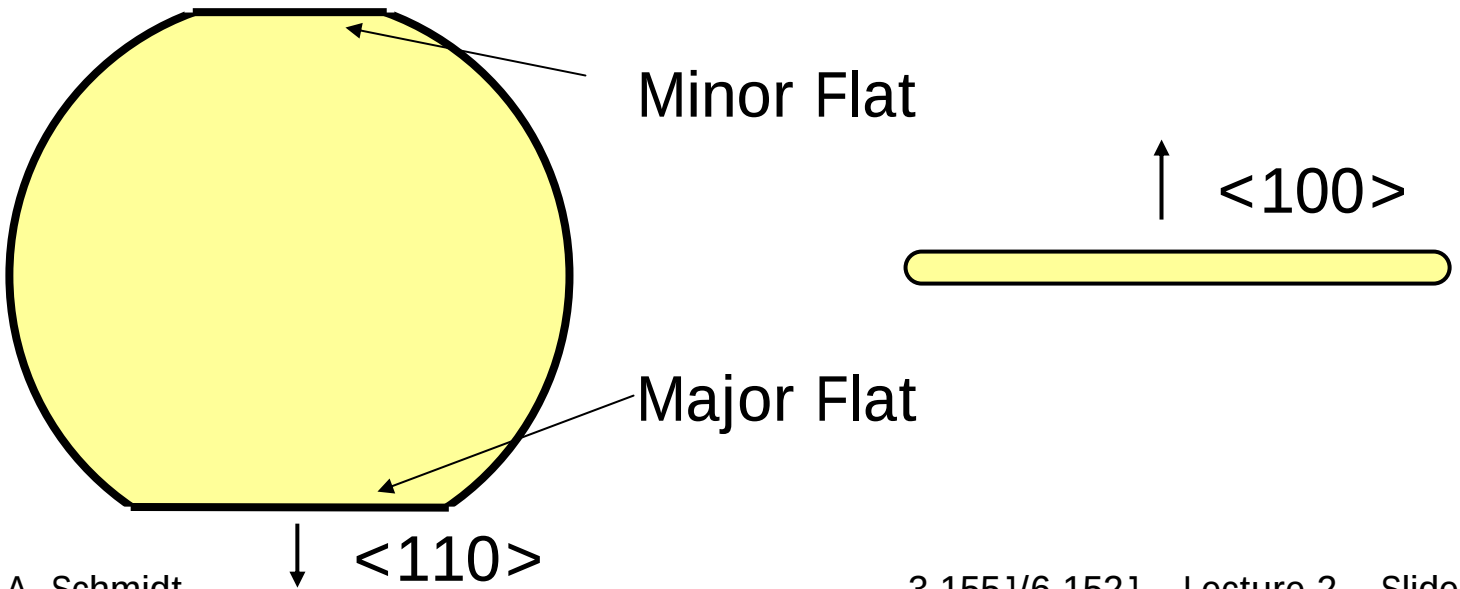
Our Process

- Poly Gate pMOS



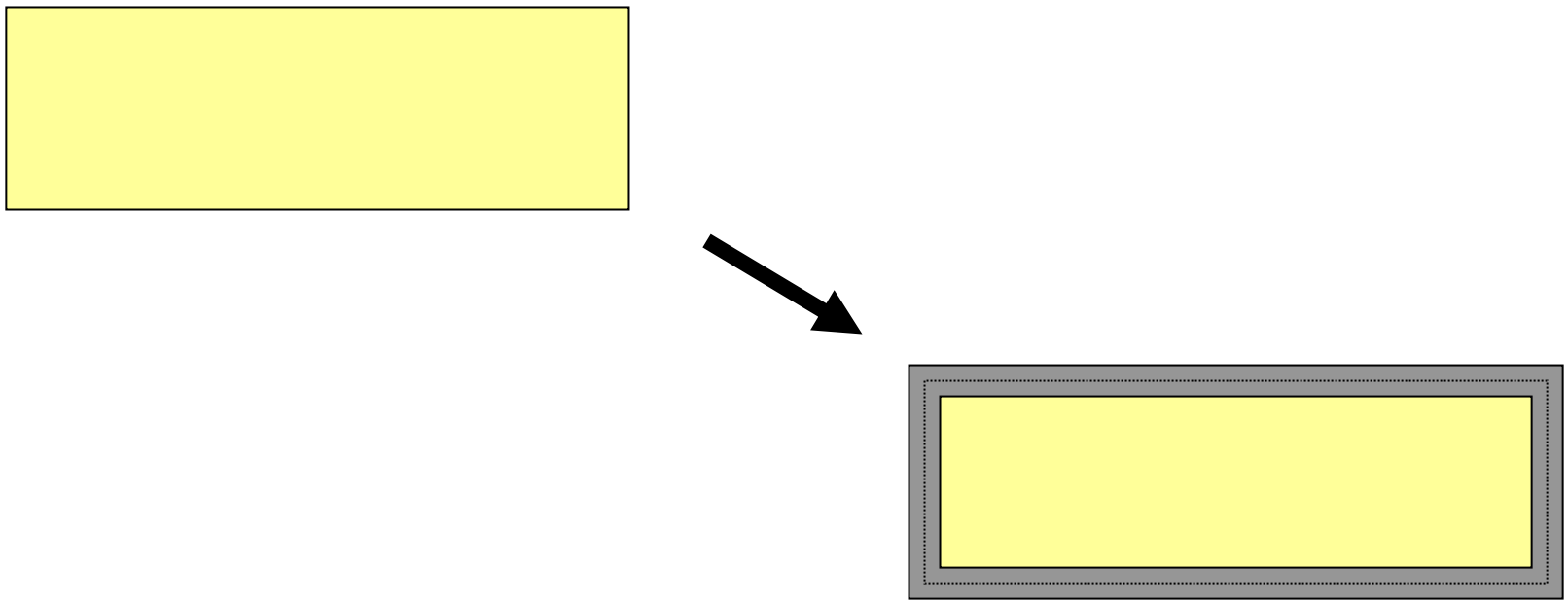
Starting Material

- 6” (150mm) Diameter Silicon Wafer
  - 30 +/- 1 mil thick (~750 μm)
  - n-type (doped with Phosphorus)
    - 1.5 Ω-cm resistivity (10^{15} cm^{-3} Phos)
  - <100> crystal orientation



FET Process Steps

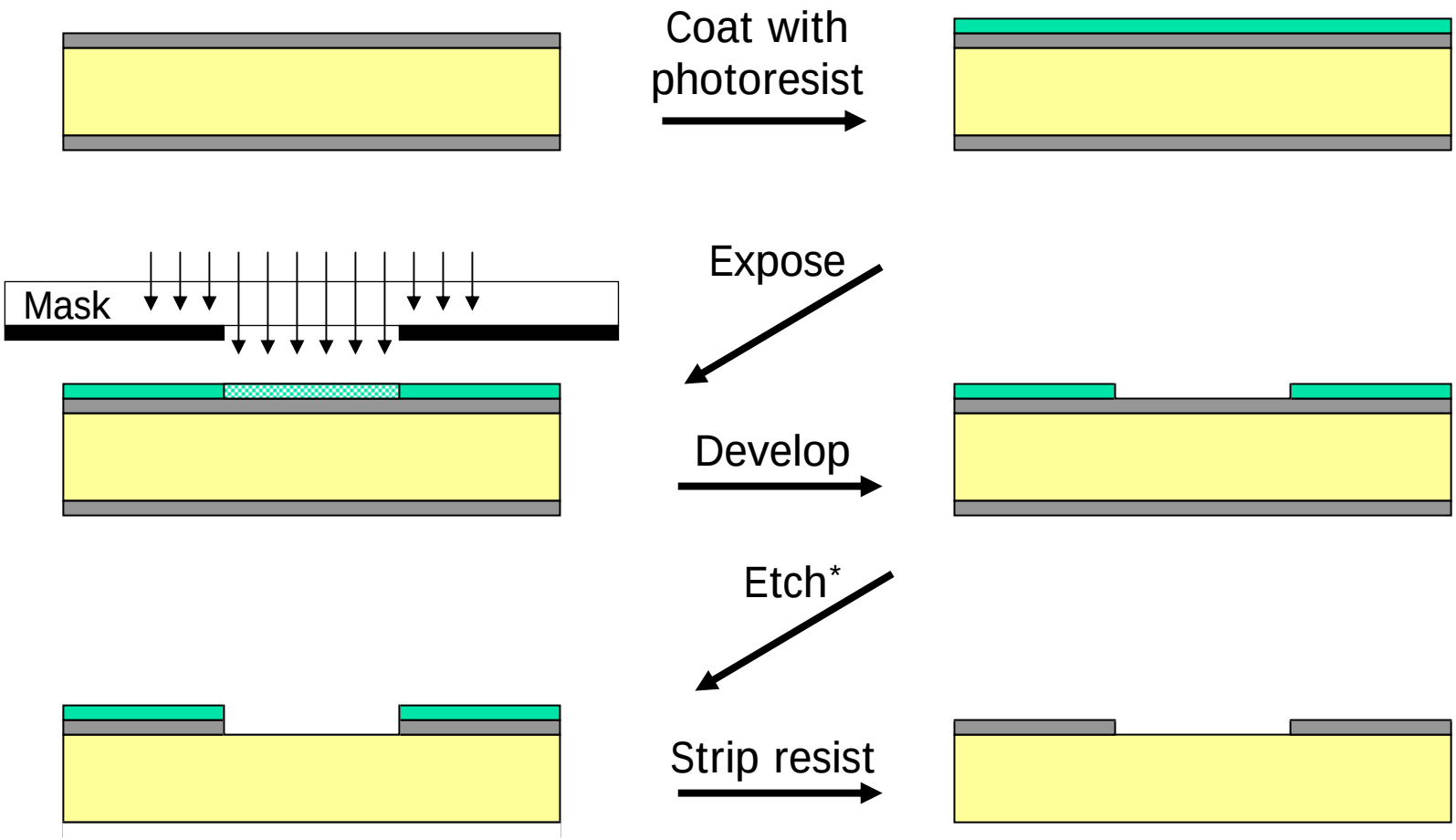
1. Characterize the wafer (resistivity, orientation, and type)
2. Grow 5000A ‘Field Oxide’ for device isolation



Typically at 800-1100C for 1 hour in O_2 or steam

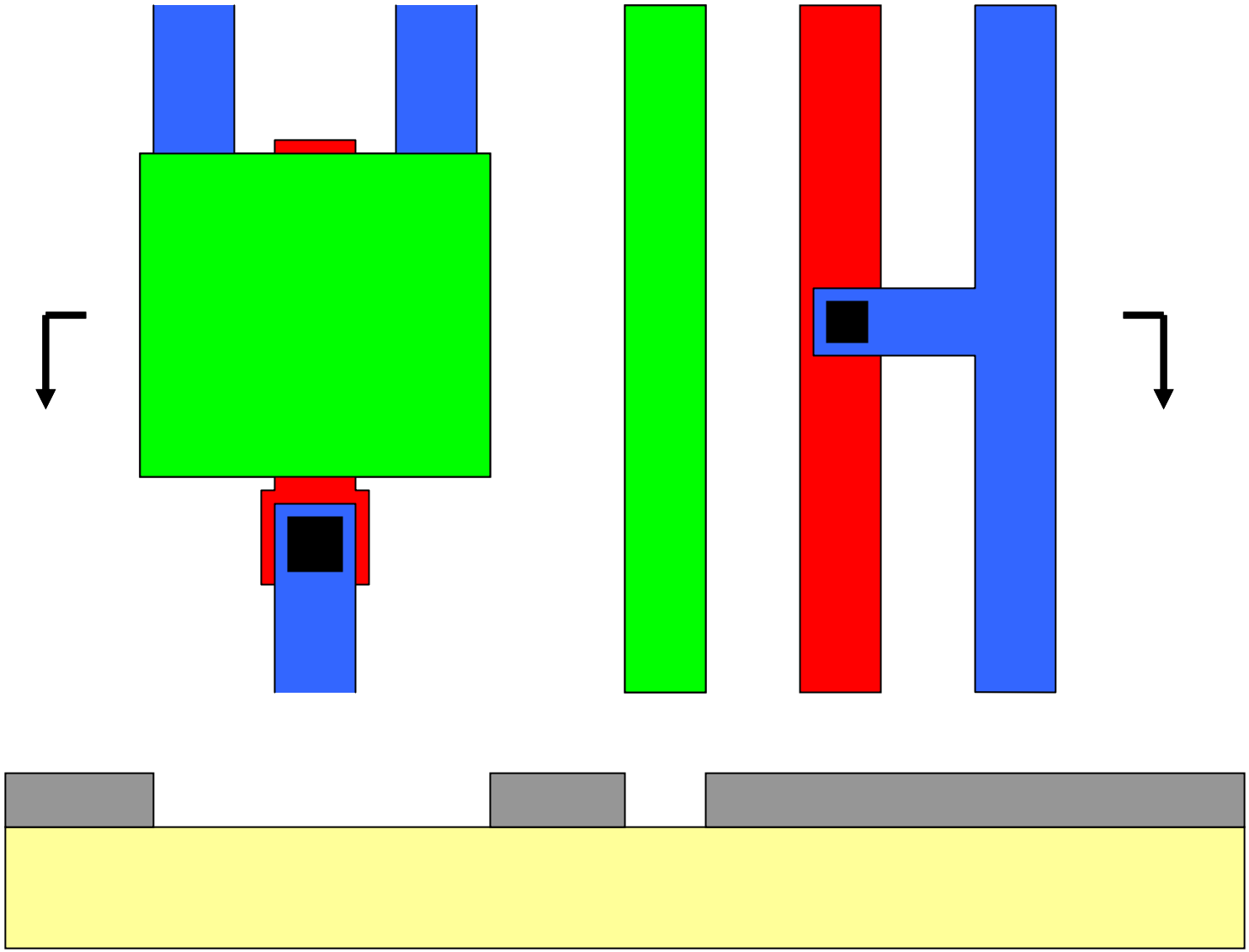
Process Steps

3. Pattern Active Area (Mask #1)



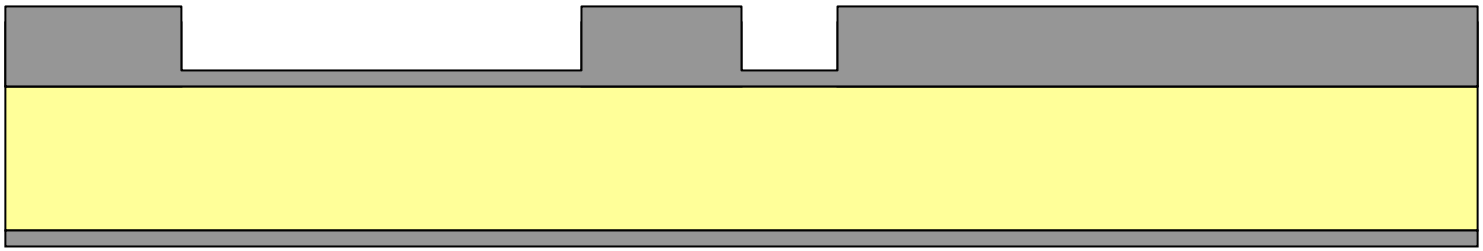
*Wet etch

Process Steps

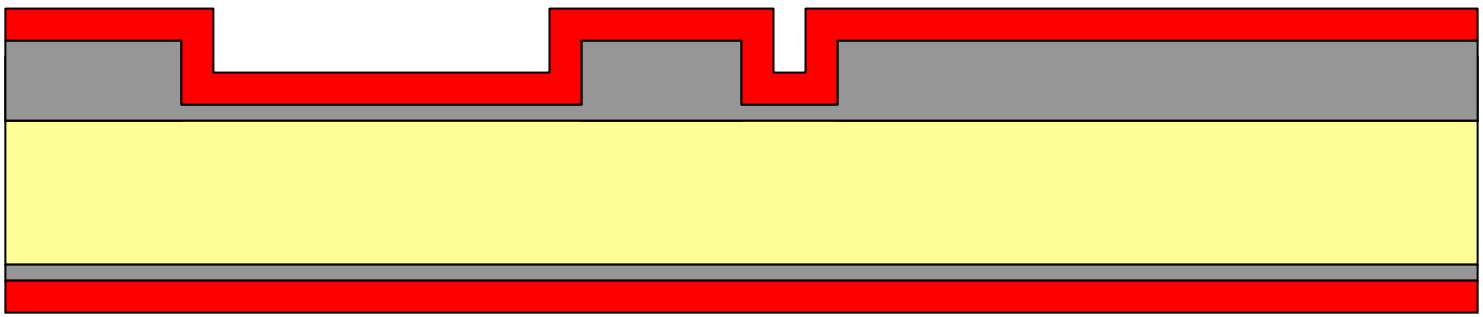


Process Steps

4. Grow 500A Gate Oxide

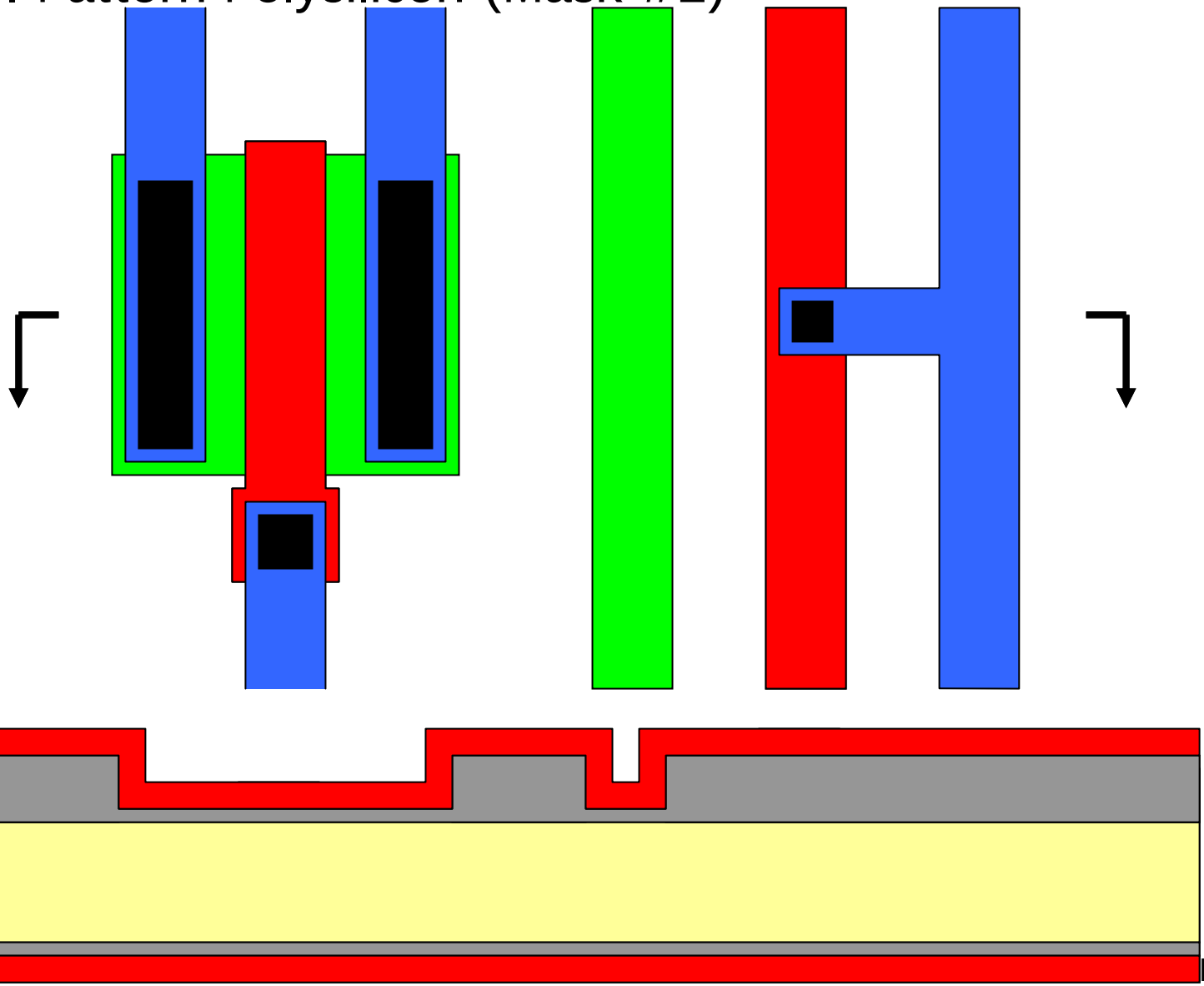


5. Deposit 5000A Polysilicon by LPCVD (low pressure chemical vapor deposition)



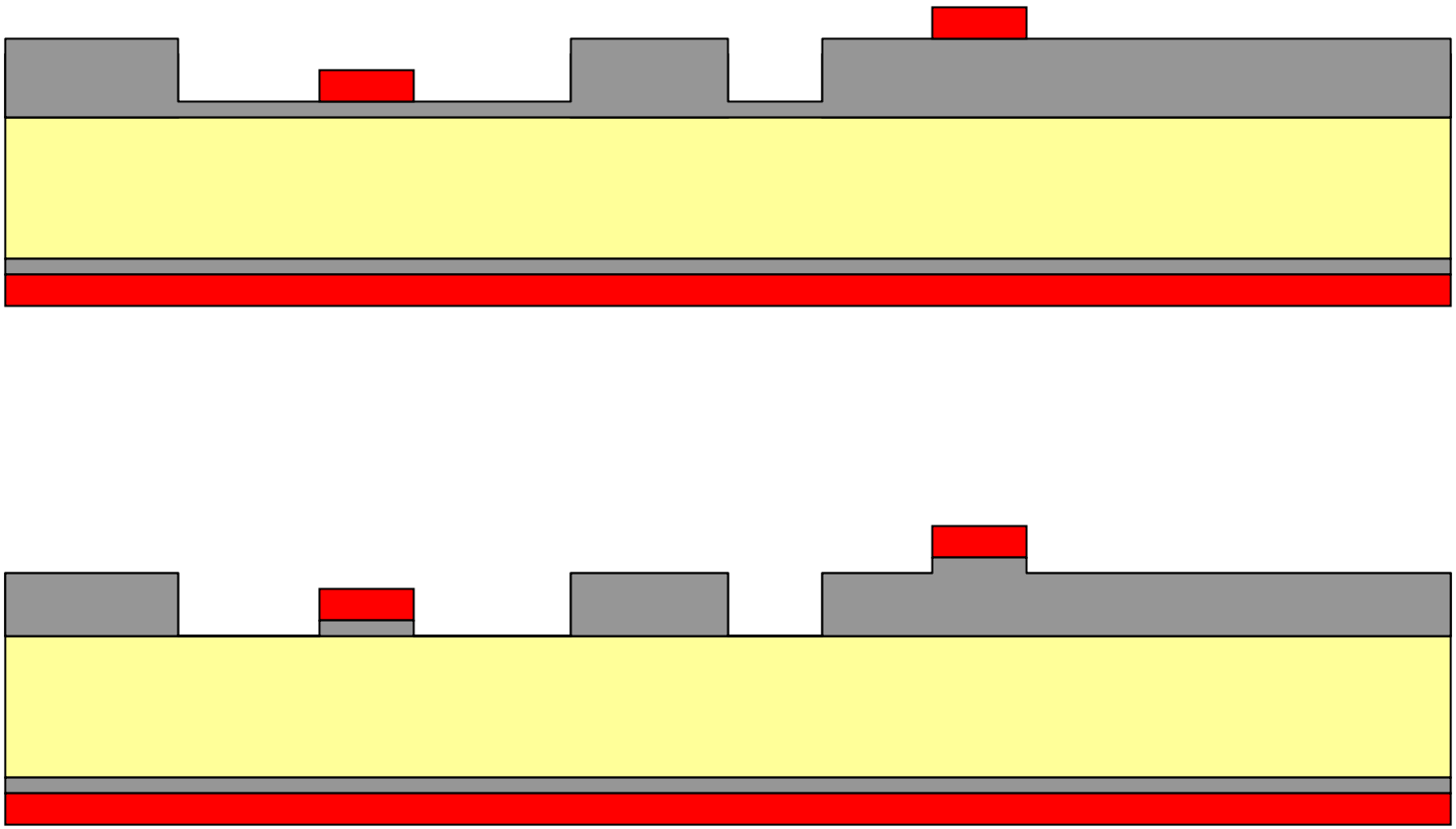
Process Steps

6. Pattern Polysilicon (Mask #2)



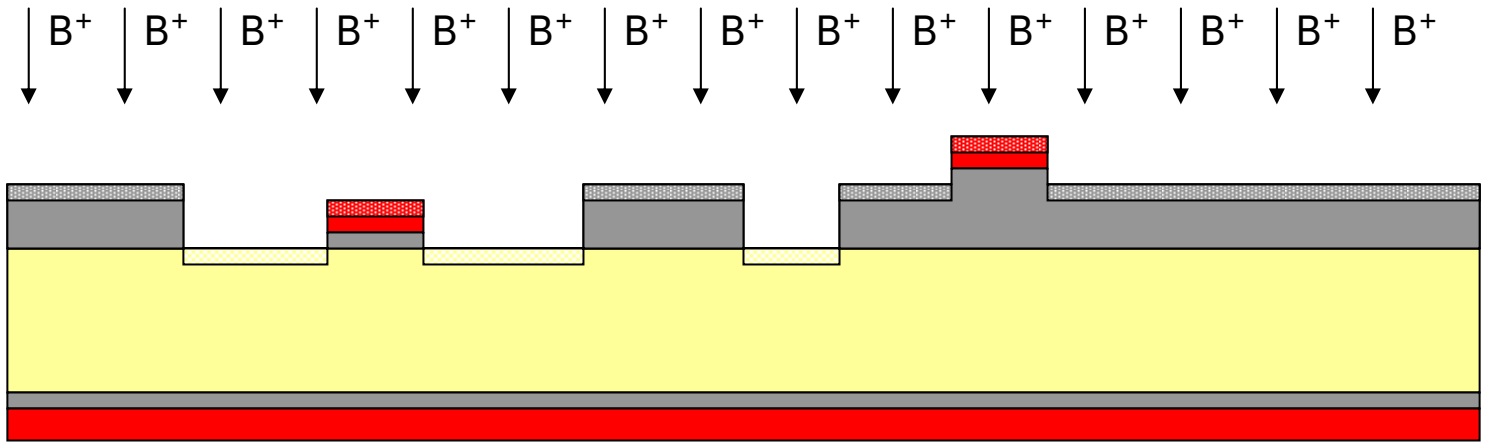
Process Steps

7. Etch Gate Oxide

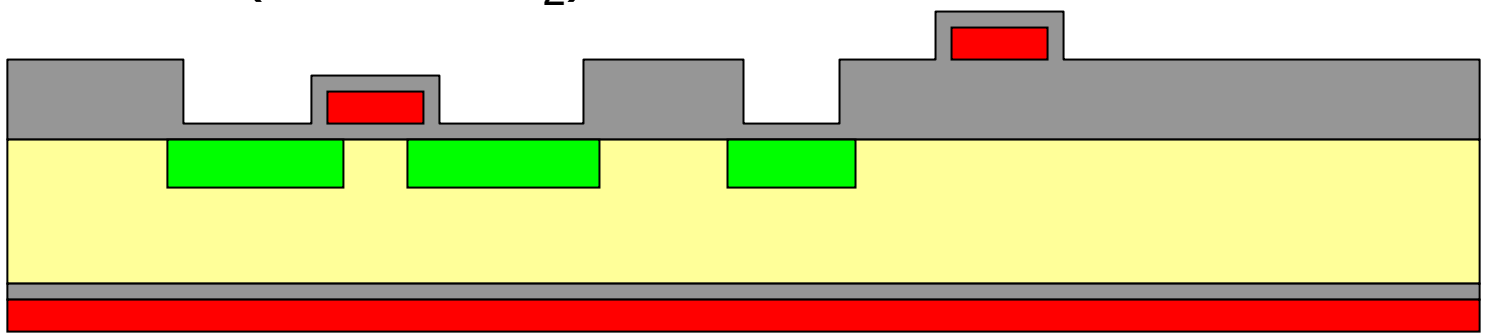


Process Steps

8. Ion Implantation of Boron



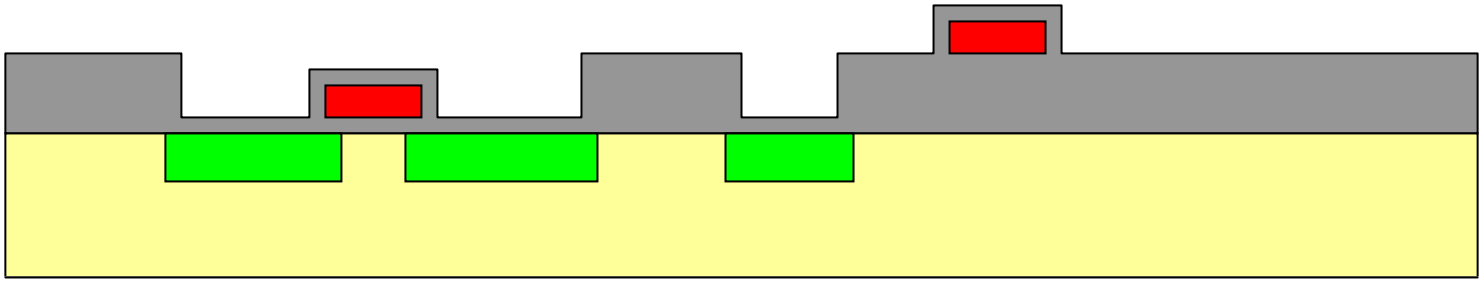
9. Drive-In (950C in O_2)



Note self alignment

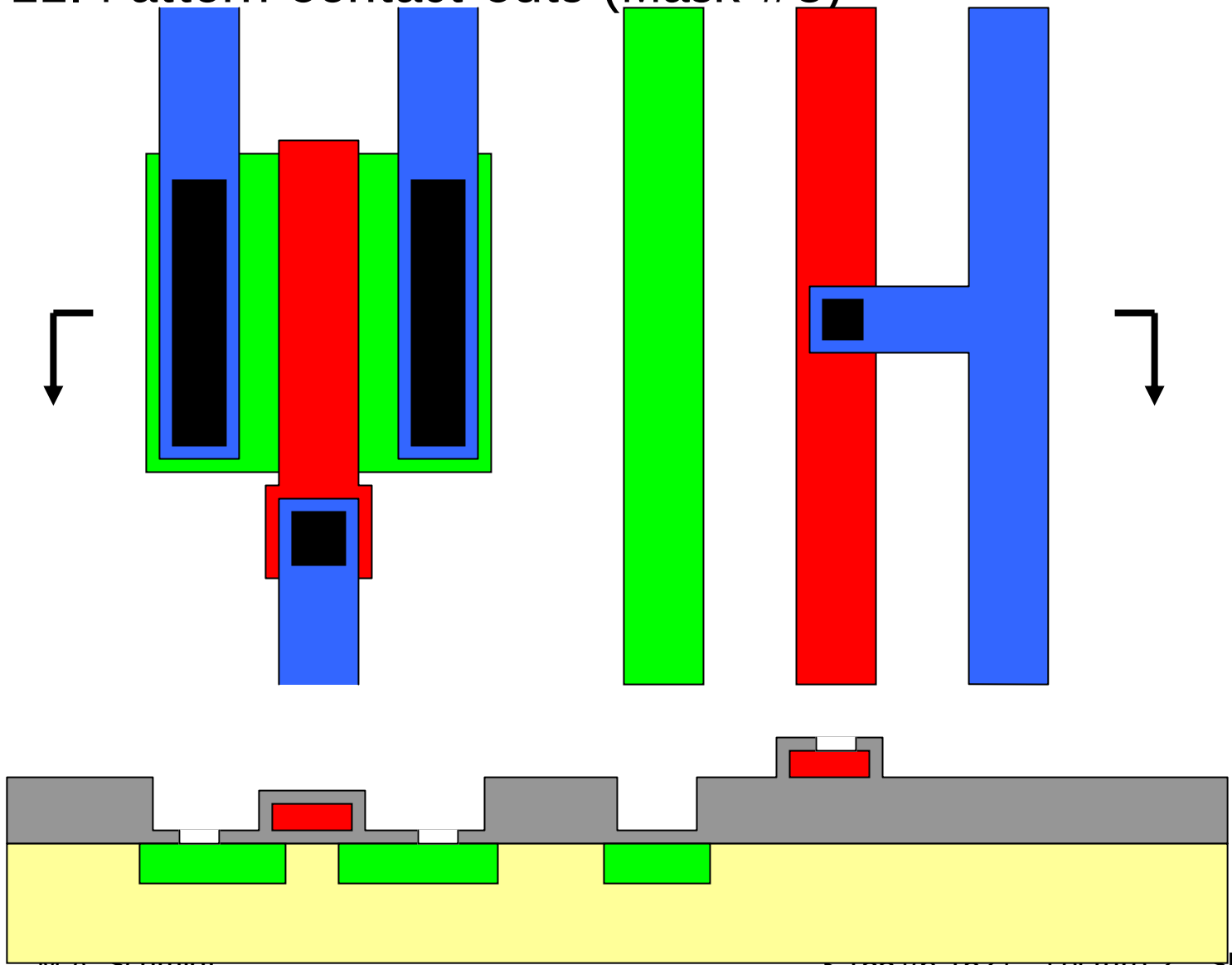
Process Steps

10. Strip Backside



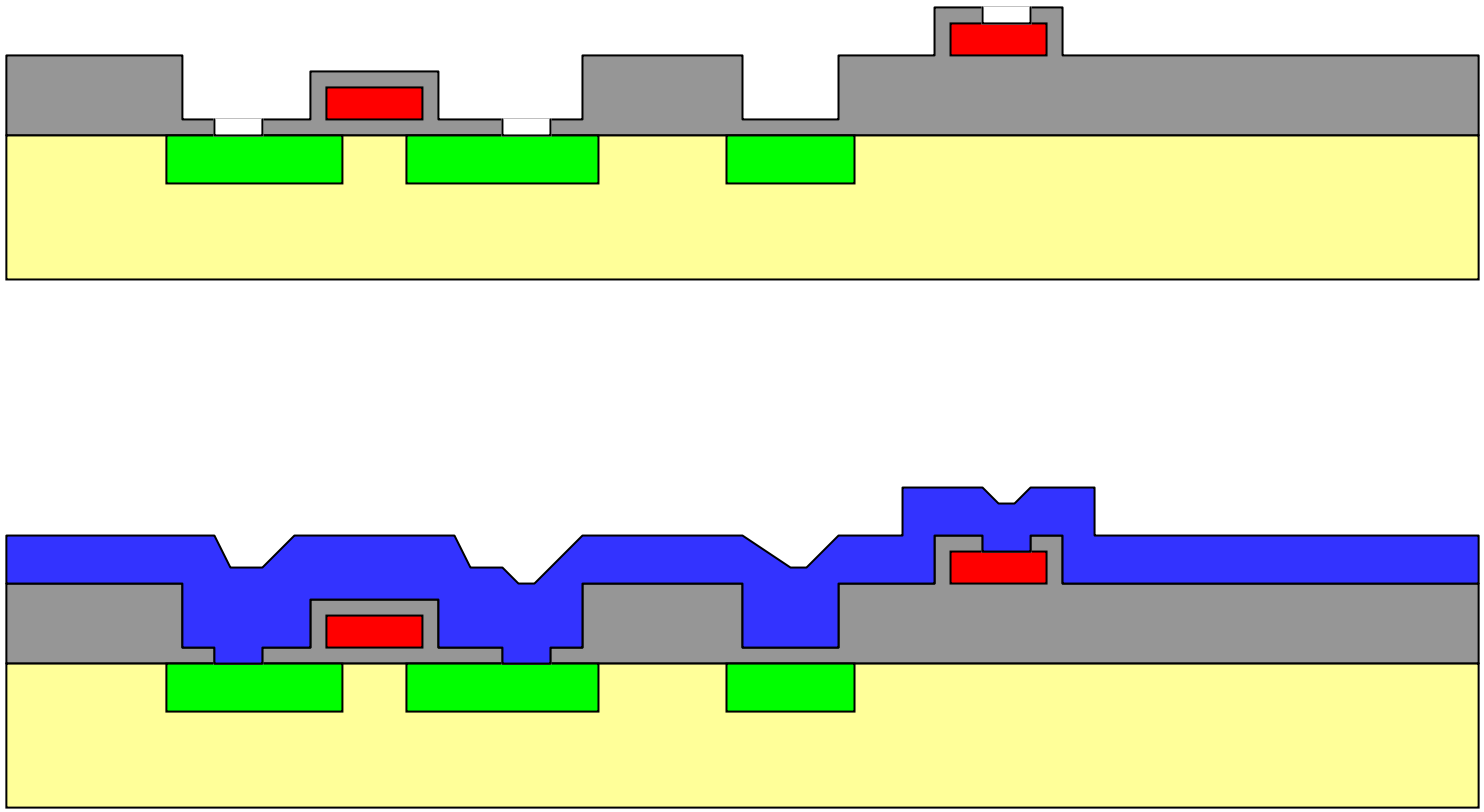
Process Steps

11. Pattern Contact Cuts (Mask #3)



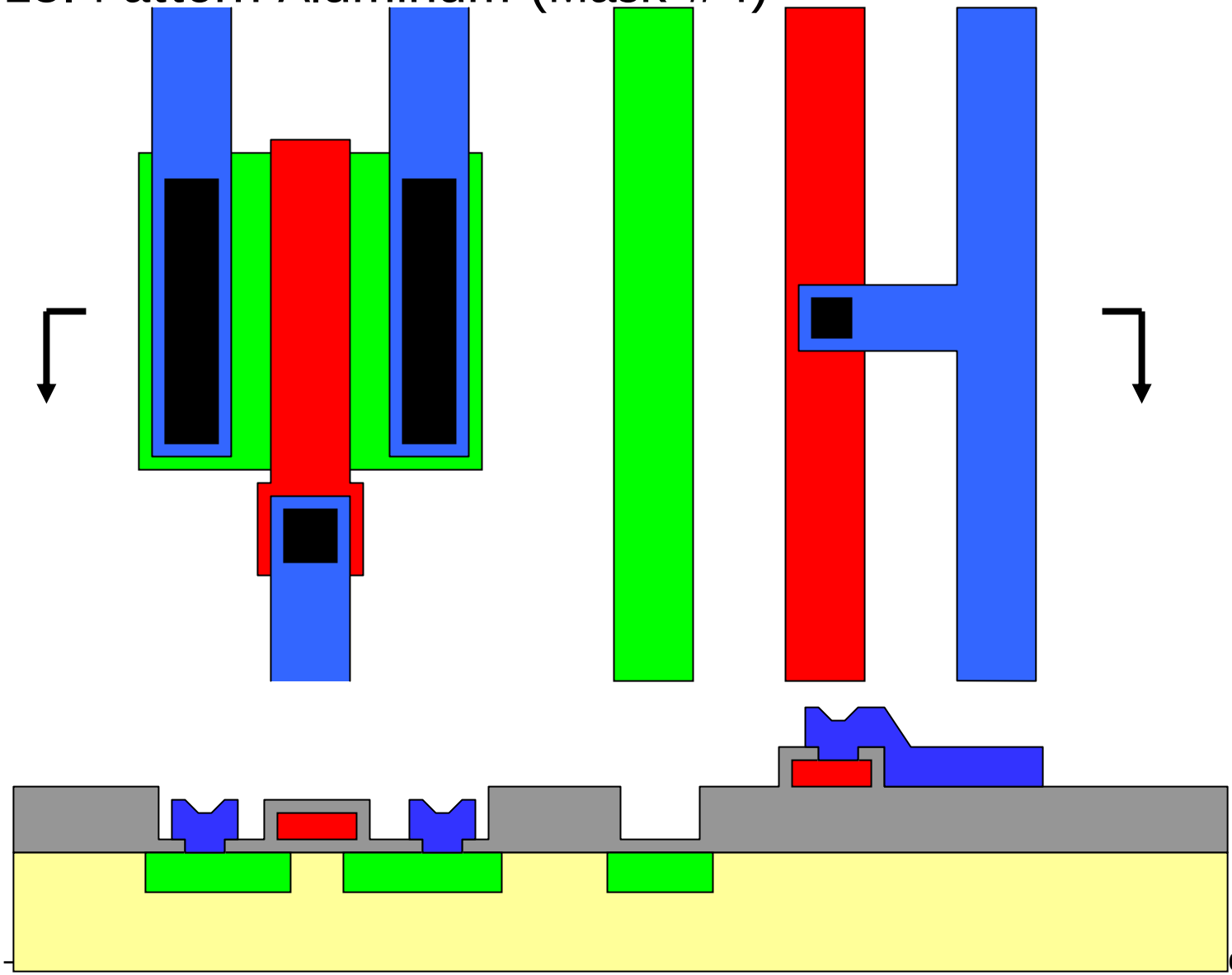
Process Steps

12. Evaporate Aluminum



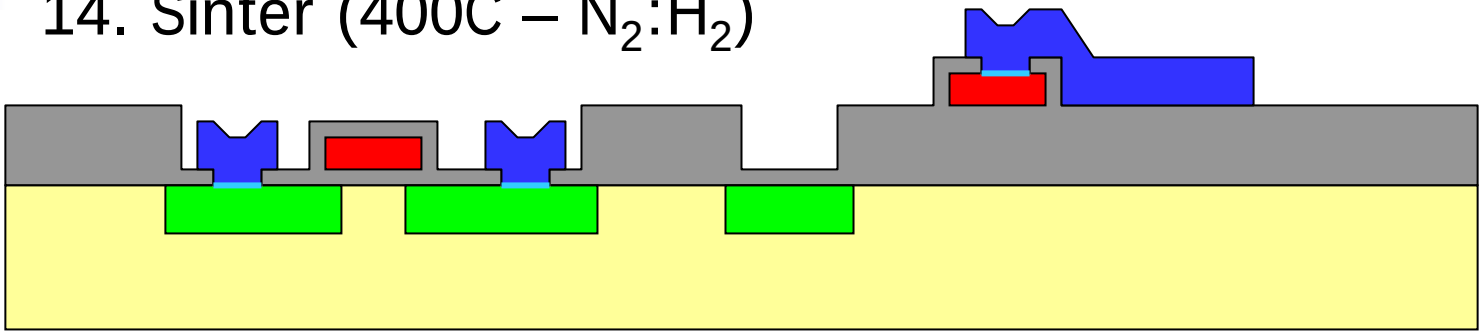
Process Steps

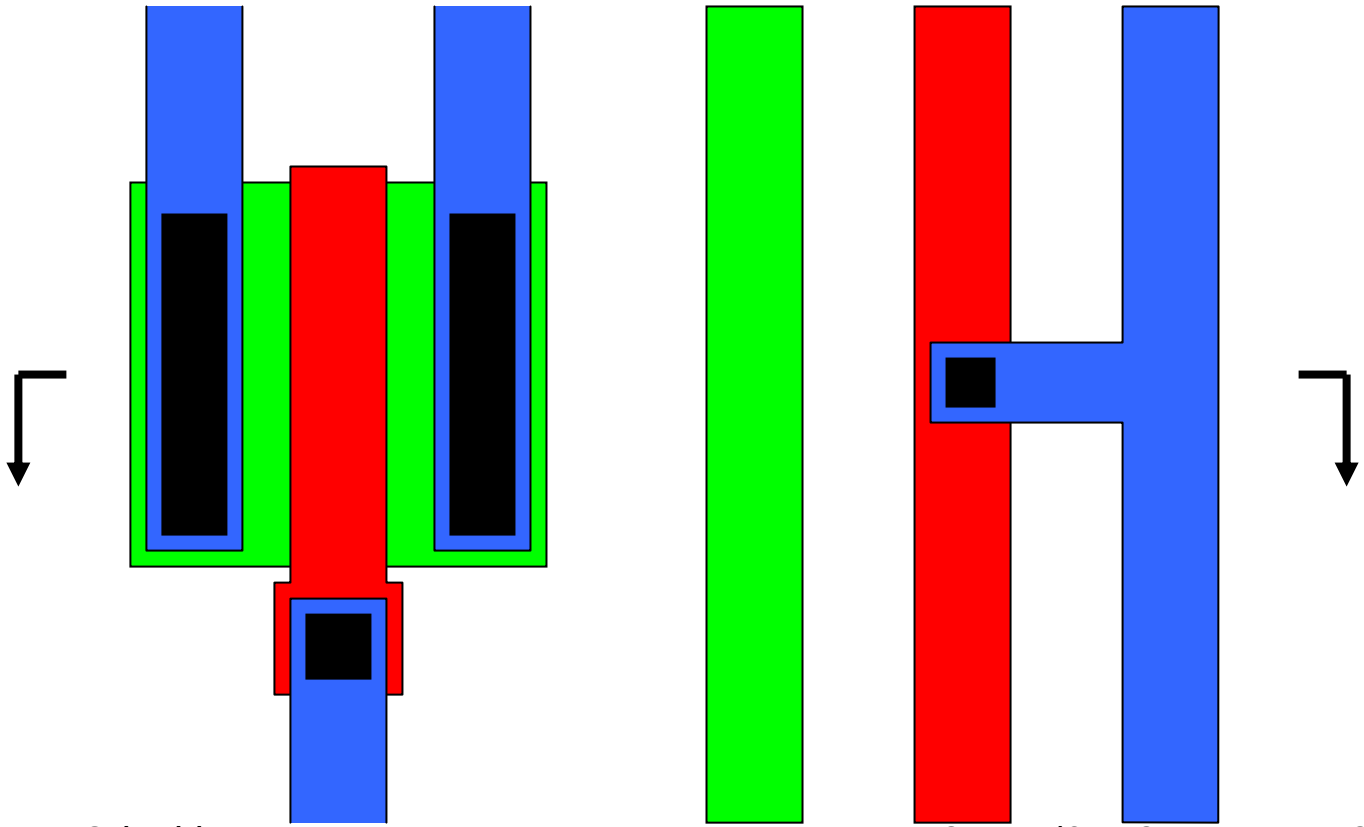
13. Pattern Aluminum (Mask #4)



Process Steps

14. Sinter (400C – N_2:H_2)





Process Results

- The Four Mask Process Yields
  - Resistors
    - Metal
    - Polysilicon
    - Diffusion
  - Capacitors
    - Metal-Silicon
    - Metal-Polysilicon
    - Polysilicon-Silicon
      - Gate Oxide
      - Field Oxide
  - Diode
  - MOSFET
  - Bipolar Junction Transistor (low quality)