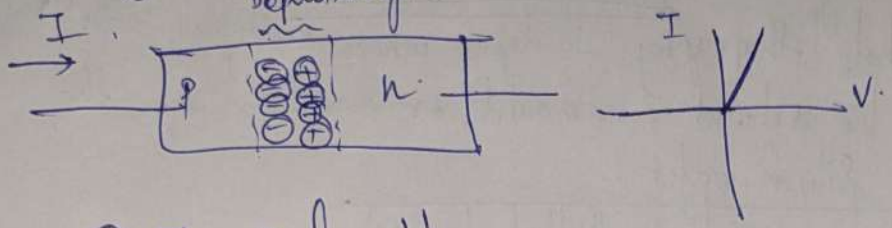
Semiconductor Fabrication - 101

Week 1

① Depletion Region



② Tap Analogy!!
(Mosfet as a switch)

③ Microfab:
- Starting material : Single crystal silicon (defect free bar). extremely pure.
- Mask Set :
- Process sequence :
  - gives 2-direc info.
    - shows how layers are built, etched or deposited step by step in depth.
  - defines x-y patterns that will be transferred onto silicon. each mask corresponds to one lithography step in the process.

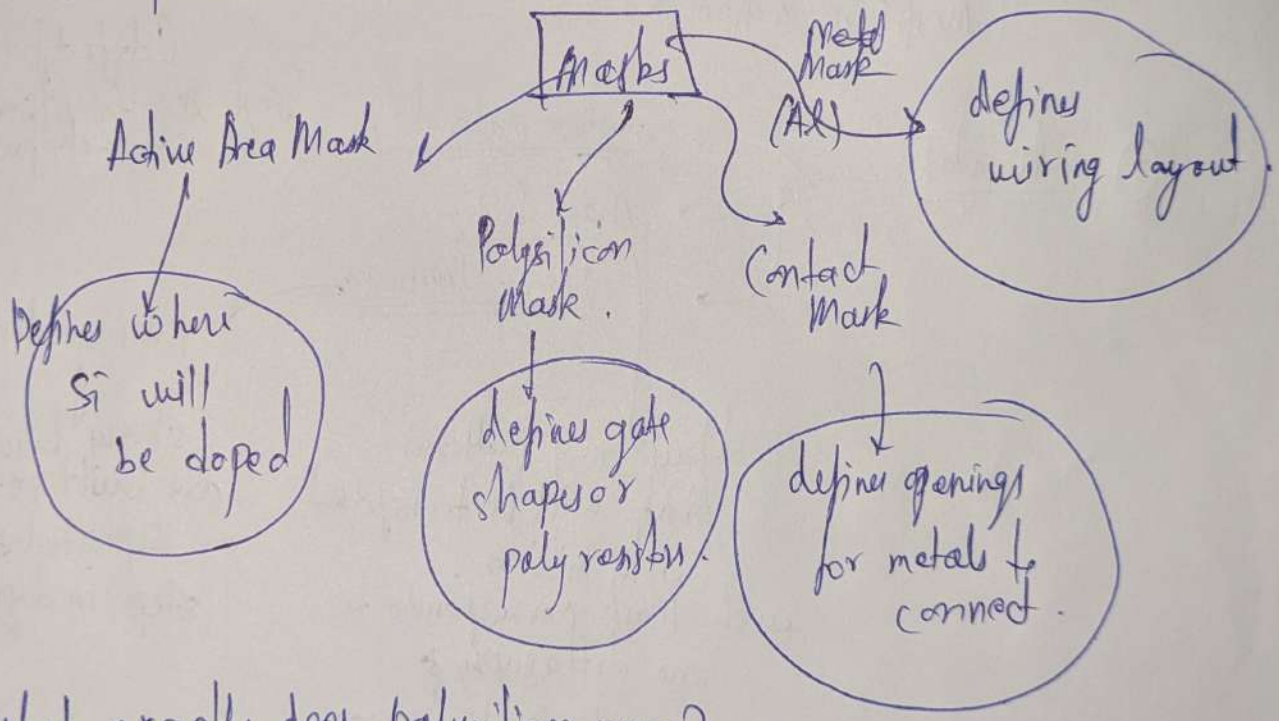
④ Counter doping :- introducing impurities of opposite type (eg n-type into p-type)

→ ~~you~~ one might use it to compensate for unintended doping.

⑤ Annealing → the heat treatment ~~used~~ for materials that soften them, reduces hardness & increases ductility by heating, holding & then cooling the material. This 'reorganizes' the material's internal structure, easier to work with

Masks:- They are stencil-like patterns used during photolithography to define where material should be added, removed or modified on the silicon wafer.

Each mask:- one layer of that device



What exactly does polysilicon mean?

→ Polycrystalline Silicon.

→ Small randomly oriented crystals fused together. Contrasting with single-crystal silicon (monocrystalline).

→ Extremely high purity.

→ Chip fabrication is like drawing shapes layer by layer on wafer

6-inch si wafer lightly doped n-type.

↓

Heating wafer in O_2 so that oxide forms on top.

↓

Pattern Active Area (Mask 1)

(Coat, expose, develop, etch) green area. (active area)

- coat: covers wafer with photoresist
- expose: place mask 1 & shine UV through mask 1 → those places photoresist: soluble
- develop: soluble photoresist washed away since soluble!
- etch: the oxide where mask wanted

Expose Si only in place where transistors exist, everywhere else → covered by oxide

↓

Grow gate oxide

↓

Deposit Polysilicon.

↓

Pattern Polysilicon (Mask 2)

↓

Etch gate oxide.

↓

Implant Boron

↓

Drive in.

↓

Strip Backside.

↓

(Mask 3). Pattern Contact Cuts

↓

Evaporate Al

↑

Pattern Al (Mask 4)

↑

Sinter

Green :- for transistors

Red :- make the gate

Ion implantn :- make source / drain aligned to gate

Black :- open holes for connections

Blue :- metal wiring later connects everything

with just 4 masks → the fab process can create all fundamental circuit components : resistors, caps, diode, Mosfets (even BJTs!

TEL Keypoints (General Reading material)

① CN: CarbonNanotube → diameter : nanoscale.
can be single walled or even nested multi walled.
→ exceptional tensile strength & thermal conductivity.

② ~~Integral~~ IC : combines all parts onto a single substrate or chip.

③ Kilby's groundbreaking idea! : father of IC in a way.
@ TI

④ Moore's Law :- no. of transistors will double every 18 months.

⑤ Microprocessor :- CPU on a chip.

⑥ Semiconductor memory devices → RAM → DRAM, SRAM
→ ROM

I have already spent hours on these concepts while studying for NEC

⑦ Liquid crystal (New)!

→ properties of both solids & liquids.

→ Cholesteryl benzoate (flowing crystal) (liquid crystal)
below! → melting pts (MP1 & MP2 & in btw the two
anisotropy (optical property)

As you ~~apply~~ voltage (change voltage) → ~~ori~~ orientn of LC molecules change. (transparency changes)

Thin film transistors (compos" from amorphous silicon)

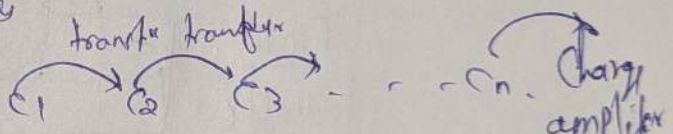
used to make LCD (Liquid Crystal Displays)

{ 'TFTs' are special kinds of 'FETs' made by 'thin film depos" process. substrate → generally glass. { unlike mosfet in which substrate → Si wafer } }

(*) Image Sensors (2 kinds mentioned)

CCDs: charged couple devices

light intensity → charge stored from a pixel



CMOS sensors use less power than CCD ones.

↓ large circuitry on smaller areas (also lower cost)! (*)

(*) GaAs:- truly a goat but Si wins because lesser expensive!

Doping

n^-, p^- → light doping
n, p → Normal doping
n^+, p^+ → Heavy Doping

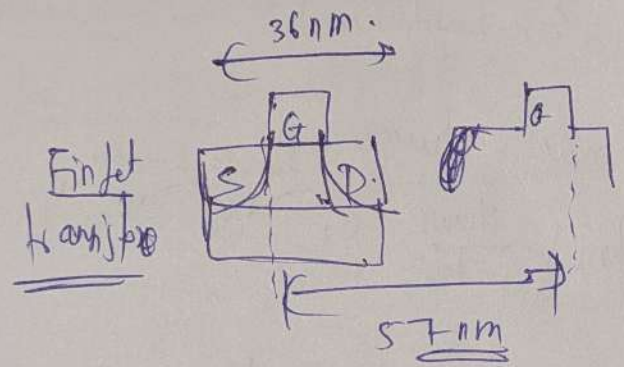
① Ion Implementation * my favourite
② Wafer growth doping.
③ Diffusion

→ Methods of doping

Fab

Cleanroom

Die → Another name for chip?



Oxide deposition → Photoresist spin coat → Photolithography (UV Light thing) → Photoresist development

→ Etching (oxide removal where wanted)

→ Photoresist Removal.

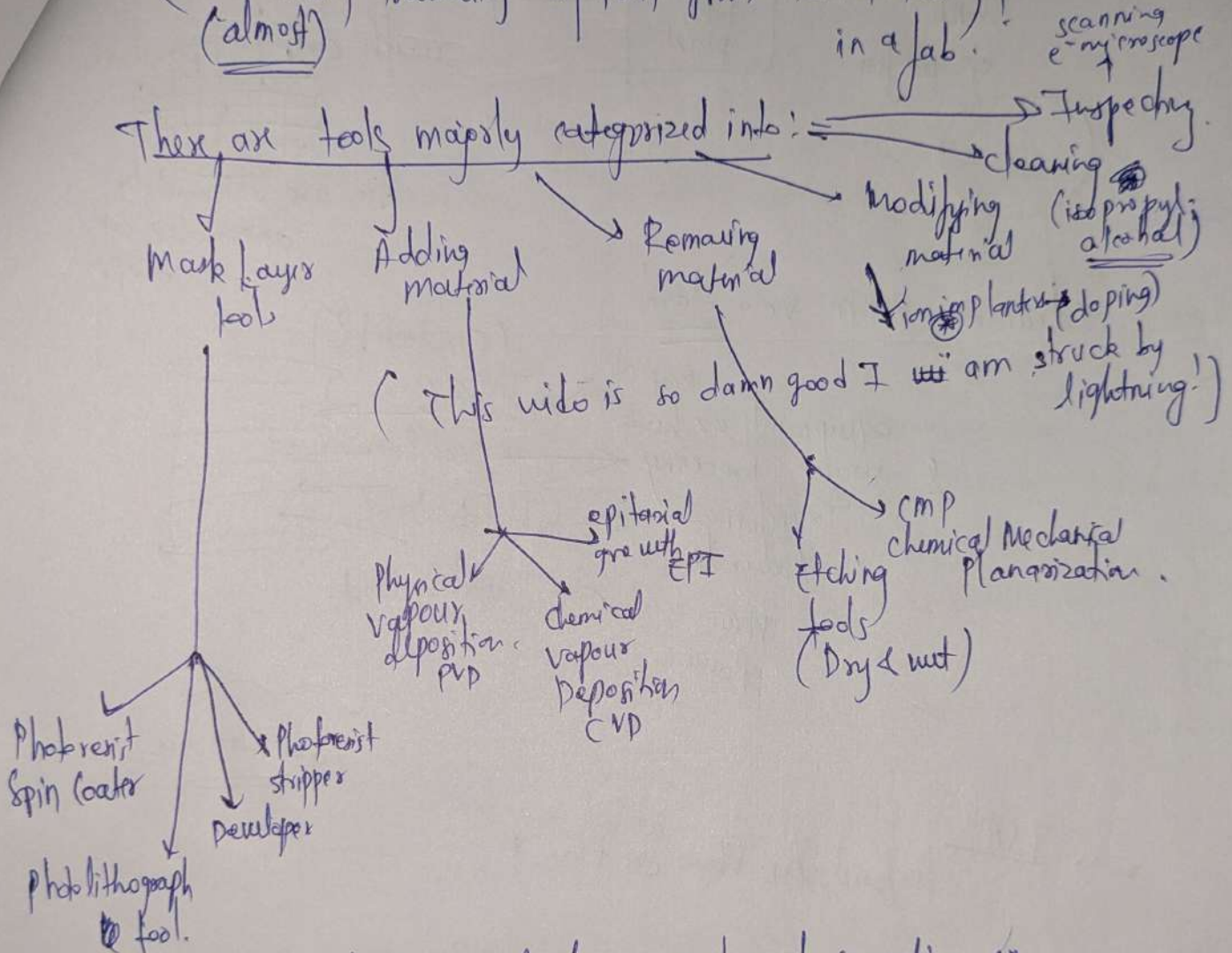
→ metal deposition (on areas just etched away)

→ Wafer Planarization

for building a single layer → repeated again for another layer (just a different ~~mask~~ (pattern) mask)

FOUP - Front Opening Universal Pod
↳ carries silicon wafers in batches/groups of ~25 (say)

(3 months of travelling of FOUP from tool to tool) (almost)! in a fab.



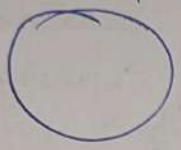
Semiconductor industry: extremely secretive ☹

Note:- Metrology devices
(Inspectory devices)
like diagnosis (not useful)
just give confidence
to stay & keep
moving.

SemiX Talk Lec # on Fab Functioning

Tata is → fab plant in Gujarat!

'Blank' Si wafer → [Fab plant.] → Processed Si wafer with die



die are ultimately assembled as chips.

cleaning room very 'clean'

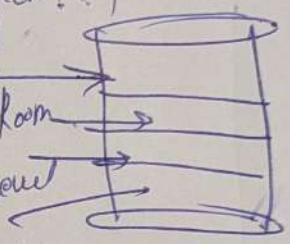
(Fan deck!?)

keep air clean → Interstitial level

equipments & wafer processing ← Clean room

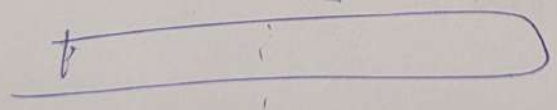
Transformers, Power line. ← Sub-Fab level

main Power ← Utility level.

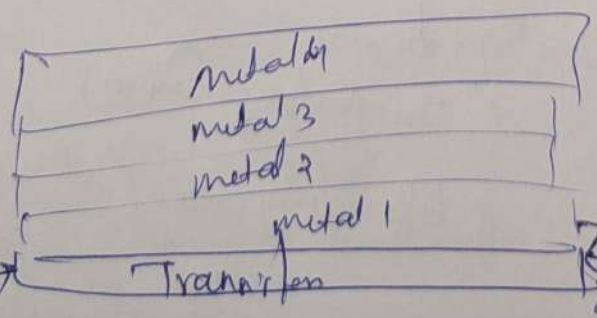


Fab Structure

→ ISMC Perfect Air Flow at on Flow!



All these → floors metal interconnects.



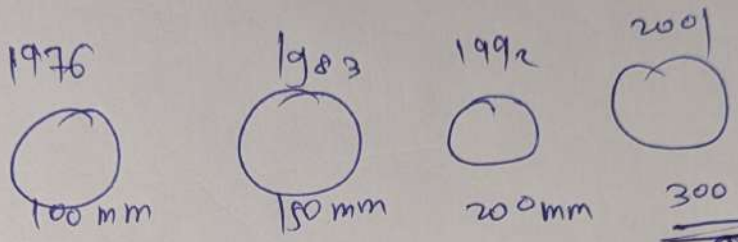
Metal to metal connection → Vias

Metal 1 to transistor connection → contacts

Wafer & Feature size

As wafer size ↑es : economic boom (you'll get 2.25 times more chips per wafer)

Understandable



After 2001 hasn't ↑ed :.

~~Feature~~ Feature size - ⊛ minimum dimension of a transistor that can be manufactured on a chip. The lesser it is → more advanced the tech

Tata → will be capable of 28nm

Chip war :- Chris Miller Do Read !!

Failing fast ! ⊛better ! & changing path & doing the right thing !

⊛ fundamentally understand semiconductors & then become an Entrepreneur !