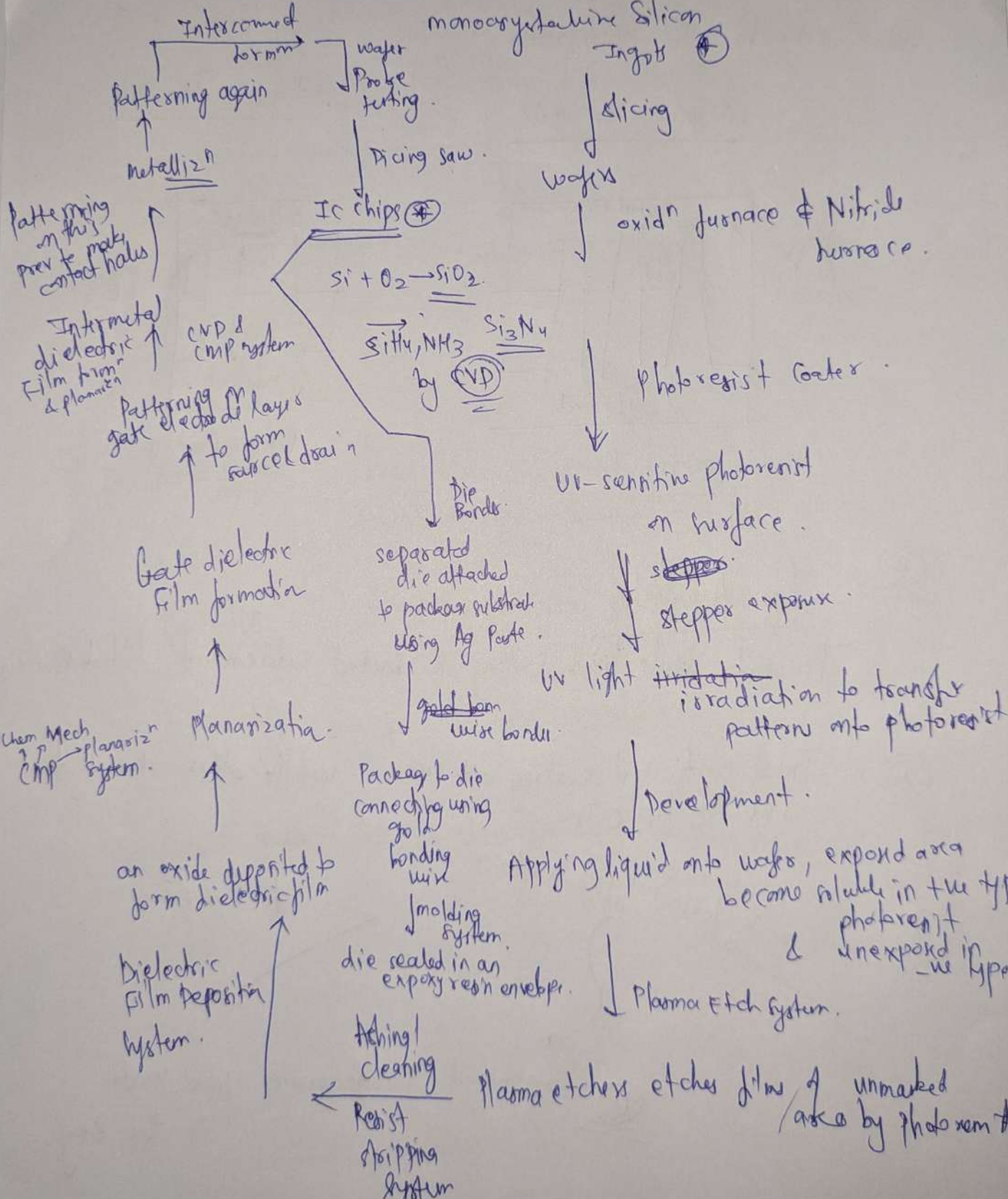
Fab 101 → week 2

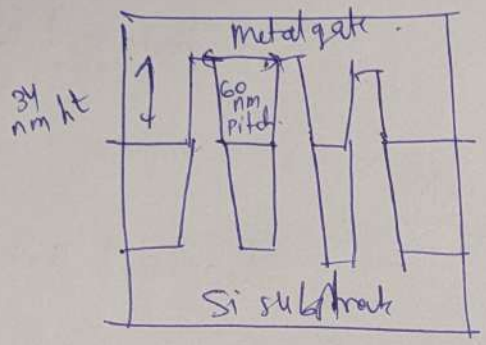
(1) Complete Process Demonstration :-



Node Scaling (contain ideas only)

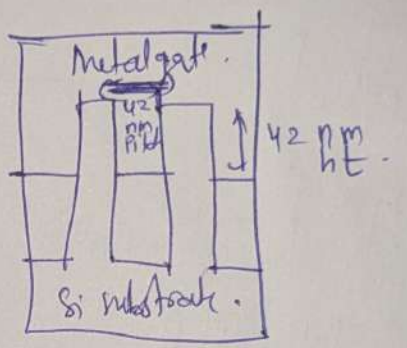
- Intel's 14 nm Tri Gate Transistor
- Transistor fin optimization.

1st gen^n Tri-gate



22 nm Process

2nd gen^n Tri-gate



14 nm Process

- Logic Area Scaling

Transistor Gate Pitch scaling & metal interconnect Pitch scaling

- Intel continued scaling at 14nm while other pause to develop FinFETs.
- Performance per watt.

Active power.

Improved Performance per watt is the key.

Lec0

① Process: fabricn with smaller dimension
② Structure:- new design for greater performance.
③ Feature size:- smallest dimension in device

Δ many things (history + overview)

Lec1

Si wafer manufacturing : too deep
note in book
& key concepts.

Lec2

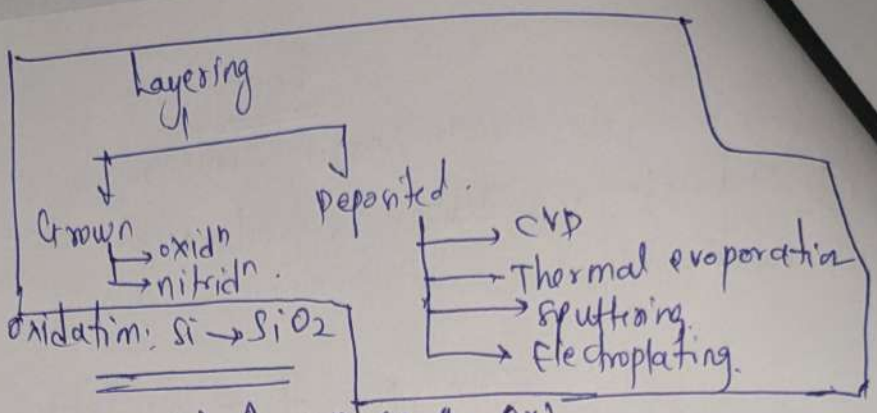
Device Manufacturing

Scribe lines :- Area blw different dies (chips) on a wafer. Blank or some additional test circuits.

Test die :- dies for electrical testing.

Edge chips :- partial dies at edge

Basic Wafer Fab operation → Layering
→ Patterning.
→ Doping
→ Heat Treatment.



In Grown :- underlying Si is consumed.

(eg) oxidation: $Si \rightarrow SiO_2$

$Si + O_2(g) \xrightarrow{\Delta} SiO_2(g)$ (dry ox).

$Si + H_2O(g) \xrightarrow{\Delta} SiO_2(g) + 2H_2$ (wet ox)

In Deposited :- underlying Si not consumed.

Epitaxial growth using CVD (chemical vapour deposition)

- homo-epitaxial → same matl.
- hetero-epitaxial → diff matl.

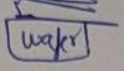
$SiCl_4(g) + 2H_2(g) \rightarrow Si(s) + 4HCl(g)$ → homo-epitaxy using CVD.

MBE → molecular beam epitaxy — GaAs → Ga source, As source.

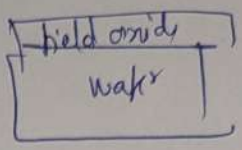
Doping :-
- by thermal diffusion (dopant are delivered to wafer surface at high temp)
- by Ion Implantation. (wafer @ RT :- Implantation & high energy ions annealing post implantation.

Example Fab process (imp)

(1) Base Si

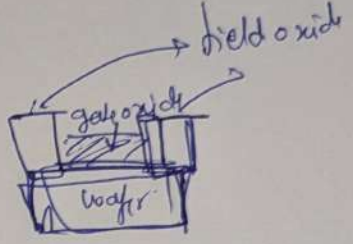


(2) Layering opening (to grow field oxide on Si)

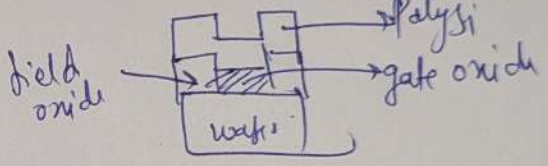


(3) Patterning step (create a hole in field oxide)

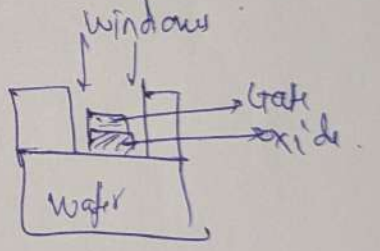
(4) Layering step — gate oxide is grown.



(5) Poly Si on top of oxide.

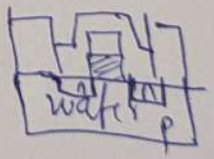


(6) Patterning → 2 openings for source & drain



(7) Doping → if n type dopes with p type & vice versa.

(8) Layering — oxide layer for patterning elec contacts

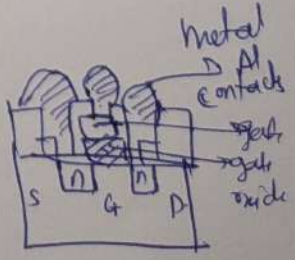


(9) Patterning — holes are opened in oxide for metal interconnects.

(10) Layering — Metal Al is deposited

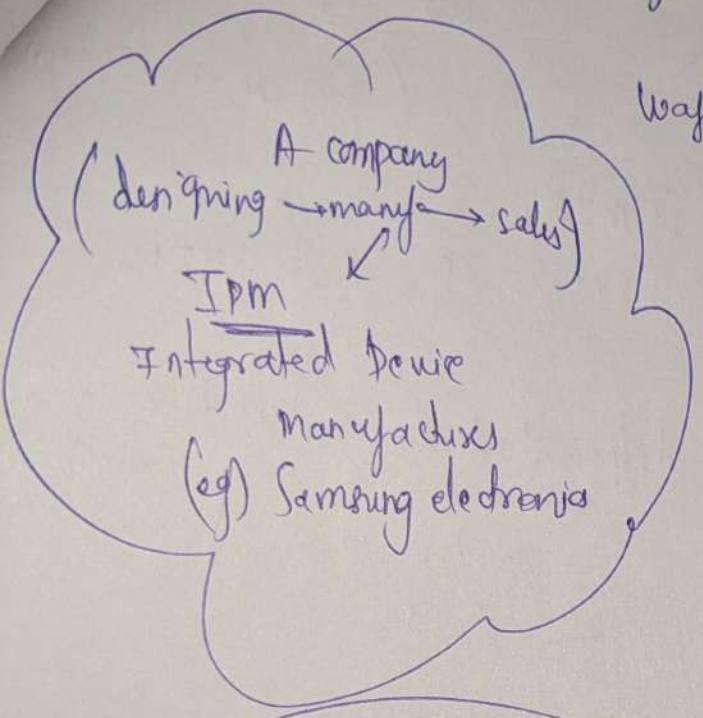
(11) Patterning → excess metal is removed.

(12) Heat treatment.

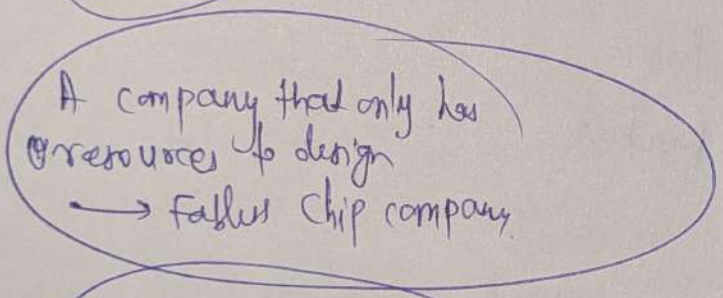


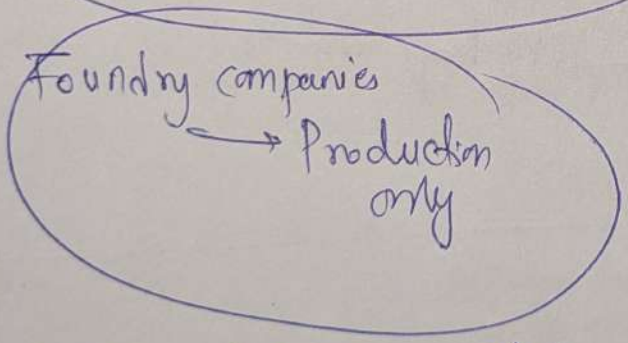
Glossary

⊛ Semiconductor ecosystem.



design
↓
Wafer manufacturing
↓
wafer dicing
↓
Packaging. (chips are attached on substrate)
↓
Shipping - (sales)





$$\text{Yield} = \frac{\text{Activating no. of chips}}{\text{max no. of chips}} \times 100\%$$

1 billionth of a metre → nano

Packaging (Intel again!)

* Adv package allow us to not just SOC. but SOP (System on Package)

* Intel's Haswell, Stratix 10. , EMIB, Feveros 3D, Co-EMIB.

In chip design :-
type of transistors for different tasks (like tiles in a home)

High Performance ⟶ CPUs.
High Density ⟶ GPUs.
low Power ⟶ SOC tile.
low Leakage ⟶ I/O Tile.

* After wafer assembly ⟶ Package assembly.