Winter Semiconductor School Fab 101

Assignment 2.

(Q1) Size of unit cell of Si is 0.54nm, how realistic is your prediction of size reduction? When do you predict the break down of Moore's Law?

→ According to Moore's law, no. of transistors on a chip doubles every 2 yrs, that implies a continuous shrinking of transistor.

Silicon lattice constant. ≃ 0.54 nm. (given).

Transistor gate length cannot be meaningfully smaller than 5–10 atomic spacings (~2–5 nm).

otherwise Quantum ~~Tunell~~ Tunneling. dominates.

Aggressive scaling below ~5nm is not physically realistic.

Moore's law breaks at atomic-scale limits (~1–2 nm) where silicon lattice physics dominates.

(Q2) Distinguish between Czochralski & float zone technique processes. Why do you think the float zone technique is harder to implement for larger wafers?

	Czochralski (CZ) Process	Float zone (FZ) process.
Crucible	Uses a quartz (SiO_2) crucible	Crucible-less, uses an induction coil.
Purity	Contains oxygen impurities from the crucible.	Extremely high purity, low oxygen/carbon.
Applicn	Std VLSI, microprocessors	High-power devices, detectors
Cost	Cheaper & supports very large diameters	More expensive & difficult to scale.

Why FZ is harder for large wafers?

1. Molten zone becomes gravitationally unstable.
2. Surface tension cannot support wide molten regions.
3. Mechanical sagging & breakage risks increase with diameter

FZ is limited by melt stability, making larger wafers impractical.

(Q3) Distinguish using chemical reactions, the two type of oxidation processes. Which one do you think would have faster rate & why?

→

silicon oxidⁿ types

Dry oxidation

$$Si + O_2 \rightarrow SiO_2.$$

Slower growth rate.
High quality, dense oxide.
used for gate oxides.

wet oxidation.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2.$$

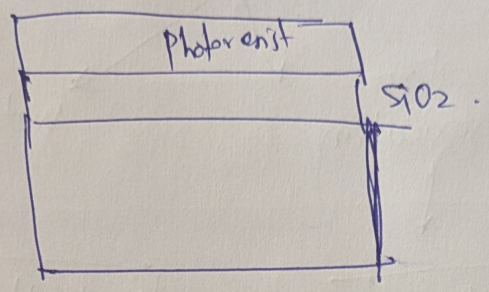
Faster growth rate.
lower oxide density.
Used for field oxides

↓

faster
Because H_2O diffuse faster through SiO_2 than O_2.
(H_2O is smaller than the larger O_2 molecule)

(a) Bonus

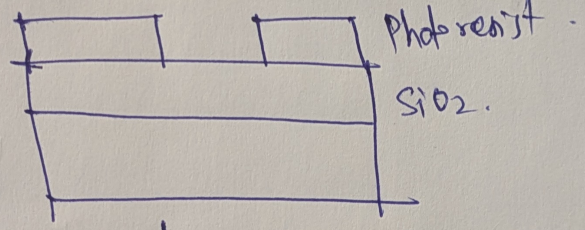
① start with
p-type silicon substrate.



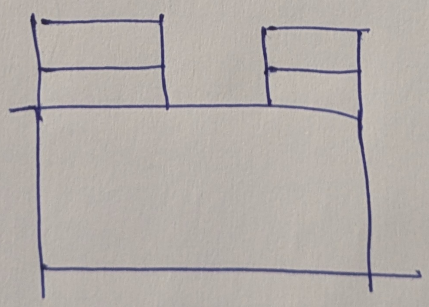
SiO_2 layer is grown on Si substrate & then Photoresist..

↓

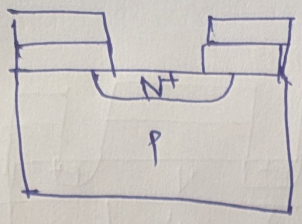
Mask 1



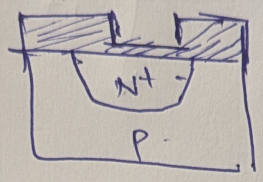
↓ Dry Etching (Remove SiO_2 in those places where it isn't protected by the Photoresist)



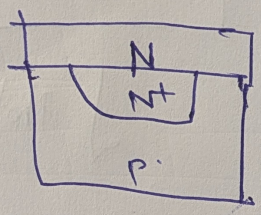
↓ N^+ implantation.



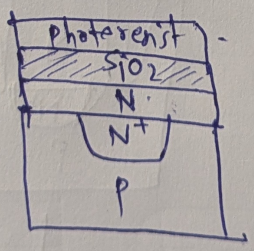
↓ Bury this N+ layer in a high temp furnace cycle.



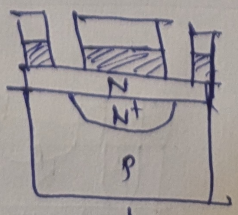
↓ etch out SiO_2 & grow an N type epitaxial layer



↓ SiO_2 is grown thermally & photoresist.

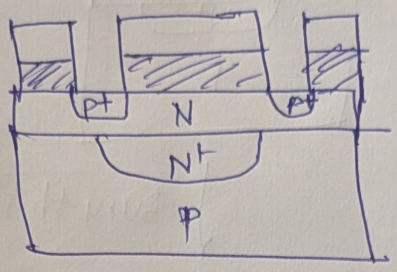


↓ mask 2 + (etching of SiO_2 in region where photoresist is not there).

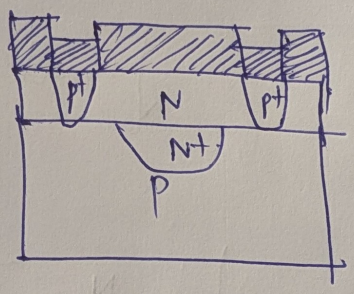


↓

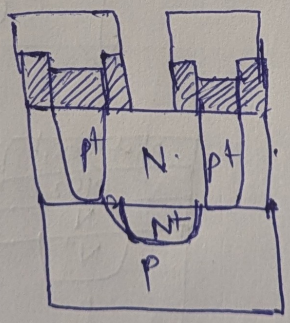
↓ P type implantation.



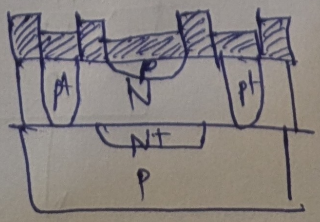
↓ p^+ regions are driven ~~to~~ into the P substrate. & SiO_2 is grown on the surface.



↓ Photoresist again & Mask 3 again for base region. + etching of SiO_2 in that region in which photore is not there.

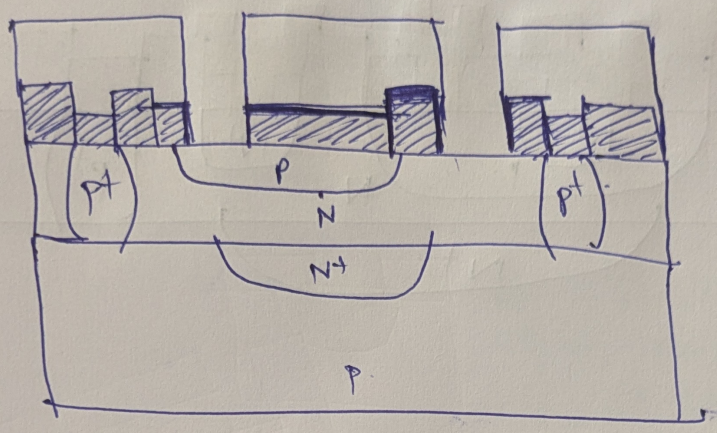


↓ P implantation in base region & SiO_2 grown again to cover it

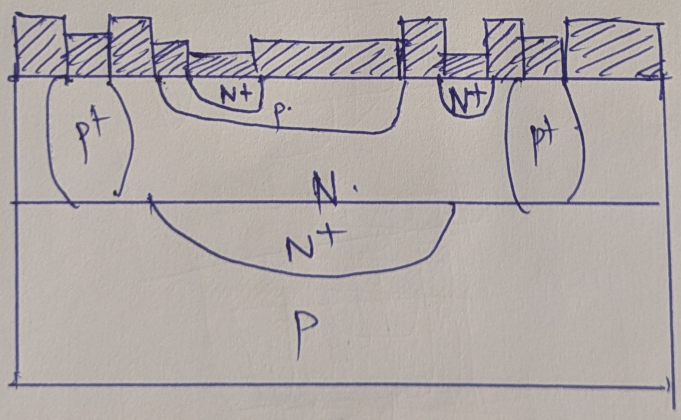


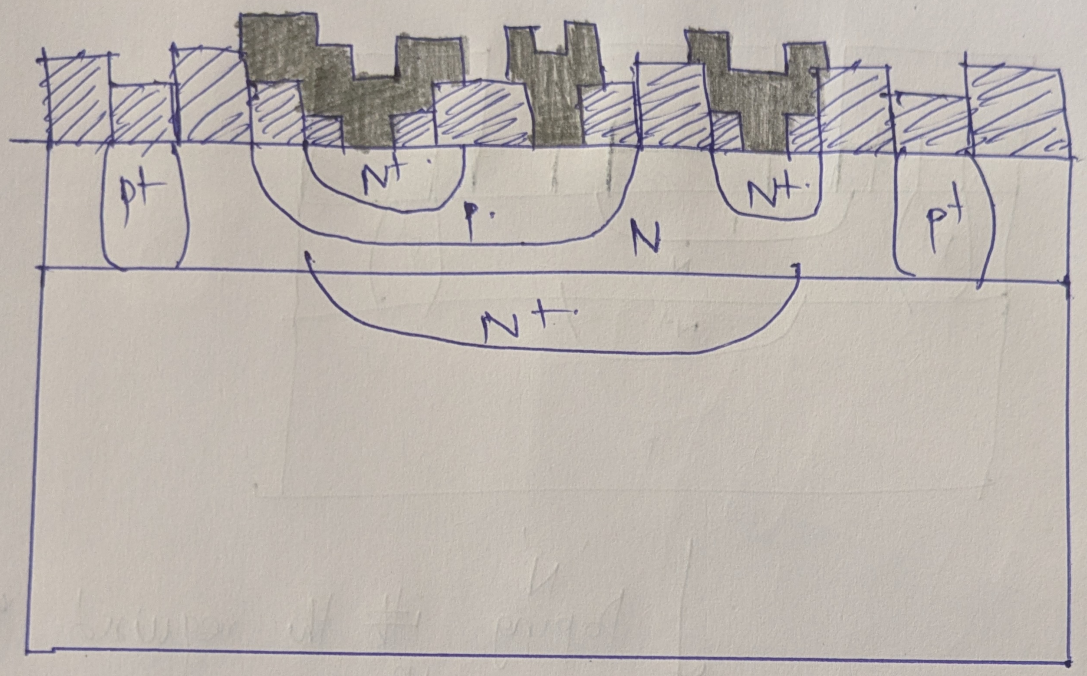
(for emitter collector regions)

Photo resist again on SiO_2
then Mask 4 then etch SiO_2
in those regions where Photo resist is not there.



↓ 'N' Doping ~~in~~ in the required regions.
& after that SiO_2 all again on the surface.



↓ Photoresist then mask 5 (contact regions) etch SiO_2 → deposit Al → Photoresist again → mask 6 (wiring regions) → etch Al. & remove Photoresist.

final