EE719: Mixed Signal VLSI Design

Assignment 3 (Spring 2025–26)

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Technology Parameters

All designs and calculations are carried out for a 130 nm CMOS process with the following parameters:

- $V_{DD} = 1.5$ V, ; $V_{SS} = 0$ V
- $V_{THn} = |V_{TP}| = 0.4$ V
- $\mu_n C_{ox} = 140\ \mu$A/V^2
- $\mu_p C_{ox} = 120\ \mu$A/V^2

1 Question 1: Choice of Sampling Switch

The suitability of a MOS sampling switch is determined by whether it can remain in strong inversion over the full input signal swing.

(a) $V_{in}(t) = 0.55 + 0.25\sin(\omega t)$

$$V_{in,\min} = 0.30 \text{ V}, \qquad V_{in,\max} = 0.80 \text{ V}$$

An NMOS switch conducts well for low-to-mid input voltages. Since $V_{in,\max} < V_{DD} - V_{THn} = 1.1$ V, the NMOS remains in strong inversion throughout the signal swing.

Chosen switch: NMOS

(b) $V_{in}(t) = 0.85 + 0.35\sin(\omega t)$

$$V_{in,\min} = 0.50 \text{ V}, \qquad V_{in,\max} = 1.20 \text{ V}$$

Near the upper end of the swing, an NMOS suffers from threshold voltage drop, while a PMOS provides lower resistance for high input levels. Thus a PMOS switch is better suited.

Chosen switch: PMOS

(c) $V_{in}(t) = 0.8 + 0.5\sin(\omega t)$

$$V_{in,\min} = 0.30 \text{ V}, \qquad V_{in,\max} = 1.30 \text{ V}$$

The signal spans almost the full supply range. Neither NMOS nor PMOS alone can provide uniform low resistance. A complementary transmission gate ensures rail-to-rail operation.

Chosen switch: Complementary (Transmission Gate)

2 Question 2: NMOS Track-and-Hold Design

Given:

- Sampling frequency $f_s = 10$ MHz, duty cycle = 50
- Track time $T_{track} = \frac{1}{2f_s} = 50$ ns
- $C_H = 1.2$ pF (from roll number 24B1312)
- $V_{in} = 0$ V,; $V_{out}(0) = 1$ V

2.1 (a) Output during Track Phase

During tracking, the NMOS switch behaves as a resistor R_{on} charging/discharging C_H.

$$V_{out}(t) = V_{in} + \big(V_{out}(0) - V_{in}\big)e^{-t/(R_{on}C_H)}$$

$$V_{out}(t) = 1 \cdot e^{-t/(R_{on}C_H)}$$

You should draw by hand: exponential decay of $V_{out}(t)$ from 1 V to 0 V, marking the time constant $\tau = R_{on}C_H$.

2.2 (b) Switch Sizing (Worst-Case Analysis)

The steady-state tracking error must satisfy:

$$|V_{error}| = V_{out}(T_{track}) \leq 5 \text{ mV}$$

$$e^{-T_{track}/(R_{on}C_H)} \leq 0.005$$

$$R_{on}C_H \leq \frac{T_{track}}{\ln(1/0.005)} \approx 9.4 \text{ ns}$$

$$R_{on} \leq \frac{9.4 \text{ ns}}{1.2 \text{ pF}} \approx 7.8 \text{ k}\Omega$$

For an NMOS in linear region:

$$R_{on} = \frac{1}{\mu_n C_{ox}(W/L)(V_{GS} - V_{TH})}$$

Worst case $V_{GS} = 1.5$ V:

$$W/L \geq \frac{1}{R_{on}\mu_n C_{ox}(1.1)} \approx 8.3$$

Chosen aspect ratio: $W/L \approx 10$ **(with margin).**

2.3 (c) Switch Delay

The delay is approximated by the time constant:

$$\tau = R_{on}C_H \approx 7.8\ \text{k}\Omega \times 1.2\ \text{pF} \approx 9.4\ \text{ns}$$

3 Question 3: PMOS Track-and-Hold Circuit

3.1 (A) Input Signal Constraints

Given $V_{in,\min} = 0.5$ V and $V_{DD} = 1.5$ V:

$$V_{CM} = \frac{V_{max} + V_{min}}{2} = 1.0\ \text{V}$$

$$V_{max} = 1.5\ \text{V}$$

Peak-to-peak sinusoidal swing:

$$V_{pp} = 2(V_{max} - V_{CM}) = 1.0\ \text{V}$$

3.2 (B) Switch Resistance

For PMOS:

$$R_{on,min} = \frac{1}{\mu_p C_{ox}(W/L)(V_{SG} - |V_{TP}|)}$$

With $W/L = 20$:

$$R_{on,min} \approx 2.5\ \text{k}\Omega$$

$$R_{on,max} = K \cdot R_{on,min} = 5 \times 2.5 = 12.5\ \text{k}\Omega$$

3.3 (C) Hold Capacitor from kT/C Noise

$$v_n^2 = \frac{kT}{C_H}$$

$$C_H \geq \frac{kT}{v_n^2} = \frac{1.38 \times 10^{-23} \times 300}{(100 \times 10^{-6})^2}$$

$$C_H \geq 0.41\ \text{pF}$$

Conclusion

All switches were selected and sized using worst-case analysis to ensure reliable tracking accuracy. Conservative margins were intentionally used to reflect practical analog design methodology.