

$$\textcircled{1} \quad \begin{aligned} (\text{a}) (V_{in \max}) &= 0.8V \\ (V_{in \ min}) &= 0.3V \end{aligned}$$

Nmos → check $V_{in \ max}$
Pmos → check $V_{in \ min}$

Also, Nmos gate → V_{dd} .

maximum input voltage an Nmos can pass strongly :-

$$= V_{dd} - (V_{th})_n = 1.5 - 0.4 = 1.1V$$

Input signal never crosses this max input voltage that Nmos can pass strongly.

(see next page
more clarity)

$$(V_{in})_{\max} < V_{dd} - (V_{th})_n$$

Chosen switch: Nmos

Why with $(V_{in})_{\max}$?

→ Worst case (Nmos turns off) at maximum input

$$V_{GS} - (V_{th})_n > 0.$$

Gate → V_{DD}

Source → V_{in}

of course nmos is best at low voltages

∴ V_{in} is small & V_{GS} is large!

(Note:- Pmos would be needed if

$$V_{in \ max} \geq V_{PP} - (V_{th})_n$$

Cmos if

$$V_{in \ min} \ll$$

$$V_{in \ max} \approx V_{PP}$$

$$V_{in(t)} = 0.85 + 0.35 \sin(\omega t)$$

(b) Nmos clearly doesn't work → $V_{in \ max} > V_{dd} - (V_{th})_n$.

Check Pmos:- $(V_{in})_{\min} = 0.5V$ & $(V_{th})_p$ is $0.4V$

$$\therefore (V_{in})_{\min} > (V_{th})_p \quad \checkmark$$

Pmos in strong inversion as long as

$$V_{in, \ min} > |(V_{th})_p|$$

Cmos → we use if Nmos fails at high end & pmos at low end

(c)

$$V_{in}(t) = 0.8 + 0.5 \sin(\omega t)$$

$$(V_{in})_{min} = 0.3V$$

$$(V_{in})_{max} = 1.3V$$

Nmos

$$\textcircled{2} \quad V_{dd} - (V_{th})_n = 1.1V$$

PMOS

$$(V_{th})_p = 0.4V \rightarrow \text{fails}$$

Imp:-

Source & Drain \rightarrow dynamic of comp.

Nmos:- Source is lower voltage node

PMOS:- Source is higher voltage node

Max clarity

Imp Note:-

Smallest possible gate overdrive occurs when source is $(V_{in})_{max}$
bcz we are interested in least value of

$$\textcircled{3} \quad (V_{GS} - V_{th})_n > 0$$

drain voltage would be even higher of.c.

Worst Case

For PMOS :-

Note

$$V_{SG} - (V_{th})_p > 0.$$

So ~~for~~ ^{for} their to be min, -
LTS

$V_{source} \rightarrow \underline{\min}$

∴ Source is $(V_{in})_{min}$

Drain of pmos would be even
 $(V_{out}-cap)$ more smaller
at that time.