BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
First Semester 2003-2004

Course Title : OPERATING SYSTEMS **Course No *CS C372***
Component : Test II (Regular) ***Closed Book Component***
Weightage : 15% **Max Marks: 15** **Date : 25-11-2003**

SECTION I (1 X 5 = 5 Marks)

Q1. A system uses cache memory (Mc), Primary memory (Mp) and Disk as the secondary memory (Ms) to store byte data during execution. The time to access Mc is 5nS time to access Mp is 70nS and the time to access Ms (on average) is 5mS. If a probability of cache hit is 0.99 and residual probability of the data being in Mp is 0.9999 and the residual probability of data being in Ms is 1.00. Assume that the memory hierarchy is checked in the order Mc Mp Ms, what is the expected access time for a byte.

Q2. Does increasing the number of frames allocated always reduce the number of page faults for a page reference sequence? Explain with an example.

Q3. Consider the following processes, with the length of the CPU-burst time given in milliseconds:

Process	Arrival time	Burst time
P1	0	16
P2	14	6
P3	19	3
P4	20	1
P5	21	14

We use multi level feed back queue scheduling with 3 queues (Q0 to Q2). Q0 is having the highest priority (RR scheduling of 4 milliseconds) Q1 is the next highest (RR scheduling of 8 milliseconds) and Q3 is the least with FCFS scheduling. Every queue is preemptive (i.e. if the CPU is executing Q1 then any job came in Q0 it will be preempted.) Find Turn around time for individual process.

Q4. Find Average waiting time for Question 3.

Q5. We have 5 processes (P_0 through P_4) and 3 resource types *A* (10 instances), *B* (5instances), and *C* (7 instances). Snapshot at time T_0:

Process	Allocation			**Maximum**		
	A	B	C	**A**	**B**	**C**
P0	0	1	0	**7**	**5**	**3**
P1	3	0	2	**3**	**3**	**2**
P2	3	0	2	**9**	**0**	**2**
P3	2	1	1	**2**	**2**	**2**
P4	0	0	2	**4**	**3**	**3**

Find the safe sequence. A request for (3,3,0) by P4 is granted? If yes write down the safe sequence after granting the resources.

SECTION II (4 X 2.5 = 10 Marks)

Q1. A word addressable processor with 64 bit wide memory and a 48bit address bus uses a 3 level page lookup table. Outline a reasonable scheme for dividing the 48 bit addresses into regions for the various levels of lookup. In your answer, you should first decide on the size of frames/pages to manage. Give the size of your page tables, and justifications for your decisions.

Q2. Consider the following processes, with the length of the CPU-burst time given in milliseconds:

Process	Burst time	Priority
P1	10	3
P2	1	1
P3	2	3
P4	1	4
P5	5	2

The processes are assumed to have arrived in the order P1, P2, P3, P4, P5, all at time 0.

(A) Draw four Gantt charts illustrating the execution of these processes using FCFS, SJF, a non-preemptive priority (a small priority number implies high priority), and RR (quantum = 1) scheduling.

(B) What is the turnaround time and waiting time of each process for each of the scheduling algorithms in (A)?

(C) Which of the schedules in part (A) results in minimal average waiting time.

Q3. In a system that uses paging, each virtual address is 16 bits, of which 10 bits is the page number, and the remaining 6 bits is the offset. Each entry in the page table includes an 8- bit base address. Answer the following questions (answers specified as powers of two are fine).

a. What is the maximum number of pages available to each process?

b. What is the total number of available page frames in physical memory?

c. How many words are in a page frame?

d. Suppose the page table for a given process is as given below. What is the physical address that corresponds to the virtual address 0000 0000 1100 1001? (Spaces are given only to help you count bits).

0	1010 1111
1	0000 0000
2	1110 1000
3	1111 0000
4	0011 0011
5	0100 1001

4. Explain an algorithm with multiple instances of resources to Avoid deadlocks.