BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

I Semester 2019-2020

CS F372 Operating Systems Comprehensive Exam

9/12/2019 Time: 105 minutes M.M: 48

PART B (OPEN BOOK)

Note: Attempt all parts of a question together. There are 2 printed pages.

Q1. Assume an **Inverted Page Table (8-entry IPT)** is used by a processor with a 32-bit virtual address. The memory page size is **2MB**. The complete IPT content is shown below. The Physical Page Number (PPN) starts from **0 to 7** from the top of the table. There are three active processes, P1 (PID=1), P2 (PID=2) and P3 (PID=3) running in the system and the IPT holds the translation for the entire physical memory. Answer the following questions.

Valid	Process ID (PID)	Virtual Page Number (VPN)
1	1	0x3fe
1	3	0x001
1	2	0x1ad
1	3	0x7fd
1	2	0x3fe
1	1	0x2bf
0	2	0x7fd
1	2	0x0bf

a) What is the size (in MB) of the physical memory available?

b) To which "physical address" does the "virtual address" **0x7fdd8f64** of **P2** map? Derive and write down the **complete** address in **Hex** value. (If there is no valid mapping, please answer "page fault").

c) To which "**virtual address**", of "**which process**", does the physical address **0x78e968** map? Please derive and write down the complete address in **Hex** value. If you cannot find a valid mapping, please answer "address not found".

d) Now the OS writer decides to use an single level linear page table for each process without changing the page size. How big (in bits or bytes) the **total page tables** are needed for these active processes? Assume you have 2 extra bits (valid and dirty) in addition to the PPN for each page table entry.

[1+2*3]

Q2. A processor supports 2 level paging with page size of 1 MB . Each individual page table fits exactly into one memory frame, and the size of each page table entry (PTE) is 16 bytes.

(a) What is the maximum size of a virtual address space in this system?

(b) find the total number of pages supported by the system

(c) Suppose that there is a process with a virtual address space of the maximum size. How much memory is occupied by the page tables for this process?

(d) Suppose that there is a process with a virtual address space of size 32 MB . Also suppose that the entire address space is in memory. How many valid PTEs will exist in the page tables for this process total amount of memory required by this process?

(e) Draw the complete linear to physical address translation diagram, completely indicating the size of various fields of linear address and address computation.

[2+2+2+2+4]

Q3.

a) Write a code segment descriptor for an application code segment with following specifications.
The size of segment is 2MB, the base address of the allocated segment is 42960000H. the defined code segment is non conforming and is only used for storing the code. The code segment being described is present and has been accessed .

b) What is the relevance of Dword count field in call gate descriptor.

c) A conforming code segment is having privilege level 1. List the privilege level of the processes that could access this code . Give reason for your answer .

[4+2+2]

Q4. Suppose that pages in a virtual address space are referenced as follows
1, 2, 3, 1, 2, 6, 1, 3, 4, 5, 1, 2, 3, 1, 5, 6, 2, ,5, 7, 3, 1
If the system has 3 empty frames available, show the content of frames after every memory reference for the following

(A) Find the content of frames after every memory reference and the number of page faults, for the replacement algorithm which guarantees least number of page faults

(B) Show the content of frames after every memory reference and find number of page faults for the following replacement algorithms

a. LRU

b. Second Chance

[2+2+2]

Q5. A SATA Hard disk operating at 5200 RPM has total number of 180 cylinders numbered from 0 to 179. At some instance of time the disk has following outstanding request .
30, 26, 130, 55, 6, 89, 37, 12 22, 64 , 46, 28, 18 and 32.
The current head position is at cylinder number 16 and the previous cylinder number was 14. Write the disk scheduling sequence for the following algorithms

(A) SCAN
(B) SSTF
(C) FCFS

[2*3]

Q6. An organization is having 3.2 Tera bytes of data which it wants to port on a storage box . The storage box can support RAID 0 , RAID 1, RAID 2, and RAID 6. The supplier has agreed to supply 15000 RPM, 900GB SAS drive with 600mbps data transfer rate .

A) List the number of disks required for each of the RAID level listed above. Give reason for the answer. (Answers with no reason will not be given any credit)

B) If the average seek time for the above mentioned disk is 4 mili seconds , find the IOPS for the single disk

C) Write the hamming code for 8 bit data: 0 1 1 0 0 1 1 1

D) Prove that to modify a block of data in case of RAID 5 , you require two reads and two write operation

[2+2+2+2]

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BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

I SEMESTER 2019-2020

OPERATING SYSTEMS CS F372 PART A(CLOSED BOOK)

COMPREHENSIVE EXAMINATION

9/12/2019 DURATION : 75 MINUTES MM: 45

Note: This part of the question paper consists of **45** objective type questions. Each correct answer carries **+1** marks while each incorrect answer carries **–1** mark. Questions not attempted, carry no credit. Write the most appropriate answer against a question on the separate answer sheet provided. You can take Part B after submitting Part A.

Q1. A system has 4 processes P1, P2 , P3 and P4 which arrive at same time . The CPU burst required for each of the processes are 24, 4 , 16 and 8 respectively. If FCFS algorithm is used for scheduling ,the waiting time for process P2 and P4 is ,

A) 24, 28
B) 28, 52
C) 24, 44
D) 24, 52

Q2. A system has 4 processes P1, P2 , P3 and P4, which arrive at same time . The CPU burst required for each of the processes are 24, 4 , 16 and 8 respectively. The average wait time in case of FCFS and SJF scheduling algorithm will be

A) 96 and 44
B) 24 and 11
C) 28 and 16
D) 52 and 54

Q3. A system has 4 processes P1, P2 , P3 and P4 ,which arrive at same time . The CPU burst required for each of the processes are 24, 4 , 16 and 8 respectively. The average turnaround time in case of FCFS and SJF scheduling algorithm will be

A) 37 and 24
B) 24 and 37
C) 28 and 16
D) 148 and 94

Q4. Which of the following statement is true for SRTF scheduling algorithm

A) It gives reduced average wait time and increased average turnaround time
B) It gives reduced average turnaround and increased average wait time
C) It results in increased average wait time and increased average turnaround time.
D) It provides reduced average wait time and reduced average turnaround time

Q5. Scheduling algorithms ,that can cause starvation are

A) SRTF, SPN, Priority ,Multilevel feedback queue
B) SJF , Priority and VRR
C) SJF, VRR and Round robin
D) SJF, VRR and multilevel queue

Q6. A system has three processes P1, P2, and P3 belonging to three different groups G1, G2, G3 respectively. It uses fair share scheduling . The base priority of P1, P2 and P3 processes are 50, 40 and 45 respectively. The group weightage for G1, G2, and G3 are 0.33, 0.33 and 0.34 . Priority is calculated every 1 second . In one second sixty clock ticks are generated by the system. If system runs for three seconds, the order in which the processes will execute is

A) P1, P2, P3
B) P1, P3, P2
C) P2, P1, P3
D) P2, P3, P1

Q7. process synchronization problem is faced due to the fact that system has
A) Finite amount of sharable resource
B) Infinite amount of sharable resource
C) Finite amount of non sharable resource
D) Infinite amount of non sharable resource

Q8. A system is having more than one processes which are not aware of existence of the other processes. When such processes are concurrently executing, they
A) May require mutual exclusion and may cause dead lock to occur
B) May cause dead lock and starvation to occur
C) Can only cause starvation
D) May require mutual exclusion ,can cause dead lock and starvation to occur

Q9. Which of the following statements about Compaction is false?
A) Compaction is used to deal with the problem of external fragmentation
B) Compaction is only possible if the address binding takes place during loading time
C) Compaction of swap space on hard disk incurs large overhead
D) A process currently doing I/O to its local buffers cannot be compacted

Q10. Which of the statement is not true for the special instructions designed for process synchronization?
A) Can be used to support multiple critical section
B) Can lead to starvation
C) They do not use busy waiting
D) Can cause dead lock

Q11. If a counting semaphore variable S is initialized to 3 and following line of code is executed,
signal (S)
<critical section>
wait (S)
The maximum number of processes that can simultaneously access the critical section
A) will always be less than three in number
B) will be less than or equal to three
C) There is no limit on the number of processes that can simultaneously access the critical section
D) None of the above

Q12. A system has two resources R1 and R2 which are guarded by semaphore variables P and Q . At some instance of time , the value of semaphore variable P is -2 and Q is 3. This implies the condition :
A) Two processes can access resources R1 without getting blocked and three processes are accessing resource R2
B) Two processes can access resources R2 without getting blocked and three processes are accessing resource R1
C) Two Processes are blocked on semaphore variable P and nothing can be said about the number of processes currently accessing resource R2
D) Two Processes are blocked on semaphore variable P and three processes are currently accessing resource R2 .

Q13. In case of message passing , which of the following pair of synchronization primitive is most commonly used ?

A) Blocking send Non Blocking receive
B) Non blocking send and Non Blocking receive
C) Blocking send and Blocking receive
• D) Non Blocking send and Blocking receive

Q14. Choose the incorrect statement for processes issuing the receive statement

A) If the message was previously sent, it receives the message
B) if the message is not sent, the blocking receive processes waits for message to arrive
• C) If the message is not sent, the non blocking receive processes waits for message to arrive
D) If the message is not sent, the non blocking receive processes abandons the message

Q15. A processor has 30 Bit instruction pointer and uses 4KB page . It can store 16 most recently translated entries in TLB. The TLB reach of the processor is

• A) 64KB
B) 4KB
C) 256 KB
D) 1000 MB

Q 16. A processor that supports paging , has instruction pointer of size 26 Bit and uses 16 KB pages. The maximum number of pages that can be supported

A) 16 K
B) 64K
• C) 4K
D) nothing can be said as size of page table entry is not specified

Q17. In case of a system supporting demand segmentation , address binding used can be

A) Compile time , load time and execution time
B) Compile time only
C) Load time or execution time
D) Execution time only.

Q18. Which of the following statements are true for reducing the page size.

1. it will decrease the external fragmentation
2. it will increase the size of page table
3. it will require more number of I/O operations

A) Statement number 1, 2 and 3 are true
B) Only statement number 1 and 2 are correct
C) Only statement number 1 and 3 are correct
• D) Only statement number 2 and 3 are correct

Q19. In a system supporting Paging , a processes is trying to read a 8 bit data . The read could involve , reading 4 bytes of information from page directory and 4 bytes of information from page table. To avoid such a overhead, Intel processors

A) store the translated address in hidden part of segment register
B) store the translated address in instruction pointer
C) store the translated address in task state segment
• D) store the translated address in translation look aside buffer.

Q20. In case of Intel X86 / Pentium processor stack segment can be defined as

A) Expand up segment
B) Expand down segment
C) System segment
D) Expand up or expand down

Q21. In case of Intel X86 processor, the size of page directory and page table entries are

A) 4 byte, 4 byte respectively
B) 4 byte , 8 byte respectively
C) 20 bit , 12 bit respectively
D) 8 byte , 8 byte respectively

Q22. In case of Intel X86 Processor which supports 4MB page, the size of page table and maximum number of page table entries are :

A) 4KB , 1K respectively
B) 4KB and 4K entries respectively
C) 4MB and 1K respectively
D) 4MB and 1M entries respectively

Q23. A hypothetical processor supports an add instruction : ADD X, Y,Z . Where X,Y and Z are pointer to 32 bit integer locations. The instruction adds the content of memory location X & Y and stores the result in memory location Z. Assume that the instruction size is 32 bit. The processor supports paging. The minimum number of frames that should be allocated to the process is

A) 1 B) 4 C)6 D)8

Q24. A Processor Supports 8 KB page . A process of size 38 KB is executing on this machine. Assume complete processes is loaded in the main memory . The number of pages allocated to processes and % of memory wastage due to internal fragmentation is

A) 5 pages & 50% B) 4 Pages & 50 % C) 5Pages & 5% D) 5 pages and 25%

Q25. In case of Intel processor , pages are aligned to

A) 4K Boundary B)2K boundary C)8K boundary D)None of the above

Q26. Choose the most appropriate statement regarding number of page fault

A) Page fault increases with increasing number of allocated frames
B) Page fault decreases with decreasing number of allocated frames
C) Page fault decreases with increasing number of allocated frames
D) Page fault may increase or decrease with increasing number of frame allocation

Q27. The CPU utilization,

A) increases with increasing degree of multiprogramming
B) decreases with increasing degree of multiprogramming
C) first increase and then decreases with the increasing degree of multiprogramming
D) first decreases and then increases with the increasing degree of multiprogramming

Q28. In case of hard disk, where zoned data recording is used

A) Outer tracks store more information and transfer more data per revolution
B) Outer tracks store less information and transfer more data per revolution
C) Inner tracks store more information and transfer more data per revolution
D) The amount of data stored and data transfer is same for outer and inner track

Q29. Logical block address to Physical block address mapping is

A) stored in kernel space of operating system
B) stored in user process space
C) stored in task state segment of a process
D) stored in disk controller firmware

Q30. A storage box which uses RAID 4 , has total number of 5 disks with different capacity . The capacities of disk are 900 GB, 900GB , 600GB, 1200GB and 300GB. The maximum amount of user data that can be stored is

A) 3900 GB B)3600 GB C) 1500GB D)1200GB

Q31. A RAID Level which uses block interleaved stripes would

A) Provide Higher data transfer rate per application and higher I/O rate
B) Provide higher data throughput and higher I/O rate
C) Provide higher data throughput and lower I/O rate
D) Provide lower data throughput and lower I/O rate

Q32. A storage is using RAID level 1+0 and has total of 8 numbers of 600GB hard disks. The theoretical maximum usable capacity of the storage system is

A) 4800 GB B) 4200 GB C) 1800GB D)3600GB

Q33. The minimum number of disks that can be used for RAID level 5 and RAID level 6 are

A) 3 and 3 respectively
B) 2 and 3 respectively
C) 3 and 5 respectively
D) 3 and 4 respectively

Q34. Choose the most appropriate statement

A) if system is in safe state , dead lock may occur
B) If system is in unsafe state deadlock will always occur
C) If the system is in unsafe state deadlock may occur
D) None of the above

Q35. Which of the following does not cause an asynchronous interrupt?

A) Check for burst exceeding time quantum each time a process is scheduled
B) System call
C) I/O completion
D) None of the above

Q36. A dual-mode system is often used by many architectures. Privileged instructions executed in non privileged mode will cause:

A) The processor to halt
B) An asynchronous interrupt to occur
C) Instruction will execute normally
D) None of the above

Q37. In case of system supporting global page replacement policy

A) Processes can control their own page fault rates
B) Processes cannot control their own page fault rates
C) Nothing can be said about the page fault rates as information about number of pages is required
D) Page fault rate is same as in case of local page replacement policy

Q38. The effect of thrashing can be limited by

A) Choosing a local page replacement policy
B) Choosing a global page replacement policy
C) Increasing the degree of multiprogramming
D) None of the above

Q39. GDT table can have maximum of _____ entries

A) 8K B) 4K C) 2K D) 64K

Q40. In case of classical definition of monitor, when a process executes signal operation inside the monitor then,

A) The process must leave the monitor immediately
B) The process must wait inside the monitor
C) The process must finish its execution and then leave the monitor
D) all of the above

Q41. A signal on a condition variable by a process P inside a monitor can have P continue rather than Q, where Q is the process waiting on the condition variable. The implication of this policy is:

A) Only one of the process can acquire the monitor lock
B) P is slower than Q
C) dead lock will occur
D) The condition that caused the signal may become invalid by the time P finishes

Q42. Which of the following is not a correct reason for a user process termination?

A) Time limit exceeded
B) Attempt to execute a privileged instruction
C) Parent requests termination
D) I/O failure

Q43. In Unix system V operating system, which of the following is not true?

A) All processes are children of the init process
B) The swapper process is the first one to be created at startup
C) The init process is the first one to be created at startup
D) A process running in kernel mode can be preempted

Q44. In Intel X86 processor, page directory base address and GDT base address is stored in

A) CR0 and GDTR register B) CR3 and GDTR register
B) CR3 and LDTR register D) CR0 and LDTR register

Q45. Which of the following statements about Symmetric Multiprocessing is not true?

A) Kernel can execute on any processor
B) Typically each processor does self-scheduling form the pool of available processes
C) Symmetric Multiprocessing is a case of tightly coupled systems
D) None of the above

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