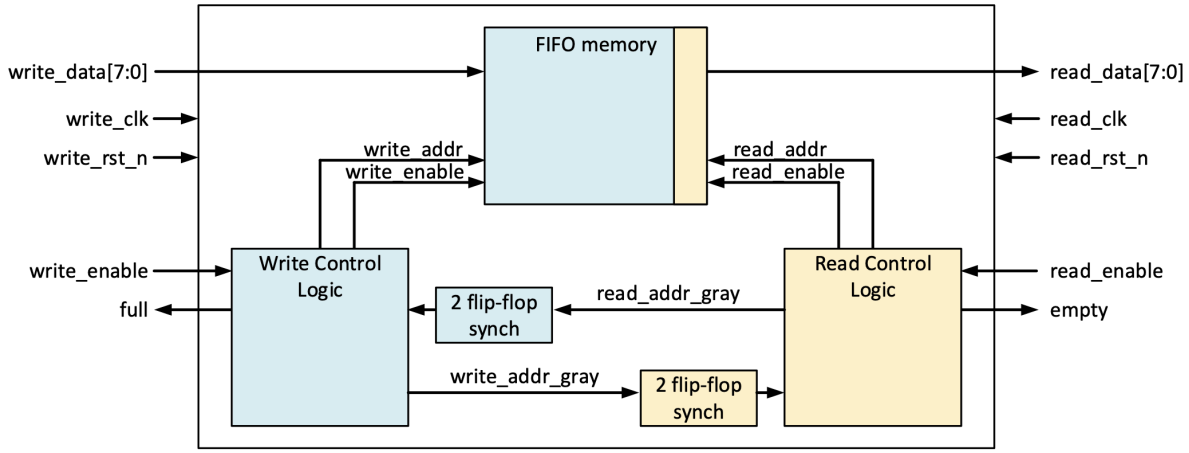
Architectural Requirements:

1. Interface requirements
    a. Inputs: write_clk, read_clk, write_rst_n, read_rst_n, write_data[7:0], write_enable, read_enable
    b. Outputs: read_data[7:0], fifo_full, fifo_empty
2. FIFO size requirements
    a. 8 addresses, 8-bit data
3. FIFO functional requirements
    a. If FIFO is full, FIFO write is not possible until FIFO is no longer full
    b. If FIFO is empty, FIFO read is not possible until FIFO is no longer empty
4. CDC requirements
    a. Read/write pointers need to be synchronized across clock domains using Gray pointers
    b. Two flip-flop synchronizers needed for pointer synchronization



CDC FIFO block diagram