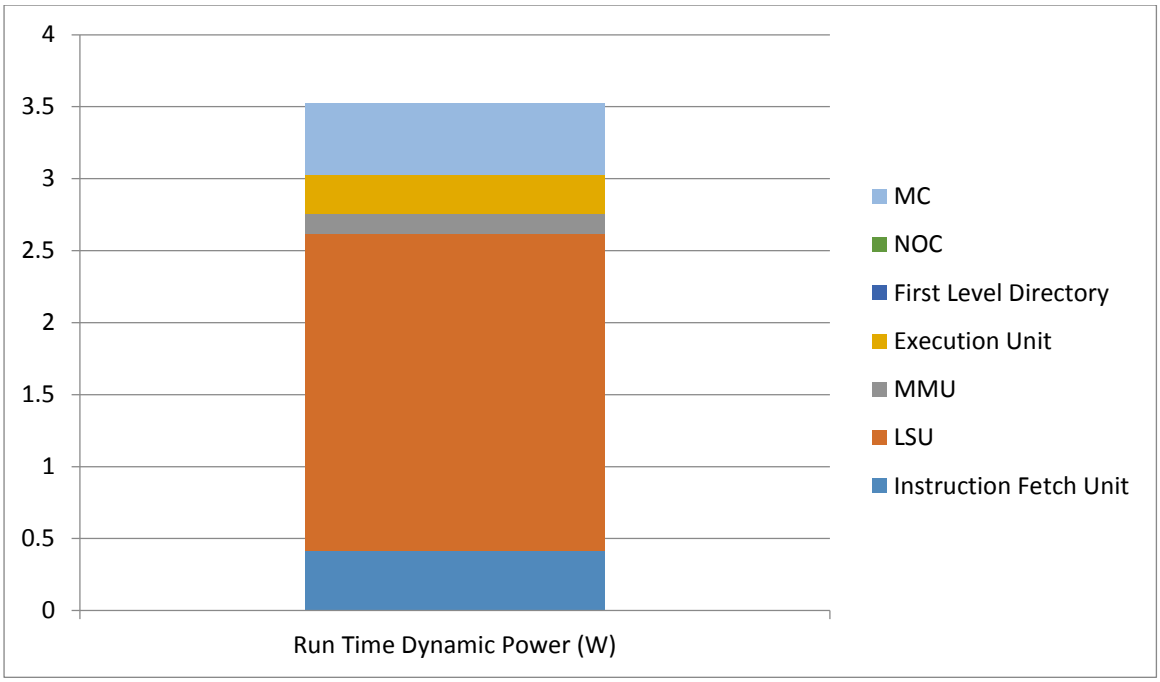
LAB 4 Report

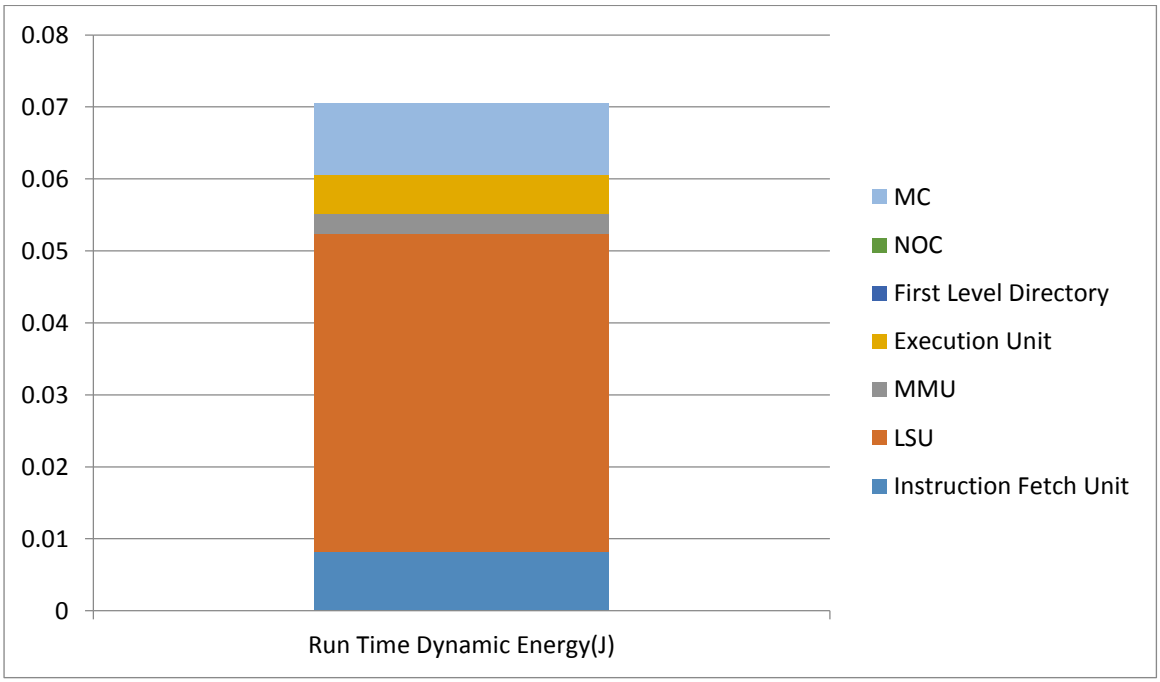


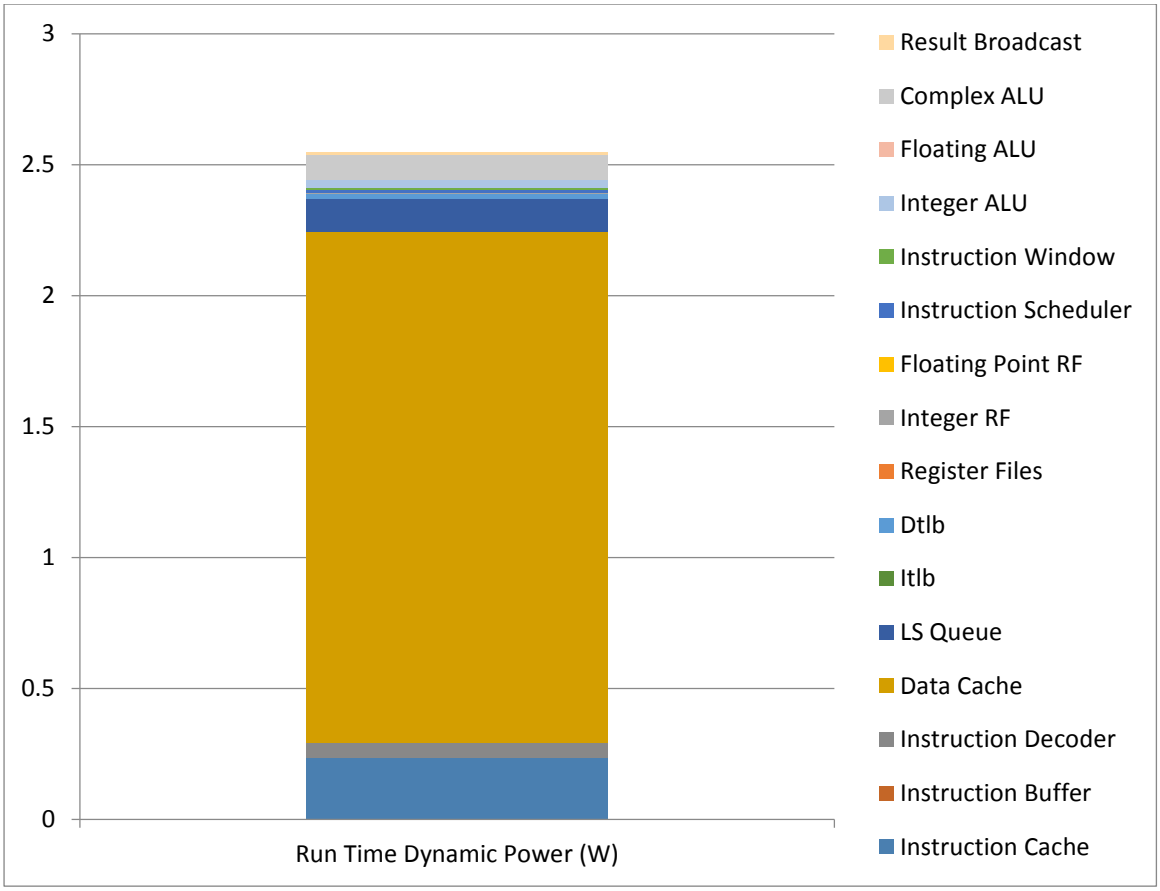
Execution Time Calculation:

Execution Time = Total Cycles *(1/ Frequency(default))

= 24318949 * (1/(1200*10^6))

= 0.02 s





The run time dynamic power is observed to be dominated by the data cache.

Frequency Variation

Frequency	IPC	Power(W)	Energy(J)	Energy Delay Product
900	0.323284	2.674	0.07225	1.95 * 10^-3
1200	0.323284	3.5223	0.07044	1.408 * 10^-3
1500	0.323284	4.27923	0.06937	1.124 * 10^-3

Explanation:

Dynamic Power = C(V^2)f

Thus **P α f**

As frequency increases we observe that the Power correspondingly increases.

GHR Variation

GHR Length	IPC	Power(W)	Energy(J)	Energy Delay Product
12	0.323284	3.5223	0.07044	1.408 * 10^-3
8	0.315881	3.4641	0.0718	1.488 * 10^-3
4	0.306698	3.39194	0.07245	1.547 * 10^-3

Explanation:

The number of mis-predictions decreases with increase in GHR for this trace. That is storing longer histories helps predict branches having correlation over longer duration. Due to less miss-prediction the IPC is seen to increase. Also, as the prediction improves, the number of control hazards decreases leading to better utilization of the pipeline. Resulting in decrease in execution time. Power being inversely proportional to time, it increases correspondingly. For the same reason, the energy decreases because now the entire system is active for a lesser amount of time and with better efficiency.

Cache Size Variation

Cache Size	IPC	Power(W)	Energy(J)	Energy Delay Product
1 MB	0.323284	3.5223	0.07044	1.408 * 10^-3
2 MB	0.323284	3.76637	0.07532	1.506 * 10^-3
4 MB	0.323284	4.57129	0.09142	1.828 * 10^-3

Explanation:

It is observed that trace's working set requirements is satisfied by a cache size of 1MB. Resulting in a similar number of capacity misses. The IPC is thus observed to remain same. The change in IPC is observed when the cache size is decreased to the range of 64-128 KB range. Although the IPC remains same, the power increases due to the additional hardware which includes comparator logic, tag store, etc. This increases the power, which is ultimately wasted.

Counter Values for all simulation test cases

Default Case:

no_total_instructions:7861921
no_total_cycles:24318949
no_fp_instructions:7168
no_int_instructions:5105019
no_branch_instructions:1603095
no_load_instructions:1739490
no_store_instructions:978692

no_icache_read_accesses:7861921
no_branch_mispredictions:50706
no_scheduler_access:24128251
no_int_regfile_reads:1927819
no_float_regfile_reads: 14336

no_mul_accesses:3494784

no_dcache_reads:1888787
no_dcache_writes:979580
no_memory_accesses:3029
no_dcache_read_miss:5040

no_dcache_write_miss:2141

no_tlb_miss:154337

no_int_regfile_writes:1489064
no_float_regfile_writes: 7168

GHR = 8

no_total_instructions:7861921
no_total_cycles:24475306
no_fp_instructions:7168
no_int_instructions:5105019
no_branch_instructions:1603095
no_load_instructions:1739490
no_store_instructions:978692

no_icache_read_accesses:7861921
no_branch_mispredictions:241040
no_scheduler_access:23522229
no_int_regfile_reads:1927819
no_float_regfile_reads: 14336

no_mul_accesses:3494784

no_dcache_reads:1806024
no_dcache_writes:979570
no_memory_accesses:3029
no_dcache_read_miss:5040

no_dcache_write_miss:2151

no_tlb_miss:71574

no_int_regfile_writes:1489064
no_float_regfile_writes: 7168

GHR = 4 rest default

no_total_instructions:7861921
no_total_cycles:25634041
no_fp_instructions:7168
no_int_instructions:5105019
no_branch_instructions:1603095
no_load_instructions:1739490
no_store_instructions:978692

no_icache_read_accesses:7861921
no_branch_mispredictions:490321
no_scheduler_access:23600412
no_int_regfile_reads:1927819
no_float_regfile_reads: 14336

no_mul_accesses:3494784

no_dcache_reads:1888817
no_dcache_writes:979583
no_memory_accesses:3029
no_dcache_read_miss:5010

no_dcache_write_miss:2138

no_tlb_miss:154337

no_int_regfile_writes:1489064
no_float_regfile_writes: 7168

Cache Size: 2 MB

no_total_instructions:7861921

no_total_cycles:24318949
no_fp_instructions:7168
no_int_instructions:5105019
no_branch_instructions:1603095
no_load_instructions:1739490
no_store_instructions:978692
no_icache_read_accesses:7861921
no_branch_mispredictions:50706
no_scheduler_access:24128251
no_int_regfile_reads:1927819
no_float_regfile_reads: 14336

no_mul_accesses:3494784

no_dcache_reads:1888787
no_dcache_writes:979580
no_memory_accesses:3029
no_dcache_read_miss:5040

no_dcache_write_miss:2141

no_tlb_miss:154337

no_int_regfile_writes:1489064
no_float_regfile_writes: 7168

Cache Size: 4 MB

no_total_instructions:7861921
no_total_cycles:24318949
no_fp_instructions:7168
no_int_instructions:5105019
no_branch_instructions:1603095
no_load_instructions:1739490
no_store_instructions:978692

no_icache_read_accesses:7861921
no_branch_mispredictions:50706
no_scheduler_access:24128251
no_int_regfile_reads:1927819
no_float_regfile_reads: 14336

no_mul_accesses:3494784

no_dcache_reads:1888787
no_dcache_writes:979580
no_memory_accesses:3029
no_dcache_read_miss:5040

no_dcache_write_miss:2141

no_tlb_miss:154337

no_int_regfile_writes:1489064
no_float_regfile_writes: 7168