

PCB MANUFACTURING SPECIFICATIONS

"Altium Templates"

SPECIFICATIONS

NOTE #	NOTE
1	ALL SPECIFICATIONS REFERENCED ARE OF THE REVISION SPECIFIED IN THE TITLE BLOCK
2	SUPPLIER SHALL NOT MODIFY THE DESIGN OR APPROVED STACK-UP WITHOUT WRITTEN PERMISSION
3	ALL MATERIALS SHALL BE RoHS COMPLIANT AND FINAL PRODUCT SHALL BE ACCEPTABLE TO USE IN RoHS ASSEMBLY. RoHS LOGO SHALL BE MARKED IN SILKSCREEN INK NEAR BY THE SUPPLIER.
4	COPPER FOIL: REFER TO LAYER STACK LEGEND FOR Cu THICKNESS DETAILS. ALL Cu THICKNESSES ARE FINISHED AND INCLUDE BASE FOIL PLUS Cu PLATING ON PLATED LAYERS
5	ELECTRICAL TEST: ALL PRINTED CIRCUITS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS/SHORTS USING PROVIDED NETLIST. REJECTED PRINTED BOARDS MUST BE CLEARLY MARKED WITH NON-CONDUCTIVE, PERMANENT INK.
6	MARKINGS: VENDOR MARKING AND DATE/LOT CODES SHALL BE LOCATED ON THE BOARD IN THE RESERVED AREA AS SPECIFIED IN THE GERBER LAYER "PCBM_NOTES" BY THE TEXT "PLACE MARKINGS HERE".
7	MARKINGS: THE SIDE ONTO WHICH PLACE THE MARKINGS IS AT THE SUPPLIER DISCRESSION UNLESS OTHERWISE NOTED ONTO THE LAYER "PCBM_NOTES"
8	SUPPLIER SHALL CHECK PCBM_NOTES LAYER BEFORE ASKING FOR CLARIFICATIONS
9	MANUFACTURE TENTED/PLUGGED VIAS AS SPECIFIED IN THE GERBER FILES

SPECIFICATIONS

LENGHT	80.00mm
WIDTH	75.00mm
LAYERS	2
MATERIAL	FR-4
MATERIAL MIN TG	130-140
TRACK WIDTH/CLEARANCE	8 mils / 8 mils
THICKNESS	1.6mm
COPPER THICKNESS	35um (1oz)
SOLDERMASK	YES, TOP AND BOTTOM
SOLDERMASK COLOR	RED
SILKSCREEN	YES, TOP AND BOTTOM
SILKSCREEN COLOR	WHITE
SURFACE FINISH	HASL LEAD FREE
GOLD FINGERS	NO
CHAMFERING	NO
IMPEDANCE CONTROL	NO
HALF-CUT/CASTELLATED HOLES	NO
BURIED/BLIND VIAS	NO
VIAS FILLED WITH RESIN	NO
CARBON MASK	NO
COUNTERSINKS/COUNTERBORES	NO
Z-AXIS MILLING	NO
PEELABLE SOLDERMASK	NO

Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber
		Top Overlay			Legend	GTO
	Surface Material	Top Solder	0.03mm	SM-001	Solder Mask	GTS
	Lead-Free	Top Surface Finish	0.02mm		Surface Finish	
	CF-004	Top Layer	0.04mm		Signal	GTL
	Core		1.50mm	Core-043	Dielectric	
	CF-004	Bottom Layer	0.04mm		Signal	GBL
	Lead-Free	Bottom Surface Finish	0.02mm		Surface Finish	
	Surface Material	Bottom Solder	0.03mm	SM-001	Solder Mask	GBS
		Bottom Overlay			Legend	GBO

Total thickness: 1.66mm

NON-COPPER LAYER THICKNESS FOR REFERENCE ONLY
LAYERS OF TYPE "INTERNAL PLANE" ARE NEGATIVE

Title: Altium Templates		Author:	CONFIDENTIAL My Company Address Line 1 Address Line 2 Address Line 3 Address Line 4
Size: A3	Prj: Altium Templates	Approved:	
Unit: mm		Edited: 25/08/2020	
		Variant: [No Variations]	
Date: 25/08/2020 22:57	Sheet 1 of 3	SW version: 20.1.14.287	
Git Hash: 8dce3f0d4731524eb776483ab40d9ceaa18d5c61 [No modification]			
File: C:\Users\d\Documents\Fermium\AltiumTemplates\Draftsman\PCB MANUFACTURING.DwfDot			

[YOUR LOGO HERE]

A

B

C

D

E

F

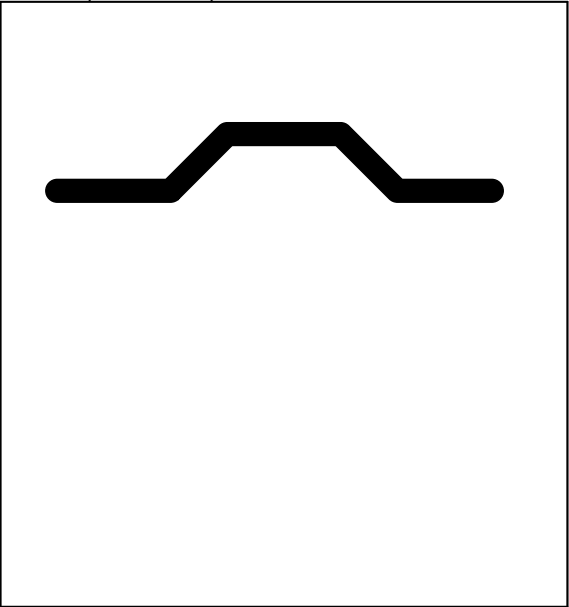
G

H

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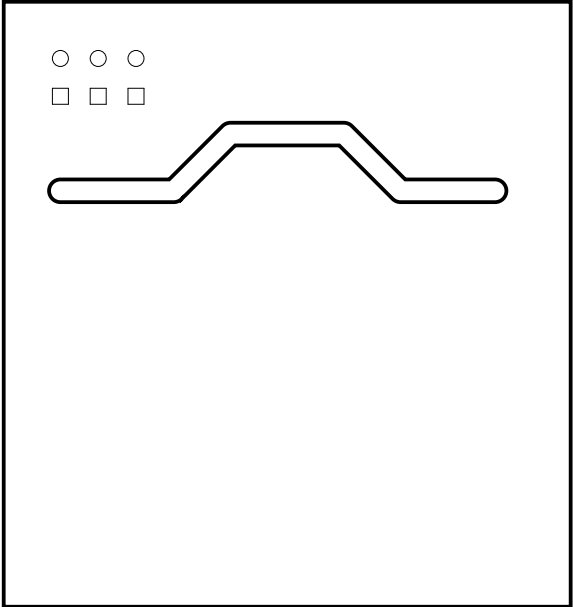
Board (Scale 1:1)



2

2

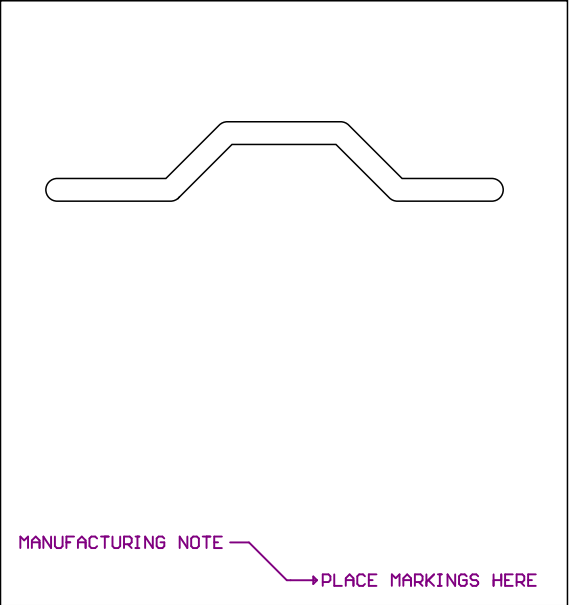
Drill Drawing View (Scale 1:1)



3

3

PCBM Notes (Scale 1:1)



4

4

5

5

ALWAYS CAREFULLY READ
THE NOTES ON THIS LAYER!

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
○	3	0.71mm	Plated	
□	3	0.76mm	Plated	
	6 Total			

6

6

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[YOUR LOGO
HERE]

A

B

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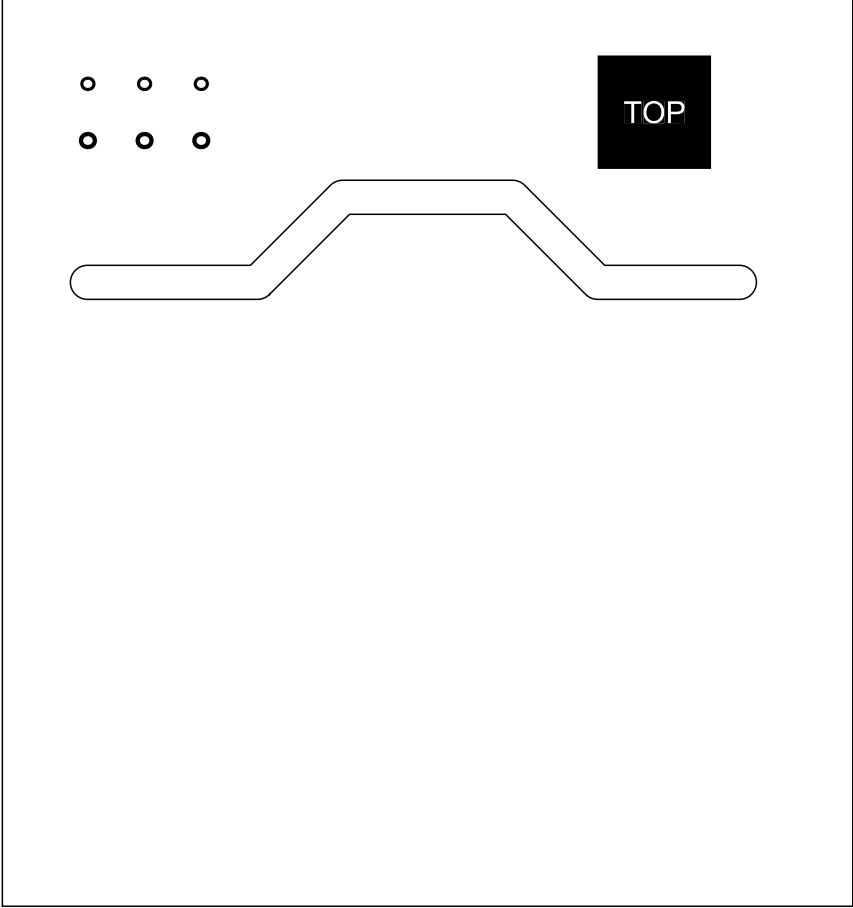
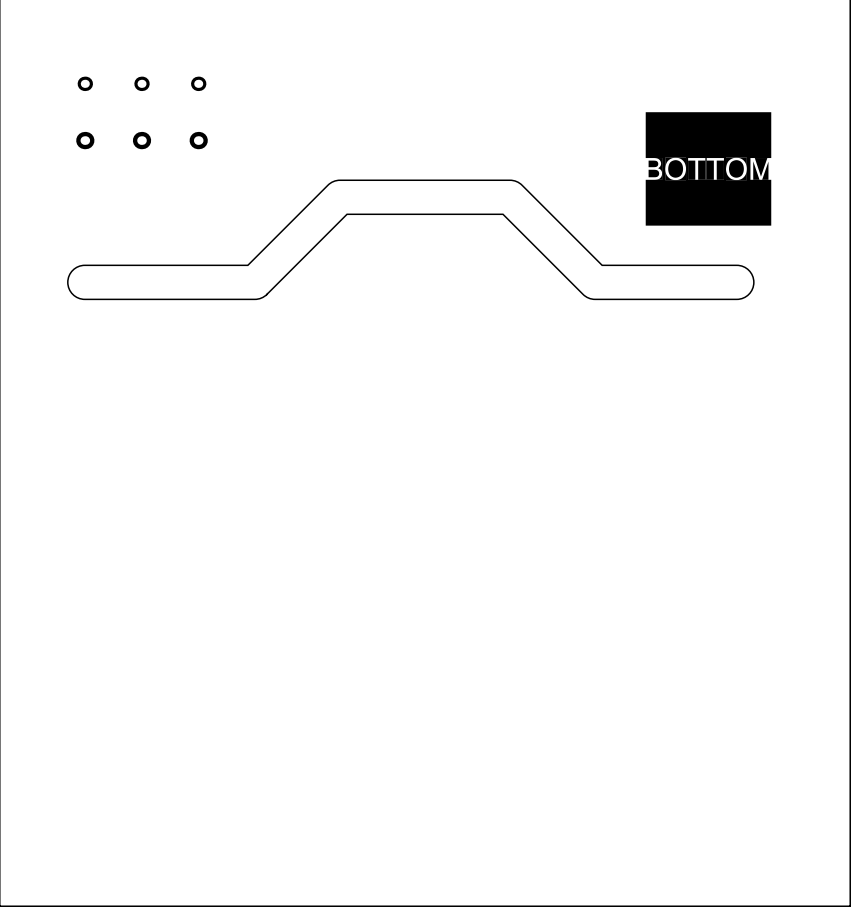
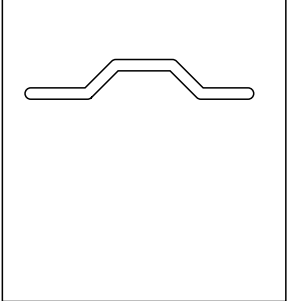
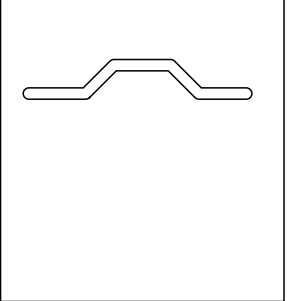
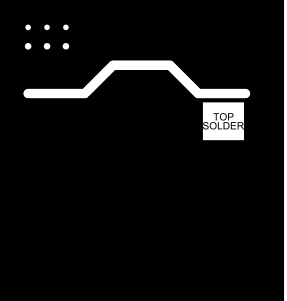
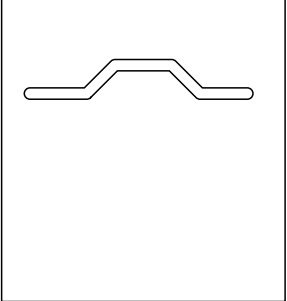
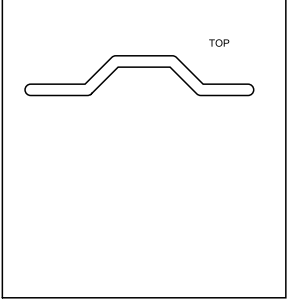
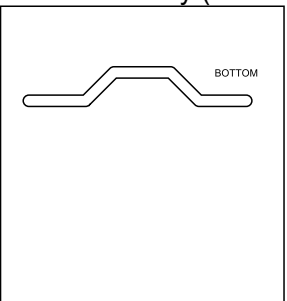
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	A	B	C	D	E	F	G	H																							
1	<div>Top Layer (Scale 3:2)</div> 			<div>Bottom Layer (Scale 3:2)</div> 																											
2																															
3																															
4	<div>Top Paste (Scale 1:2)</div> 	<div>Bottom Paste (Scale 1:2)</div> 		<div>Top Solder (Scale 1:2)</div> 		<div>Top Paste (Scale 1:2)</div> 																									
5																															
6	<div>Top Overlay (Scale 1:2)</div> 	<div>Bottom Overlay (Scale 1:2)</div> 		<table><tr><td colspan="2">Title: Altium Templates</td><td>Author:</td><td>CONFIDENTIAL</td></tr><tr><td>Size: A3</td><td rowspan="2">Prj: Altium Templates</td><td>Approved:</td><td>My Company</td></tr><tr><td>Unit: mm</td><td>Edited: 25/08/2020</td><td>Address Line 1</td></tr><tr><td>Date: 25/08/2020 22:57</td><td>Sheet 3 of 3</td><td>Variant: [No Variations]</td><td>Address Line 2</td></tr><tr><td colspan="2">Git Hash: 8dce3f0d4731524eb776483ab40d9ceaa18d5c61 [No modification]</td><td>SW version: 20.1.14.287</td><td>Address Line 3</td></tr><tr><td colspan="2">File: C:\Users\d\Documents\Fermium\AltiumTemplates\Draftsman\PCB MANUFACTURING.DwfDot</td><td></td><td>Address Line 4</td></tr></table>				Title: Altium Templates		Author:	CONFIDENTIAL	Size: A3	Prj: Altium Templates	Approved:	My Company	Unit: mm	Edited: 25/08/2020	Address Line 1	Date: 25/08/2020 22:57	Sheet 3 of 3	Variant: [No Variations]	Address Line 2	Git Hash: 8dce3f0d4731524eb776483ab40d9ceaa18d5c61 [No modification]		SW version: 20.1.14.287	Address Line 3	File: C:\Users\d\Documents\Fermium\AltiumTemplates\Draftsman\PCB MANUFACTURING.DwfDot			Address Line 4	<div>[YOUR LOGO HERE]</div>
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